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ABSTRACT

A low temperature catalytic growth of orderly ultrathin silicon nanowires (SiNWs) is desirable for the construction of monolithic 3D stacked electronics but usually suffers a large diameter fluctuation and a low growth deployment rate (GDR). In this work, the ultra-confined growth dynamics of in-plane solid–liquid–solid SiNWs within narrow groove tracks has been systematically investigated, and a converging-guiding-track strategy is proposed and testified to accomplish 100% GDR of ultra-dense and uniform SiNW array, with diameter and spacing of only $D_{nw} = 22.5 \pm 3.5$ nm and 25 nm, respectively. Despite a low temperature growth at 350 °C, the SiNWs are found to be all monocrystalline and Si⟨100⟩ oriented, while prototype Schottky barrier tunneling field effect transistors built on the SiNW channels demonstrate a high $I_{on/off}$ ratio and subthreshold swing of $>10^5$ and 197 mV dec^{-1}. This new strategy complements a long-missing key capability of catalytic growth approach to serve a reliable integration technology of ultrafine high quality 1D c-Si channels, without the need of preexisting wafer substrate, for a wide range of 3D electronics, neuromorphic, and logic-in-memory functionalities.

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Taking a low temperature, high-yield, and versatile catalytic growth to produce orderly ultra-dense and thin c-Si nanowires (SiNWs), as high-quality semiconducting 1D channels in microelectronics, has been a long-sought after goal over the decades.[1–4] This motivation becomes stronger with the scaling of large-scale-electronics approaching to fundamental limits, where monolithic 3D integration has been widely identified as a promising paradigm to further push the Moore's Law,[5,6] in a stacked configuration as diagramed in Fig. 1(a), and to explore non-von Neumann neuromorphic or logic-in-memory functionalities.[7–10] However, fabricating another c-Si logic layer *monolithically* over the previous front-end-of-line (FEOL) logics is, by itself, a formidable challenge because of (i) the lack of c-Si wafer in the top layer and that (ii) the back-end-of-line (BEOL) fabrication processes are subject to a tight thermal budget limit (≤450 °C) to protect the integrity of bottom FEOL logics.[11,12]

To this end, a low temperature catalytic growth of monocrystalline SiNWs becomes advantageous.[13,14] Though the famous vapor–liquid–solid (VLS) mechanism[15,16] has been widely explored to produce high-quality SiNWs, serving as beneficial 1D channels to prototype a series of high-performance logics and sensors,[17–19] a key challenge remains as to how to grow orderly and uniform SiNW channels for device integration, where a high uniformity and close-to-unity growth deployment rate (GDR) are necessary. Unfortunately, most VLS-grown SiNWs are obtained as vertical bundles that are difficult to precisely transfer, align, and position on planar surfaces for scalable device fabrication.[20–22] Recently, an in-plane solid–liquid–solid (IPSLS) growth mechanism has been developed in our previous works,[23–26] where indium (In) catalyst droplets are employed to absorb a surface-coating amorphous silicon (a-Si) precursor to produce crystalline SiNWs. Importantly, these IPSLS SiNWs can be guided by single-sided step edges to grow into prescribed locations, with the main fabrication steps as diagramed in Fig. 1(b). While the IPSLS SiNWs can be grown at rather low temperatures, even down to 90 °C by using low-melting-point metal catalysts,[27] a major drawback for the single-sided-step guiding approach is, as depicted in Fig. 1(c), that it direct only the growth direction of SiNWs, with little control over their diameter uniformity and growth stability, making them easy to *derail* upon the surface or edge roughness or imperfection disturbances. However, to serve as reliable c-Si channels for monolithic 3D integration, a new strategy must be established to guarantee a high diameter uniformity, growth

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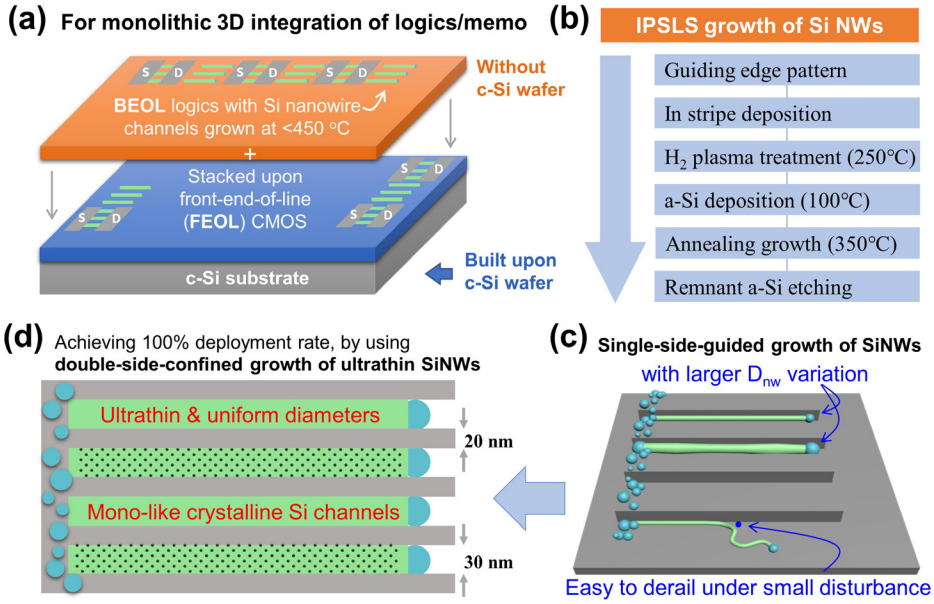


FIG. 1. Schematic diagram of bilaterally confined ultrathin SiNWs for monolithic 3D integration. (a) Schematic illustration of the monolithic 3D integration structure, which has the front-end logics by top-down etching, and other device layers built directly on the first layer. (b) Basic steps of the IPSLS growth mode. (c) Single-sided guided nanowires have poor uniformity due to the uncontrollable size of indium droplets. (d) Quasi-monocrystalline ultrathin nanowires are confined bilaterally by tracks.

stability, and close-to-unity (100%) GDR of these tiny 1D channel building blocks.

In this work, a tightly double-side-confined growth of ultrathin and uniform monocrystalline IPSLS SiNWs has been explored. The high-density guiding grooves were formed directly within a hydrogen silsesquioxane (HSQ) layer and patterned by the electron beam lithography (EBL) technology. In order to achieve 100% GDR, a special converging guiding track has been designed and testified, which can greatly boost the SiNW growth occupation rate in each guiding groove from ~60% to close-to-unity (~100%). All these key capabilities combined could provide a solid basis for the integration of ultrathin and uniform SiNW channels for the implementation of 3D electronics.

In order to impose a double-sided confinement of the IPSLS growth of SiNWs, a dense array of SiO_2 grooves was fabricated upon the SiO_2 (90 nm)/wafer substrate by using EBL with a 25 nm thick HSQ resist layer, spin-coated at a speed of 4000 rpm for 60 s followed by a subsequent soft-baking at 90 °C for 4 min. Under electron beam irradiation, the HSQ was converted to SiO_2, with an optimized acceleration energy, beam current, and dose of 100 keV, 1 nA, and 3100 $\mu C/cm^2$, respectively. The resulted guiding groove tracks, as illustrated and seen in the scanning electron microscope (SEM) image in Fig. 2(a), have a groove width of 20 nm and a wall spacing of 30 nm. Note that these groove dimensions represent roughly the lowest limits that can be reliably repeated by the EBL system used in this work; then, In catalyst stripes of 100 nm wide and 5 nm thick were prepared [see Fig. 2(b)], crossing the ends of the guiding tracks, patterned by using EBL with PMMA resist, and deposited by electron beam evaporation (EBE) via the standard liftoff procedure; after that, the samples were loaded into the PECVD system and treated by the H_2 plasma at 250 °C to remove the surface oxide layer of In stripes, allowing them to diffuse and merge into discrete droplets, prior to coating a thin a-Si precursor layer at 100 °C by using pure silane plasma; finally,

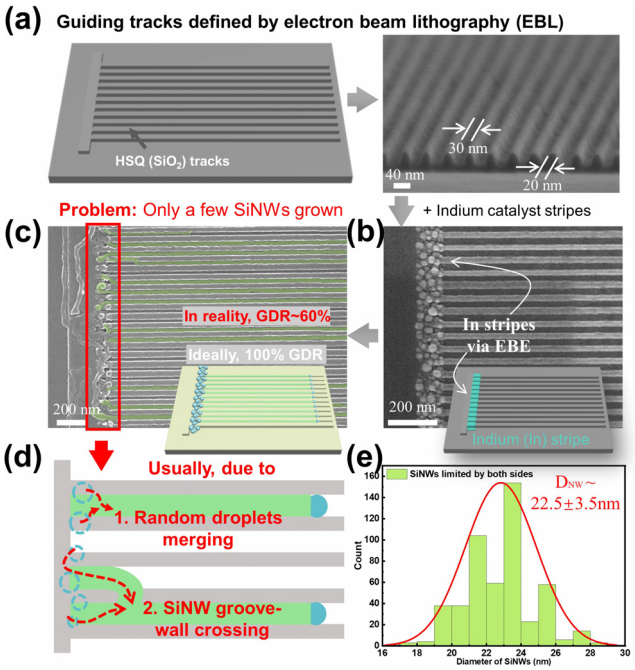


FIG. 2. IPSLS growth dynamics of dense array of SiNWs tightly confined within SiO_2 grooves. (a) In the left panel, the formation of dense HSQ (SiO_2) guiding grooves patterned by EBL, with the corresponding SEM image in the right panel, is schematically depicted; (b) The SEM image of the In catalyst stripe deposited at the end of grooves, as diagramed in the bottom inset; (c) the SiNWs grown directly within the dense array of grooves, with a low SiNWs growth deployment/occupation rate (~60%), due to the random merging of neighbored In droplets and SiNW track-crossing, as schematically depicted in (d). (e) Statistics and Gaussian fitting of more than 500 as-grown SiNWs.

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the substrate temperature was raised to 350 °C to melt the In droplets and activate them to absorb the a-Si layer and produce SiNWs along their moving courses. More details of the IPSLS growth mechanism are available in our previous works.[28–31]

Figure 2(c) presents a typical SEM image of the as-grown SiNWs within dense grooves, where the SiNWs are pseudo-colored to green for easy observation. It is found that there are only 12 SiNWs grown within 20 guiding grooves, corresponding to a 60% GDR, which is far below the desired 100% GDR filling required for a reliable growth integration. Despite a low GDR, the statistics of more than 500 SiNWs, found in the grooves as shown in Fig. 2(e), indicate that the guided growth of SiNWs can be rather stable, with a uniform diameter of $D_{NW} = 22.5 \pm 3.5$ nm. Close scrutiny of the kicking off places along the catalyst stripe reveals that the low growth rate can be assigned to the random crossing and merging of the neighbored In droplets, as depicted schematically in Fig. 2(d), which pose a major threat to achieving a stable 100%-GDR growth integration of ultrathin SiNWs.

In order to guarantee one and only one SiNW grown into each groove, a special converging-guiding-track was designed. As seen in Figs. 3(a)–3(b), a group of slanting but converging guiding step lines were patterned, with widely separated ends (260 nm apart) intersecting with the In stripes at the initial kicking off places, and converging ends joining the narrow open ends of the dense groove tracks. In this way, multiple catalyst droplets could be safely and separately formed within the wider spaces at the *stripe-edge* crossing regions, but all of them have a chance to be captured by the nearby guiding edges and directed to grow toward the joining entrance of the dense groove tracks. Note that only the In droplets that were guided by the step edges can travel over a long enough distance to reach the converging entrance, as witnessed indeed in the SEM view in the middle of Fig. 3(a), while the freely grown ones can travel only to a short distance of <250 nm away from the In stripe boundary. Interestingly, this *converging-feeding* strategy helps to (1) greatly suppress the random merging of the In droplets, as they are now well separated at the wider stripe-edge crossing regions and more importantly (2) ensure that there are usually a pair of SiNWs that will be brought by the converging single-sided edge lines, into the entrance of narrow grooves [see Fig. 3(d)], as an important *redundant mechanism* to guarantee a 100% GDR. Actually, only the first arrival one will grow into the narrow grooves, as the latecomer will find that the local a-Si supply has been consumed by the previous one, which is a critical mechanism to avoid overlapping SiNW growth within the same groove track.

Remarkably, close SEM examinations of the 100%-GDR SiNWs within the dense groove tracks reveal, as shown in the left and right panels Fig. 3(a), that the tightly confined IPSLS growth can be rather stable at least over a long distance >70 μm, even over the turning tracks as seen in Fig. 3(b). More importantly, this tight double-sided confinement improves substantially the uniformity of the SiNWs,

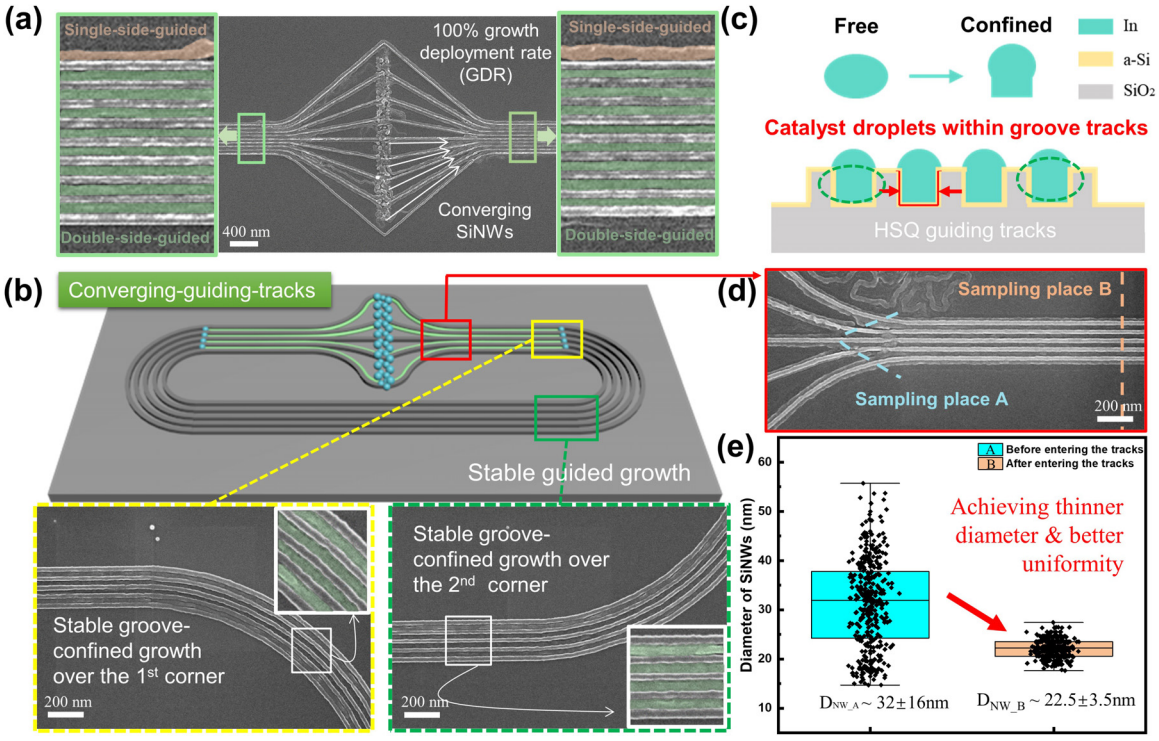


FIG. 3. (a) SEM image of a group of inclining single-sided guiding edges that converge from the wider In-stripe-intersecting center parts toward the entrances of narrower groove tracks, with enlarged close-views provided in the insets on both sides. (b) The layout of a special racetrack converging design that achieve a 100%-GDR stable growth, even over the bending corner places as witnessed in the SEM images of the marked regions. (c) Diagrams show the change in the leading In droplets from free form to confined state within groove tracks. (d) A close scrutiny of the entrance place joining the converging and narrow groove tracks, while the diameter statistics on >350 SiNWs sampled at place A (single-side-guided, cyan) and place B (double-side-guided, orange) are compared in (e).

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compared to those found along single-sided edges. For example, a straightforward comparison of the SiNWs grown within or out of the guiding grooves was obtained from SEM images shown in the left and right panels of Fig. 3(a), where the upmost one (orange) is guided only by the outmost single-sided edge and, thus, features a much larger fluctuation in both diameter and growth position. Statistics of the SiNWs' diameters shown in Fig. 3(e) and the SEM characterization in Fig. 3(d) indicate that, with the same growth conditions, the diameter dispersion of the single-edge-guided SiNWs (cyan-colored) is $D_{nw_A} = 32 \pm 16$ nm, which can be largely reduced to only $D_{nw_B} = 22.5 \pm 3.5$ nm for the SiNWs grew into narrow tracks (orange).

This improved uniformity can be explained based on the regulated a-Si supply for the catalyst droplets when growing within the narrow grooves. As illustrated in Fig. 3(c), when the free spherical In droplets (green) grow into the grooves (gray) coated with the a-Si layer (yellow), they are supposed to be confined by the narrow tracks and deform into a complex shape, with a hemispheric top and a roughly squared bottom. Under this situation, the effective In/a-Si absorption, as indicated by the red lines, is simply the sum of the double sidewall depths and the width of the grooves, which are determined beforehand by design. Even for the droplets with somehow different initial volume, the free top surface is allowed to adjust the height of the upper hemisphere part, which has only a little influence on the touched amount of a-Si supply. This feature is also considered as beneficial to suppress the impact of catalyst droplet size variation, improving the uniformity of as-grown SiNWs.

In order to examine the crystalline structure of the groove-confined SiNWs, the cross-sectional profiles of the SiNWs were exposed by focused ion beam (FIB) milling and then analyzed by high resolution transmission electron microscope (HR-TEM). As shown in Fig. 4(a), a row of seven crystalline SiNWs (light-green) can be found in the HSQ-SiO_2 grooves (gray), with remnant a-Si layer (light-blue) discernable on the top of the groove sidewalls. Note that this specific sample was chosen with the rightmost #8 groove left empty, due to intentional In stripe misalignment, providing an opportunity to preserve the initial *pristine* a-Si layer coating profile within the groove tracks. Comparing the unoccupied and occupied grooves (#1–#7 SiNWs), it is found that the confined SiNWs growth did not consume all the a-Si layer, particularly for that deposited on the top of sidewalls. According to the caved/or absorbed profile of the remnant a-Si layer, the gesture of the In droplets can be roughly constructed, as delineated by the dashed line at the locations of #1 and #4 in Fig. 4(a). All these observations indicate that the groove-confined In droplets can presume an ecliptic shape and consume mostly the a-Si supply coated on the vertical sidewalls and the bottom surface, instead of spreading over to absorb the a-Si layer coated the top of sidewalls, which is important to prevent droplet merging/crossing.

Interestingly, most of the as-grown SiNWs were found fitting well to the bottom of grooves, with an ecliptic shape of $W_{nw} = 23 \pm 3$ nm wide and $H_{nw} = 18 \pm 4$ nm thick, according to the statistics in Fig. 4(c). HR-TEM examinations of the #1 and the #4 SiNWs in Fig. 4(b) reveal that the SiNWs are monocrystalline and grown in the Si⟨100⟩ crystallographic orientation, despite the somehow different aspect ratio. In addition, an aberration-corrected HR-TEM imaging of another SiNW grown within similar grooves is presented in Fig. 4(d), which provides a clearer view of the coherent monocrystalline lattice

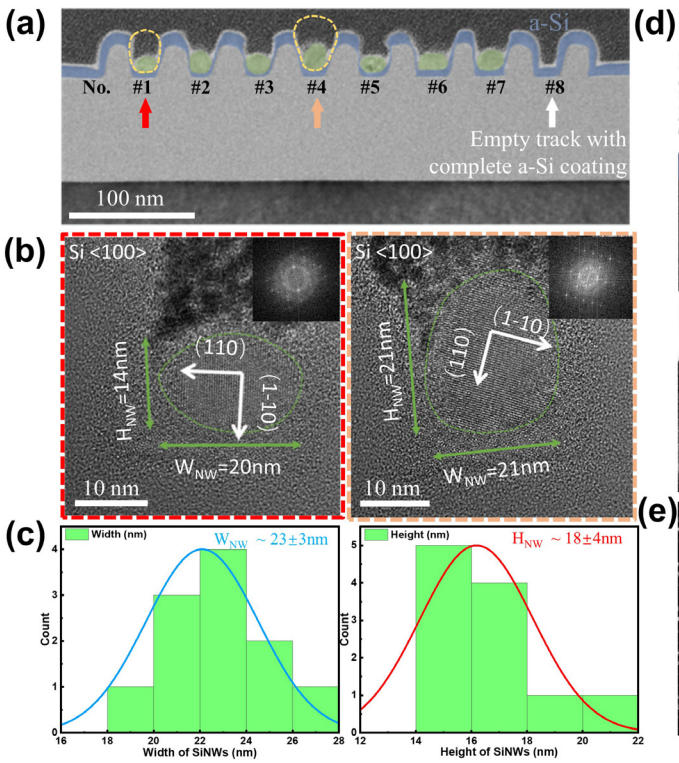


FIG. 4. Structural analysis of the groove-confined ultrathin SiNWs. (a) The cross-sectional TEM image of an array of SiNWs within the groove tracks, where the residual a-Si and SiNWs are tinted to blue and light-green, respectively. (b) The enlarged HR-TEM image of the lattice fringes of the #1 and #4 SiNWs labeled in (a), which have a growth orientation of Si⟨100⟩ inferred from the corresponding electron diffraction patterns presented in the top-right insets. Statistics of the width and height of the SiNWs are extracted and plotted in (c), while (d) and (e) showcase an aberration-corrected HR-TEM analysis and high-resolution lattice imaging of another SiNW grown in the Si⟨100⟩ crystallographic direction.

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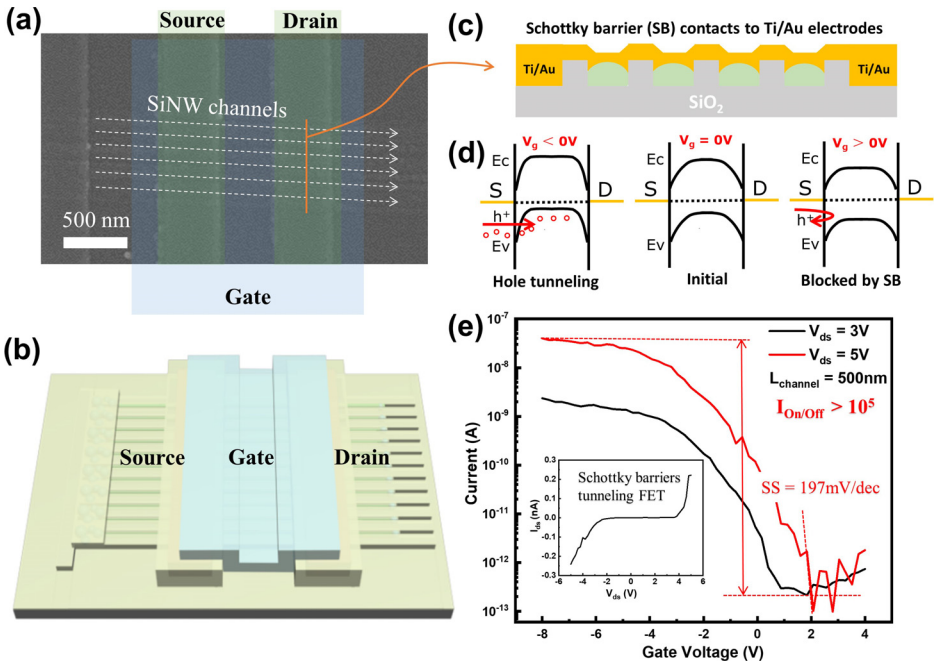


FIG. 5. Electronic transport properties of the SiNW Schottky barrier tunneling (SBT)-FET. (a) SEM image of the device with an array of six SiNWs as channels, with corresponding schematic diagram shown in (b); (c) the local configuration of the S/D metal contacts (yellow) to p-type SiNW arrays (light green), forming typical Schottky barriers to the S/D electrodes. (d) Three band alignment situations of the SiNW channels with different gating biases, where only under large negative gating voltage, the hole carriers can tunnel through the thinned SB to turn on the transport current, as observed indeed in (e) the transfer properties of the SBT-FET device with a channel length of 500 nm, while the inset showing a typical I_{ds}–V_{ds} characteristic of the SB-contacted SiNW FET device.

of Si atoms, with an electron diffraction pattern provided in the inset of Fig. 4(e). Note that though a preferential growth orientation along Si⟨100⟩ seems to be identified among the SiNWs grown in grooves, it remains still an open question, largely due to the lack of sufficient data, as to how this has been established during the guided growth and how it will switch at the turning bends.

To testify quickly the electronic transport property of the ultrathin SiNWs channels, a simple junctionless FET device was fabricated, without removing the surrounding SiO_2 grooves, where the remnant a-Si layers were selectively etched off by reactive ion etching (RIE), followed by an annealing at 850 °C in dry O_2 for 1 min to form a thin SiO_2 layer of ∼2 nm thick. Then, a pair of composite Ti (5 nm)/Au (45 nm) source/drain (S/D) electrodes were defined by EBL and deposited by EBE. After that, an Al_2O_3 dielectric layer (30 nm) was deposited at 300 °C by atomic layer deposition (ALD), followed by patterning and depositing 60 nm thick Al as the top gate electrode. Figures 5(a) and 5(b) show the SEM images and schematic diagram of the as-fabricated device, while the typical transfer properties are shown in Fig. 5(e), with an $I_{on/off}$ ratio $> 10^5$ and sub-threshold swing $= 197\ \text{mV dec}^{-1}$.

According to the output I_{ds}–V_{ds} curve in the inset of Fig. 5(e), the p-type SiNWs channels form typical Schottky barrier (SB) contacts to S/D electrodes, with a local SB contact band profile as depicted schematically in Fig. 5(d). Note that the p-type doping in the as-grown SiNWs arises from the incorporation of In atoms into the c-SiNWs, with an equivalent Boron-doping of $\sim 10^{18}/\text{cm}^3$ as verified in our previous works.[32,33] Hence, under $V_{gs} = 0$ V or positive gating bias, a pair of back-to-back connected SBs blocks the current transport through the SiNWs channels, while under a negative gating bias, the band profile of the SiNW channel is uplifted, causing a quick thinning of the SB width that allows the hole carriers to easily tunnel through the triangle SBs, thus turning on the transport current.

It is noteworthy that the relatively high SB contact resistances at the S/D electrodes pose always a limit for achieving a high drive current. Thus, the full potential of the SiNW-FET has yet to be verified within a more advanced gating-all-around (GAA) configuration,[34,35] implanted and heavily doped S/D contacts,[36,37] as well as more carefully controlled high-k dielectric layers and work function-matched metal gating electrodes.[38,39] Nevertheless, these prototype SB-tunneling FET devices represent at least a primitive experimental verification of the potential of such groove-confined high-density, uniform and ultrathin SiNWs, as advantageous 1D channels, for future monolithic 3D integration of more advanced logics and memory functionalities directly upon amorphous dielectric medium, without the need of preexisting monocrystalline c-Si wafer as substrate. Also, these results solicit more systematic and collaborative efforts to develop more specific fabrication technologies, dedicated to the GAA-channel release, passivation and contact formations of these catalytically grown and integrated SiNW channels.

In summary, a low-temperature catalytic growth integration of ultra-dense and thin SiNW array has been demonstrated, with a uniform width of $W_{NW} = 22.5 \pm 3.5$ nm, NW-to-NW spacing of 25 nm, and a close-to-unity 100% growth deployment rate (GDR), thanks to a tight double-side-confined growth with a converging-guiding-track design. This has enabled a reliable and scalable fabrication and integration of orderly array of monocrystalline ultrathin SiNW channels, with unified Si⟨100⟩ growth orientation directly upon dielectric layers, without the preexisting c-Si wafer as a substrate. Prototype Schottky barrier tunneling SiNW-FETs are successfully demonstrated with a $I_{on/off}$ ratio and sub-threshold swing of $>10^5$ and 197 mV dec^{-1}, respectively. These results indicate a reliable growth integration of ultrathin monocrystalline SiNW channels that could be particularly suited for the implementation of more advanced monolithic 3D integration paradigm.

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AUTHOR DECLARATIONS

Conflict of Interest

The authors have no conflicts to disclose.

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The authors have no conflicts to disclose.

Author Contributions

Wentao Qian: Conceptualization (equal); Data curation (lead); Formal analysis (equal); Investigation (equal); Methodology (equal); Validation (lead); Visualization (lead); Writing – original draft (lead). **Yifei Liang:** Formal analysis (supporting); Investigation (supporting); Methodology (supporting). **Junzhuan Wang:** Data curation (supporting); Funding acquisition (equal); Investigation (equal); Project administration (supporting); Writing – review & editing (supporting). **Zongguang Liu:** Data curation (supporting); Investigation (supporting); Resources (supporting). **Jun Xu:** Funding acquisition (supporting); Resources (supporting); Writing – review & editing (supporting). **Linwei Yu:** Conceptualization (lead); Data curation (equal); Formal analysis (equal); Funding acquisition (lead); Investigation (lead); Methodology (equal); Project administration (lead); Resources (lead); Supervision (equal); Validation (equal); Visualization (equal); Writing – original draft (equal); Writing – review & editing (lead).

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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