Journal of Alloys and Compounds 1001 (2024) 175189

Contents lists available at ScienceDirect

Journal of Alloys and Compounds

journal homepage: www.elsevier.com/locate/jalcom

Performance improvement of planar silicon nanowire field effect transistors via catalyst atom doping control

Lei Liang [a], Lei Wu [a], Wei Liao [a], Wentao Qian [a], Ying Zhang [a], Ruijin Hu [b,*], Junzhuan Wang [a,*], Linwei Yu [a,*]

[a] School of Electronic Science and Engineering, National Laboratory of Solid-State Microstructures, Nanjing University, Nanjing, PR China
[b] School of Physical Science and Technology, Microelectronics Industry Research Institute, Yangzhou University, Yangzhou 225002, PR China

ARTICLE INFO

Keywords:
Silicon nanowires
Catalytic growth
Dopant control
FET

ABSTRACT

Catalytic growth of silicon nanowires (SiNWs), mediated by metallic droplet, provide ideal quasi-1D channels to construct high performance field effect transistor (FET). However, the incorporation of catalytic metal atoms into SiNWs channels has significant impact on the FET characteristics, and thus needs to be better understood and controlled to fulfil its potential for high performance electronics. In this work, we focus on the effect of the incorporation of indium (In) catalytic atoms into planar SiNWs, grown via an in-plane solid-liquid-solid (IPSLS) mechanism, on the FET device performance. It is found that the initial high concentration of p-type In dopants in the as-grown SiNWs led to an equivalent boron (B) doping of 5×10^{18} cm^{-3}. However, a simple step-wise annealing in oxygen at different temperatures, varied from 620 °C to 920 °C, can help to out-diffuse the dissolved In atoms into the surface SiO_2 layer, and reduce the In concentrations down to $<5\times10^{17}$ cm^{-3}, as verified by atom-probe tomography (APT) and four-point-probe measurements. This effective dopant control enables a remarkable device performance improvement of the Schottky barrier FETs, built upon an orderly array of parallel SiNWs of approximately 25 nm in diameter, where the current ratio (I_{on}/I_{off}) has been substantially boosted from 10^5 to 10^8, while the subthreshold swing (SS) reduced from 400 mV/dec down to ~100 mV/dec, with a hole carrier mobility increased from 10 to ~75 cm^2 V^{-1} s^{-1} as extracted according to a finite element analysis. These results pave the way for the employment of the catalytic IPSLS SiNWs to serve as high quality 1D channels for high-performance SiNWs-based electronics and sensors.

1. Introduction

Low temperature catalytic growth of Si-based materials provides a rather convenient, high yield and diverse fabrication approach to explore a wide range of nanoscale electronics and devices [1–7], where quasi-one-dimensional (1D) silicon nanowires (SiNWs), led by metal droplets, have attracted particular research interests for the construction of high performance nanoelectronics and sensors, where the ultrathin SiNWs serve as ideal 1D channels to achieve excellent electrostatic gating or sensing effects [8–13]. For example, the famous vapor-liquid-solid (VLS) mechanism has been widely explored to produce various high-crystallinity vertical SiNWs, upon which high performance field effect transistors (FETs), memory, and logics have been built successfully [13–22]. Various metal catalysts such as Al, Sn, Bi, Ga, Pb, and Au have been used to prepare SiNWs via the VLS methods, the choice of metal has profound effects on the morphology and electrical properties of the SiNWs, such as doping type and electrical resistivity [21]. For planar electronic device fabrication, the VLS-grown vertical SiNWs usually need to be picked and transferred onto planar substrate, which by itself is a technical challenge for achieving scalable device integration. In order to grow orderly SiNW channels on planar substrate, a relatively new in-plane solid-liquid-solid (IPSLS) growth mode has been established in our previous works [23–25], where a-Si thin film (instead of the gaseous silane as in VLS growth) is fed as precursor layer and consumed by indium (In) catalyst droplets to produce c-SiNWs. The IPSLS growth enables a deterministic guiding growth control of the planar SiNWs, following the pre-defined step edge routines [26].

However, similar to all the catalytic grown SiNWs [13,17], the metal atoms will dissolve into the SiNW channels during the growth. During the IPSLS growth, it has been known that a high concentration of In atoms will be incorporated into SiNWs, close to 10^{19} cm^{-3} which is much higher than the equilibrium solubility of In atoms in c-Si, due to a

* Corresponding authors.
E-mail addresses: huruijin@yzu.edu.cn (R. Hu), wangjz@nju.edu.cn (J. Wang), yulinwei@nju.edu.cn (L. Yu).

https://doi.org/10.1016/j.jallcom.2024.175189
Received 29 April 2024; Received in revised form 2 June 2024; Accepted 13 June 2024
Available online 13 June 2024
0925-8388/© 2024 Elsevier B.V. All rights are reserved, including those for text and data mining, AI training, and similar technologies.

colossal injection kinetic process [27]. This thus gives rise to efficient p-type doping in the as-grown SiNW channels, as the In dopant causes an energy level 0.16 eV above the valence band top (VBT) [28]. In order to fabricate high performance SiNW FETs, this catalytic atom doping has to be reduced to an efficient doping level$<10^{17}$ cm^{-3}. Though the IPSLS SiNWs have been explored to demonstrate reasonable FETs in a convenient junctionless configuration with Schottky tunneling barrier (STB) contacts at the metal/SiNW interfaces, a more comprehensive understanding of the doping control of the In-catalyzed SiNWs, and its potential for high performance device, is definitively needed.

In this work, we carried out a systematic parametric investigation of the device performance improvement of the SiNW-FETs, mainly by a series of post-growth annealing method that promotes out-diffusion of In atoms from the SiNW core and segregates into the surface SiO_2 layers [29–33]. This thus provides a convenient and effective means to control/reduce the In dopant density in the catalytic SiNW channels, as depicted schematically in Fig. 1**(a)-(b).** It was found that the effective doping effect of In dopants can be greatly reduced from an equivalent B (boron) concentration of 5×10^{18} cm^{-3} down to $\sim10^{16}$ cm^{-3}, as verified by atomic probe tomography (APT) and four-point probe measurements, accompanied with a significant device performance improvement, in terms of higher current ratio, sharper subthreshold swing (SS) and higher hole mobility. These results provide a solid basis for the massive integration of catalytic-grown SiNW arrays to fabricate high performance transistors.

2. Experimental procedure

2.1. Process of SiNWs growth

The planar SiNWs arrays were fabricated upon Si wafer substrate coated with an oxide layer of 500 nm thick, via an IPSLS growth approach, along pre-patterned guiding edge lines by using photolithography[34]. In order to increase the lateral density of the parallel SiNW channels, a special guiding terrace structure with multiple mini-steps (as depicted in Fig. 1**(c)** was first formed at each edge line via a multi-cycles alternating inductive coupled plasma (ICP) etching-passivation technology, as explained with more details in the Experimental procedure section and our previous works [34,35]. After that, narrow stripes of In catalyst were deposited and patterned at the starting position of the guiding terraces, as seen for example in the scanning electron microscopy (SEM) image and marked by the orange dashed rectangle in Fig. 1**(d)**. Then, the samples were loaded into a plasma enhanced chemical vapor deposition (PECVD) system and treated by H_2 plasma at 250 °C. During this course, the oxide layer of the In stripes was reduced, which allowed the diffusion and merging of In atoms to form discrete In nano-droplets.

In the next step, a thin film of amorphous silicon (a-Si) was deposited to cover the whole surface by using silane plasma at a lower temperature of 100 °C, followed by a growth annealing at 350 °C for around 1 h in vacuum. Planar SiNWs were produced by the leading molten In droplets during their movement along the mini-steps of the guiding terraces, by consuming the a-Si precursor films to precipitate crystalline SiNWs [25,36]. At the end of the growth, the remnant a-Si precursor films were selectively removed through a low temperature reaction ion etching (RIE) at 25 °C, while the residual In catalyst can be cleaned by HCl

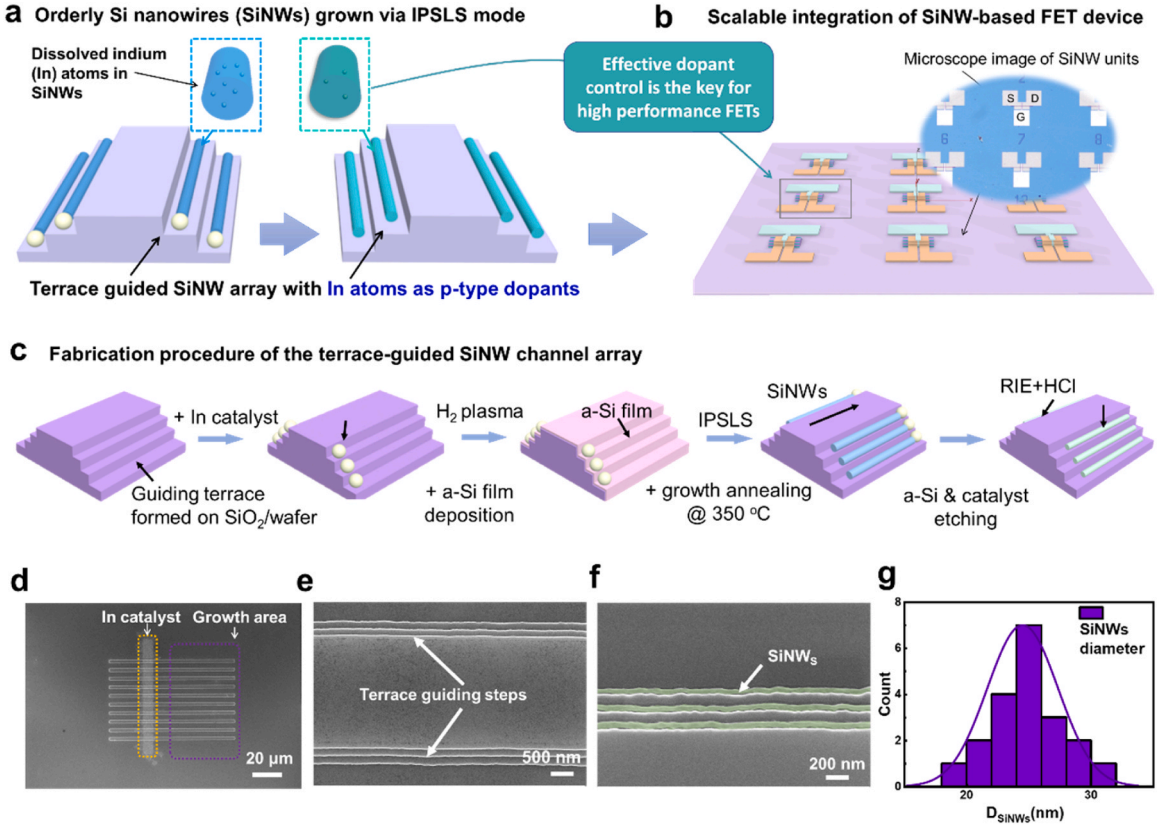


Fig. 1. High density terrace-confined SiNWs arrays grown via IPSLS mechanism. **(a)** Terrace-guided high-density SiNWs with effective In dopants control. **(b)** The idea terrace guided SiNWs channels arrays for scale integration of high-performance SiNWs-FETs devices. **(c)** Schematic illustration of the synthetic process for high density terrace-guided SiNWs. **(d)-(f)** Typical SEM images of In catalyst and SiNWs growth region, empty terrace steps, and as-grown high density SiNWs. **(g)** Diameter statistics of the SiNWs.

solvents. More details about SiNWs growth and devices fabrication process can be obtained in the Supporting Information *file* **Method** part.

2.2. Structural and elements analysis of SiNWs

Via a proper growth parameter control including the H_2 plasma treatment temperature, duration, and pressure, as well as the thicknesses of the In stripes and a-Si film, a high-density growth of parallel ultrathin SiNWs, with a close to 100 % guiding rate, can be achieved along the terrace edges, as witnessed in the SEM images shown in Fig. 1 **(e)**-**(f)** for the terrace region before and after the IPSLS growth of SiNWs, respectively (SiNWs more details in the enlarged FESEM image in Fig. S1). For the SiNWs taken as FET channels in this work, the SiNW diameter is $D_{nw} = 25 \pm 5nm$, according to the statistics shown in Fig. 1 **(g)**, with a lateral NW-to-NW spacing of 150 nm.

In addition, the lattice quality and element distributions were also examined by high-resolution transmission electron microscopy (HR-TEM). As shown in Fig. 2**(a)-(b)**, the HR-TEM analysis reveals a monocrystalline cross-section of the as-grown SiNW measured with 22 nm and 12 nm in width and height, respectively. According to the fast Fourier transform pattern, this specific SiNW was grown in Si<110> crystallographic orientation, with a clear lattice fringe spacing of d=3.14 Å, corresponding to the Si (111) planes. Furthermore, the energy dispersive X-ray spectroscopy (EDS) analysis in Fig. 2**(c)** indicates indeed the existence of dissolved In element in the as-grown SiNW, but only in a trace amount.

3. Results and discussions

3.1. Doping concentrations analysis

In our previous works[27], the concentration of the dissolved In atoms in SiNWs was found to be ~10^{19} at. cm^{-3}. Compared to the B dopants that cause a shallow acceptor level in c-Si that lies E_A^B ~0.04 eV above the valence band top, the In dopants are known to introduce a deeper acceptor level with an activation energy E_A^{In}~0.16 eV. As the Fermi level E_F is determined by the following equation [28]

$$p = N_V \exp\left(\frac{E_V - E_F}{kT}\right) = \frac{N_A}{1 + g_A \exp\left(\frac{E_A - E_F}{kT}\right)} \quad (1)$$

where the N_A/N_A is the dissolved/ionized acceptor dopant concentration, g_A is the ground state degeneracy, E_A is the acceptor energy level, k is the Boltzmann constant, N_v is the effective state density and E_v is the valence band top, the In dopants in the c-SiNW will not be fully ionized considering $E_A^{In} > kT = 0.026eV$. Therefore, according to the plots of numerically solved Fermi level positions in Fig. 2**(d)**, for the In and B dopants, the incorporation of 1×10^{19} cm^{-3} In atoms in c-Si will give rise to a p-type doping effect equivalent to that of ~2×10^{18} cm^{-3} B atoms, which are supposed to be fully ionized at room temperature. To verify this point, the resistivity of the as-grown SiNWs was measured in a four-point probe configuration, as seen in Fig. 2**(e)**, where the equidistant electrodes were patterned on a single SiNW by electron beam lithography (EBL) technology. For a single as-grown SiNW, the measured electrical resistivity (ρ) was extracted to be ~0.1 Ω cm, as seen in the left panel in Fig. 2**(f)** and Fig. S2**(a)-(b)**, which is comparable to the doping effect of 5×10^{18} cm^{-3} B dopants in c-Si according to Reference [27,28].

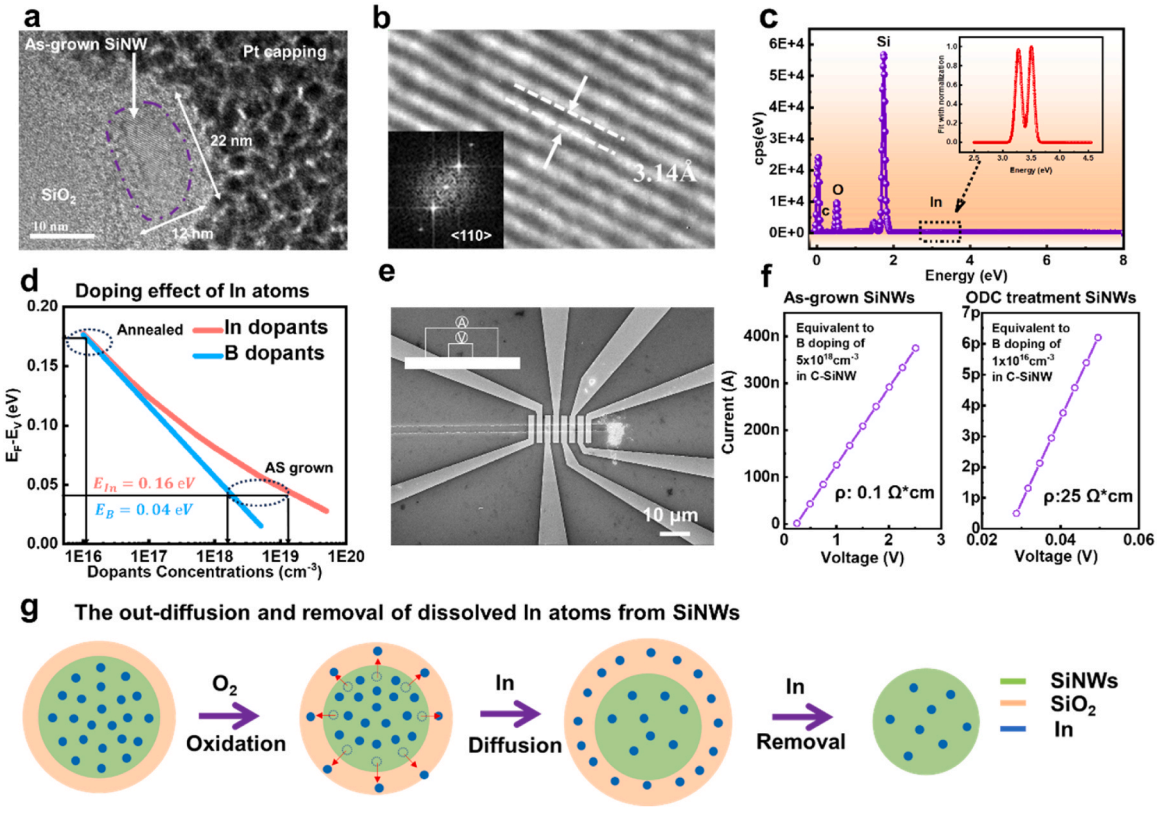


Fig. 2. Structural and compositional analysis of the SiNWs. **(a)** Typical TEM image of SiNW, where the purple dash line delineates the profile. (**b**) Partial enlarged detail of TEM image with lattice diffraction pattern as inset. (**c**) Distribution diagram of element EDX spectra. **(d)** The calculated Fermi level position as a function of the doping concentration of indium (red) and boron (blue). **(e)** Schematic diagram and SEM image of the four-point probes measurement. (**f**) Four-point probe measurements I−V characteristics for the as-grown and annealed SiNWs. (**g**) Schematic diagram of the typical processes for In atoms out-diffusion from SiNWs.

This finding indicates that there has been a large amount of In atom dopants dissolved into the as-grown SiNWs, resulting in a high concentration of hole carriers that could screen and degrade the gating effect of the top gate electrode.

3.2. In catalytic atoms out-diffusion

Fortunately, it has been known in the literature[30] that the In atoms feature a exponentially decreasing Si/SiO_2 segregation coefficient with the increase of annealing temperature,

$$m(T) = \frac{C_{Si}}{C_{ox}} = m_0 \exp(-E_m/K_B T) \quad (2)$$

where C_{ox} (C_{Si}) is the equilibrium dopant concentration in the SiO_2 (Si) medium, and an activation energy of E_m=2.55 eV. This indicates that In atoms will tend to diffuse out from the c-Si into the surrounding SiO_2 medium at temperature T>720 °C (m<1), which is in strong contrast to the Si/SiO_2 segregation of B atoms that favor diffusion from oxide medium into c-Si at elevated temperature [32].

Based on this assumption, a special oxidation-diffusion-cleaning (ODC) strategy has been designed to reduce the In concentrations in the planar SiNW, as depicted in Fig. 2**(g)** and Fig. 3**(a)**. Specifically, the as-grown SiNWs will be annealed in oxygen ambient, at varied temperatures ranging from 720 °C to 920 °C, to allow the In atoms to segregate from the c-SiNW cores into the oxide shells (that can be later etched off by DHF). On the other hand, it is noteworthy that the out-diffusion of In atoms from the SiNW core is also a thermal activated process. Fig. 3**(b)** plots the quick increase of the diffusion coefficient D_{In} of In atoms at higher temperature, with $D_{In} = D_0 \exp(-E_d/kT)$, D_0 is a pre-factor constant of 1.443 cm^2/s and E_d=3.56 eV the diffusion barrier according to Ref [33]. Ideally, the annealing duration t_{ann} should be long enough for

$$L_{In} = \sqrt{D_{In} t_{ann}} > D_{nw}. \quad (3)$$

Hence, for the SiNWs grown in this work with a diameter of 25 nm, a suitable oxidation-diffusion time of T=650 s at 920 °C should be long enough to out-diffuse most of the In atoms from the SiNWs, as marked in Fig. 3**(c)**.

As a quick check of the effect of the ODC treatment, Fig. 2**(f)** and Fig. S2**(c)-(d)** show the four-point-probe I-V curve of the annealed SiNW at 920 °C for 10 min, where the extracted resistivity increases to 25 Ω cm that is equivalent to the p-type doping effect of ~10^{16} cm^{-3} B atoms. Note that, as indicated in Fig. 2**(d)**, with this low dopant concentration, both the In and B dopants will be fully ionized, thus giving off the same doping effect in c-Si. To verify the In concentrations in the annealed SiNW, a thicker SiNW segment of 120 nm width and annealed at 920 °C for 10 min was transferred and mounted (Fig. 3**(d)**), via a procedure as depicted in Fig. S3 upon the tip of a tungsten probe for atom probe tomography (APT) analysis. Surprisingly, the APT analysis of the annealed SiNW terminal (see Fig. 3**(d)**) detects only Si atoms (grey) ~39 % and O atoms (blue) ~61 % as witnessed in Fig. 3**(e)-(g)**. Considering the elemental detection limit of the APT device of 10 ppm, the remnant In atoms concentrations in the 920 °C-annealed SiNW should be lower than <5×10^{17} cm^{-3}, which is consistent with the estimated value from four-point-probe measurement.

3.3. Electrical characteristics of the SiNW-FETs

Prototype Schottky barrier FETs were also fabricated upon the SiNW channels, treated by ODC procedures at different annealing temperatures of 620/720/820/920 °C, with a direct Source/Drain (S/D) metal contacts of composite 5/55 nm Pt/Au, via a device fabrication process as described in Fig. 4**(a)**. Then, the SiNW channels were coated with a 20 nm-thick dielectric Al_2O_3 layer by using atomic layer deposition (ALD) process, followed by the fabrication of a 45 nm Al top gate by lithography, electron beam sputtering, and standard lift-off procedure. Finally, an Ω-shaped gating configuration has been realized upon the SiNW channels, as illustrated in Fig. 4**(b)**. In principle, because of the formation of a pair of back-to-back Schottky barrier contacts at the S/D electrodes (see Fig. 4**(c)**), the hole transport through the SiNW channels will be blocked by the triangle barriers under zero or positive gating bias. But when a negative gating bias is applied, the band profile in the whole SiNW channel will be pulled up, and the Schottky barriers will be thinned quickly to become transparent for the holes to tunnel through, which leads to turning on the current transport of SiNW-FETs.

Though this Schottky S/D contact and tunneling transport scenario is applicable to all these SiNW-FETs, there are still significant differences in the transfer properties of the devices treated at different

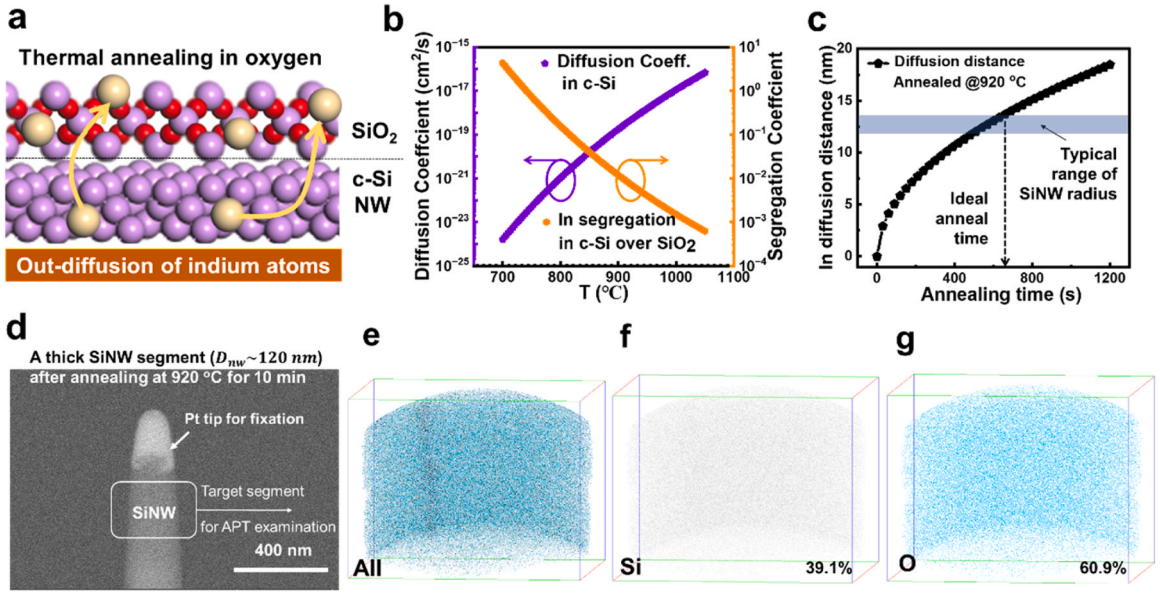


Fig. 3. Reduction of In dopants concentrations for annealed SiNWs. **(a)** The segregation of dissolved In atoms into the surface SiO_2 layer by thermal annealing in oxygen. **(b)** In Diffusion and segregation coefficient as a function of temperature. **(c)** In diffusion distance dependence on the annealing time. **(d)** Typical SEM image of the annealed SiNW tip, with corresponding Si and O atomic distribution mapping extracted in **(e)**, **(f)** and **(g)** respectively.

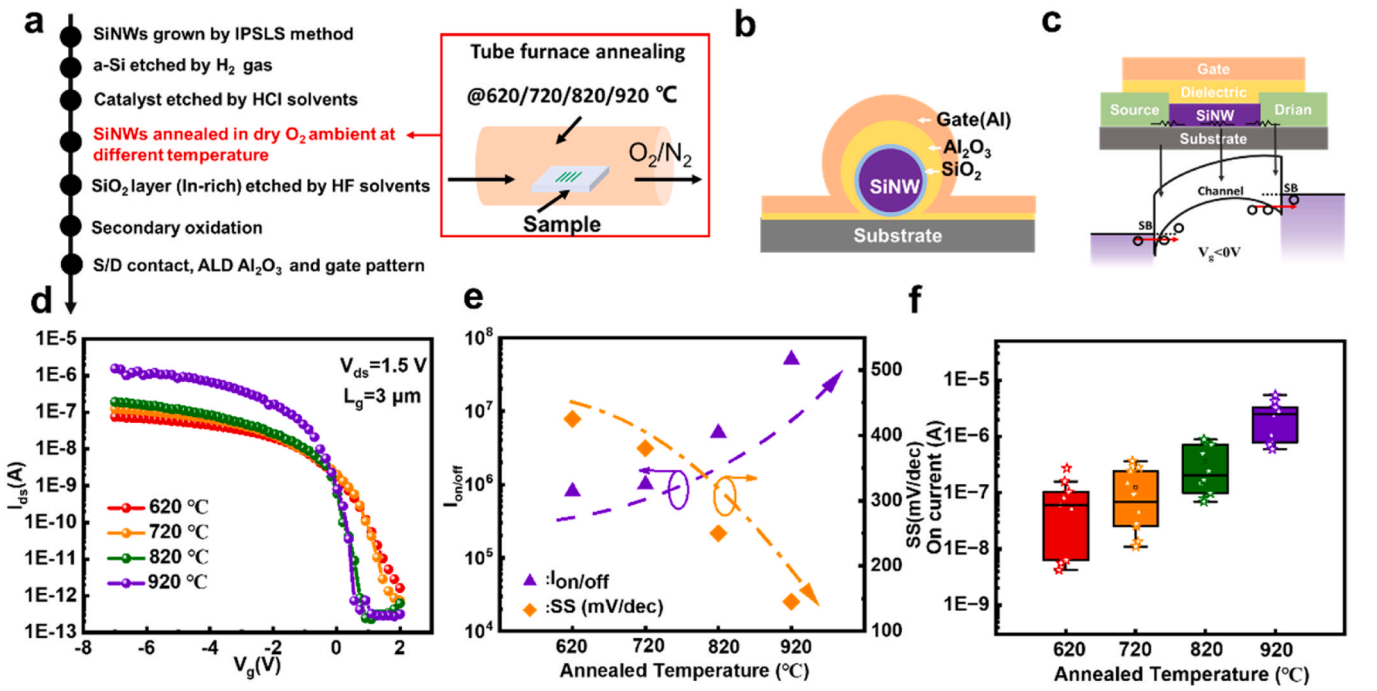


Fig. 4. Electrical properties of devices based on annealed SiNWs at different temperatures. **(a)** Fabrication processes of SiNW-FETs and schematic illustration of annealed ambient. **(b)-(c)** Profile structure and working mechanism of the SiNWs-FETs. **(d)** Transfer characteristics of devices based on annealed SiNWs at different temperatures. **(e)** SS and $I_{on/off}$ extracted from the transfer curves. **(f)** Statistics of the saturation current I_{on}.

temperatures, as observed in Fig. 4**(d)-(f)** and Fig. S4. For example, under the same channel bias of V_{ds}=1.5 V, the on/off current ratio increases gradually from 10^5 to $10^7$with the increase of annealing temperature, while the extracted SS values drop from >400 mV/dec down to <150 mV/dec, as summarized in Fig. 4**(e).** Actually, while the off-state current remains basically the same at <0.3 pA, the on-state

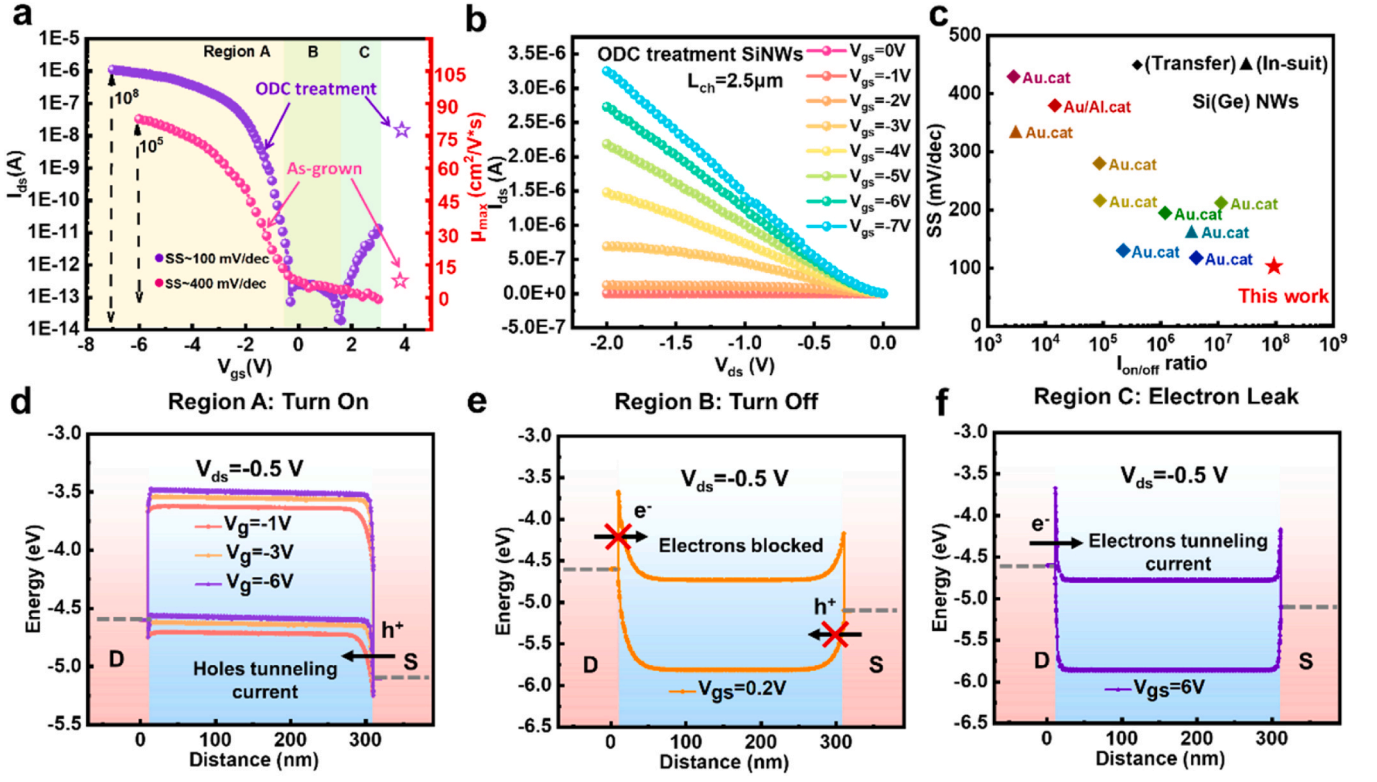


Fig. 5. Device performance analysis and simulation of SiNW-FETs. **(a)** Comparison of the transfer curves of FETs built on as-grown and annealed SiNW channels, with the corresponding extracted mobilities. **(b)** Output characteristics of the annealed SiNW-FETs. **(c)** A summary of the SS and $I_{on/off}$ ratio performance of the FETs based on catalytic Si/or Ge NW channels in the literature and in this work. **(d)-(f)** Band gap profiles of SiNW-FETs under different gating biases with a constant V_{ds}=-0.5 V, corresponding to the different transfer behavior regions as marked in **(a)**.

current is found to enhance strongly after the ODC treatment at higher temperatures, by more than 3 orders of magnitude (see Fig. 4**(f)**).

3.4. Mobility and band alignment profiles

Compared to the device built upon the as-grown SiNWs, with $I_{on/off}$~10^5, SS~400 mV/dec, the FET constructed on SiNWs annealed at 920 °C can achieve a much higher on/off ratio approaching to 10^8, and a steeper SS of 100 mV/dec, as witnessed in Fig. 5**(a)-(b)**. The hole mobility (μ_h) was extracted according to the formula of

$$\mu = \frac{g_m L_{ch}^2}{C_{gc} V_{ds}^*} \quad (4)$$

where g_m is the transconductance ($g_m = dI/dV_g$), L_{ch} the channel length, C_{gc} the gate-to-channel capacitance and V_{ds}^* the actual bias applied on the SiNW channel. It should be noted that, due to the existence of a pair of back-to-back STB at the S/D electrodes on the SiNW, only a small portion of the source-drain bias ($V_{ds} > V_{ds}^*$) is applied on the channel to drive the drifting of hole carriers [37]. So, in order to extract the actual hole mobility, the effective V_{ds}^* has to be obtained with the assistance of a finite element analysis, as seen in Fig. S5, and found to be around $V_{ds}^*/V_{ds} \sim 0.4$. Thus, the hole mobility can be estimated to be μ_h~75 $cm^2/V{\cdot}s$ for the SiNW treated by ODC at 920 °C, which is much larger than that of the 10 $cm^2/V{\cdot}s$ extracted from the as-grown SiNWs, indicating that the hole mobility in the SiNWs can indeed be substantially improved via the ODC treatment.

Furthermore, the working mechanism of STB FET can be better understood with the simulated band alignment profiles, calculated for a shorter channel of 300 nm (for simplicity) under different gate biases, by using Silvaco TCAD 3D device simulator (Synopsys, Inc.), as shown in Fig. 5**(d)-(f)**. For example, under a constant channel bias of V_{ds}=0.5 V, the transport of hole carriers through the SB/SiNW/SB channel can be quickly turned on under large negative gate biases, mainly by direct tunneling and thermal emission through the thinned SB region (Fig. 5**(d)**), corresponding to the Region A in Fig. 5**(a)** [38,39]. For the OFF state under small positive gating (see Fig. 5**(e)**), both the holes and electrons are blocked by the relatively thick and high barriers, that prohibit the transport current. Note that, for even larger positive gating to V_{gs}>2 V, the SB for electrons becomes thinner and thinner, thus leading to the rapid rise of electron tunneling current in Region C. However, this electron leak current was not observed for the FET with as-grown SiNW channels, probably due to the pinning of Fermi level in these un-treated SiNWs that prevents significant downward bending of the band profile even under large positive gate voltages.

In comparison to the other catalytically synthesized Si or GeNW-based FETs, as summarized in Fig. 5**(c)** and Table S1, the SiNW-FETs demonstrated in this work achieve superior device performances, in terms of the $I_{on/off}$ and SS parameters, compared to the FETs fabricated upon VLS-grown SiNWs [37,40–48]. Nevertheless, achieving an Ohmic contact at the S/D electrodes are still desirable and necessary, in our future works, to reduce the contact resistance and boost the On current further. One possible approach is to adopt ion-implantation at the S/D segments to form heavily doped contacts, as already demonstrated in Ref [49,50].

4. Conclusion

In summary, a simple but rather efficient oxidation-diffusion-cleaning (ODC) strategy has been investigated in this work to control the In atom doping concentration in the catalytic SiNWs, grown via IPSLS mode with In catalyst droplets. It was shown that the enhanced segregation of dissolved In atoms at the Si/SiO_2 interface allows for the extraction of In atoms from the SiNW cores into the outer SiO_2 shell at elevated temperature, which has a significant impact on the device performance as verified via a series of compositional and electric characterization/analysis. Finally, by reducing the In doping effect to ~10^{16} cm^{-3}, high performance SiNW-FETs were demonstrated with a high $I_{on/off}$ ratio >10^8, SS~100 mV/dec, and an extracted hole mobility~75 $cm^2/V{\cdot}s$. These findings indicate that the ODC-treated catalytic SiNWs have a potential to serve as high quality semiconducting 1D channels for future SiNW-based logic and sensor applications.

CRediT authorship contribution statement

Junzhuan Wang: Writing – review & editing, Writing – original draft, Supervision, Methodology, Funding acquisition, Formal analysis, Data curation, Conceptualization. **LinWei Yu:** Writing – review & editing, Writing – original draft, Supervision, Funding acquisition, Formal analysis, Data curation, Conceptualization. **Lei Liang:** Writing – review & editing, Writing – original draft, Supervision, Methodology, Formal analysis, Data curation, Conceptualization. **Lei Wu:** Methodology, Formal analysis, Data curation. **Ying Zhang:** Methodology, Formal analysis, Data curation. **Ruijin Hu:** Writing – review & editing, Writing – original draft, Supervision, Methodology, Funding acquisition, Formal analysis, Data curation, Conceptualization. **Wei Liao:** Methodology, Formal analysis, Data curation. **Wentao Qian:** Methodology, Formal analysis, Data curation.

Declaration of Competing Interest

The authors declare the following financial interests/personal relationships which may be considered as potential competing interests: Linwei Yu reports financial support was provided by Nanjing University. If there are other authors, they declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Data Availability

The authors do not have permission to share data.

Acknowledgments

This work was supported by National Key Research Program of China (Grant Nos. 92164201 61921005), National Natural Science Foundation of China (Grant Nos. 61974064 11874198 and 62304200), Natural Science Foundation of Jiangsu Province (Grant No. BK20230562) and Micro-fabrication and Integration Technology Center of Nanjing University.

Author contributions

L. Y. and L. L. proposed, designed and carried out all the experiments; L. W., W. L., W. Q., Y. Z., R. H. and J. W. participated in parts of the experiments and data analysis; L. Y., R. H. and L.L. wrote the manuscript and prepared the figures; all authors took part in the discussions of the experimental results.

Supporting Information

The data is available in the online version of the paper.

Appendix A. Supporting information

Supplementary data associated with this article can be found in the online version at doi:10.1016/j.jallcom.2024.175189.

References

[1] W.-T. Chen, R. Muruganantham, W.-R. Liu, Construction of 3D porous graphene aerogel wrapped silicon composite as anode materials for high-efficient lithium-ion storage, Surf. Coat. Technol. 434 (2022) 128147.

[2] R. Muruganantham, C.-W. Yang, H.-J. Wang, C.-H. Huang, W.-R. Liu, Industrial silicon-wafer-wastage-derived carbon-enfolded Si/Si-C/C nanocomposite anode material through plasma-assisted discharge process for rechargeable Li-ion storage, Nanomaterials 12 (2022) 659.

[3] H.-C. Wang, R. Muruganantham, C.-T. Hsieh, W.-R. Liu, Electrochemical elucidation of phosphorus-doped and 3D graphene aerogel surface-modified SiOx porous nanocomposite electrode material for high-performance lithium-ion batteries, Electrochim. Acta 477 (2024) 143775.

[4] D. Dehghanpour Farashah, F. Beigloo, A. Mohammadi Zardkhoshoui, S. Saeed Hosseiny Davarani, Boosting energy storage performance: an exploration of tellurium-based hollow FeNiCoTe nanocubes in hybrid supercapacitors, Chem. Eng. J. 474 (2023) 145584.

[5] A. Mohammadi Zardkhoshoui, B. Ameri, S. Saeed Hosseiny Davarani, A hybrid supercapacitor assembled by reduced graphene oxide encapsulated lollipop-like FeNi2S4@Co9S8 nanoarrays, Chem. Eng. J. 470 (2023) 144132.

[6] M. Molaei, M. Abdollahi, A.M. Zardkhoshoui, S.S.H. Davarani, Advancements in energy storage: Combining hollow iron cobalt selenide spheres with nickel cobalt layered double hydroxide nanosheets, J. Energy Storage 85 (2024) 111079.

[7] M. Molaei, G.R. Rostami, A.M. Zardkhoshoui, S.S.H. Davarani, In situ tellurization strategy for crafting nickel ditelluride/cobalt ditelluride hierarchical nanostructures: a leap forward in hybrid supercapacitor electrode materials, J. Colloid Interface Sci. 653 (2024) 1683–1693.

[8] W.M. Weber, T. Mikolajick, Silicon and germanium nanowire electronics: physics of conventional and unconventional transistors, Rep. Prog. Phys. 80 (2017) 066502.

[9] C.C. Jia, Z.Y. Lin, Y. Huang, X.F. Duan, Nanowire electronics: from nanoscale to macroscale, Chem. Rev. 119 (2019) 9074–9135.

[10] Y. Sun, T.G. Dong, L.W. Yu, J. Xu, K.J. Chen, Planar Growth, integration, and applications of semiconducting nanowires, Adv. Mater. 32 (2020) e1903945.

[11] R.J. Hu, Y.F. Liang, W.T. Qian, X. Gan, L. Liang, J.Z. Wang, Z.G. Liu, Y. Shi, J. Xu, K.J. Chen, L.W. Yu, Ultra-confined catalytic growth integration of Sub-10 nm 3D stacked silicon nanowires via a self-delimited droplet formation strategy, Small 18 (2022) e2204390.

[12] L. Liang, R. Hu, L. Yu, Toward monolithic growth integration of nanowire electronics in 3D architecture: a review, Sci. China Inf. Sci. 66 (2023) 200406.

[13] J. Wallentin, M.T. Borgström, Doping of semiconductor nanowires, J. Mater. Res. 26 (2011) 2142–2156.

[14] Y. Cui, X. Duan, J. Hu, C.M. Lieber, Doping and electrical transport in silicon nanowires, J. Phys. Chem. B 104 (2000) 5213–5216.

[15] K. Byon, D. Tham, J.E. Fischer, A.T. Johnson, Synthesis and postgrowth doping of silicon nanowires, Appl. Phys. Lett. 87 (2005) 193104.

[16] E.C. Garnett, Y.-C. Tseng, D.R. Khanal, J. Wu, J. Bokor, P. Yang, Dopant profiling and surface analysis of silicon nanowires using capacitance–voltage measurements, Nat. Nanotechnol. 4 (2009) 311–314.

[17] O. Moutanabbir, D. Isheim, H. Blumtritt, S. Senz, E. Pippel, D.N. Seidman, Colossal injection of catalyst atoms into silicon nanowires, Nature 496 (2013) 78–82.

[18] S.A. Dayeh, R. Chen, Y.G. Ro, J. Sim, Progress in doping semiconductor nanowires during growth, Mater. Sci. Semicond. Process. 62 (2017) 135–155.

[19] Y. Sun, W.T. Qian, S.S. Liu, T.G. Dong, J.Z. Wang, J. Xu, K.J. Chen, L.W. Yu, Unexpected phosphorus doping routine of planar silicon nanowires for integrating CMOS logics, Nanoscale 13 (2021) 15031–15037.

[20] M.V. Fernández-Serra, C. Adessi, X. Blase, Conductance, surface traps, and passivation in doped silicon nanowires, Nano Lett. 6 (2006) 2674–2678.

[21] M. Šilhavík, M. Müller, J. Stuchlík, H. Stuchlíková, M. Klementová, J. Kočka, A. Fejfar, J. Červenka, Comparative study of catalyst-induced doping and metal incorporation in silicon nanowires, Appl. Phys. Lett. 114 (2019) 132103.

[22] J.P. Meng, Z. Li, Schottky-contacted nanowire sensors, Adv. Mater. 32 (2020) e2000130.

[23] L. Yu, P. Roca, i Cabarrocas, Initial nucleation and growth of in-plane solid-liquid-solid silicon nanowires catalyzed by indium, Phys. Rev. B 80 (2009) 085313.

[24] L.W. Yu, P.J. Alet, G. Picardi, P.R.I. Cabarrocas, An in-plane solid-liquid-solid growth mode for self-avoiding lateral silicon nanowires, Phys. Rev. Lett. 102 (2009) 125501.

[25] L.W. Yu, P.R.I. Cabarrocas, Growth mechanism and dynamics of in-plane solid-liquid-solid silicon nanowires, Phys. Rev. B 81 (2010) 085323.

[26] L.W. Yu, M. Oudwan, O. Moustapha, F. Fortuna, P.R.I. Cabarrocas, Guided growth of in-plane silicon nanowires, Appl. Phys. Lett. 95 (2009) 113106.

[27] W.H. Chen, L.W. Yu, S. Misra, Z. Fan, P. Pareige, G. Patriarche, S. Bouchoule, P.R. I. Cabarrocas, Incorporation and redistribution of impurities into silicon nanowires during metal-particle-assisted growth, Nat. Commun. 5 (2014) 4134.

[28] L.W. Yu, W.H. Chen, B. O'Donnell, G. Patriarche, S. Bouchoule, P. Pareige, R. Rogel, A.C. Salaun, L. Pichon, P.R.I. Cabarrocas, Growth-in-place deployment of in-plane silicon nanowires, Appl. Phys. Lett. 99 (2011) 203104.

[29] R.-D. Chang, Y.-T. Ling, T. Liu, J.-R. Tsai, C.-C. Ma, Diffusion of Indium Implanted in Silicon Oxides, Jpn. J. Appl. Phys. 48 (2009) 056501.

[30] I.C. Kizilyalli, T.L. Rich, F.A. Stevie, C.S. Rafferty, Diffusion parameters of indium for silicon process modeling, J. Appl. Phys. 80 (1996) 4944–4947.

[31] S. Scalese, M. Italia, A. La Magna, G. Mannino, V. Privitera, M. Bersani, D. Giubertoni, M. Barozzi, S. Solmi, P. Pichler, Diffusion and electrical activation of indium in silicon, J. Appl. Phys. 93 (2003) 9773–9782.

[32] S. Solmi, A. Parisini, M. Bersani, D. Giubertoni, V. Soncini, G. Carnevale, A. Benvenuti, A. Marmiroli, Investigation on indium diffusion in silicon, J. Appl. Phys. 92 (2002) 1361–1366.

[33] K. Suzuki, H. Tashiro, T. Aoyama, Diffusion coefficient of indium in Si substrates and analytical redistribution profile model, Solid-State Electron. 43 (1999) 27–31.

[34] S. Xu, R. Hu, J. Wang, Z. Li, J. Xu, K. Chen, L. Yu, Terrace-confined guided growth of high-density ultrathin silicon nanowire array for large area electronics, Nanotechnology 32 (2021) 5602.

[35] X.X. Wu, H.G. Ma, H. Yin, D.F. Pan, J.Z. Wang, L.W. Yu, J. Xu, Y. Shi, K.J. Chen, 3D sidewall integration of ultrahigh-density silicon nanowires for stacked channel, Electron. Adv. Electron. Mater. 5 (2019) 1800627.

[36] L.W. Yu, P.R.I. Cabarrocas, Morphology control and growth dynamics of in-plane solid-liquid-solid silicon nanowires, Phys. E: Low. Dimens. Syst. Nanostruct. 44 (2012) 1045–1049.

[37] D.-Y. Jeon, S. Pregl, S.J. Park, L. Baraban, G. Cuniberti, T. Mikolajick, W.M. Weber, Scaling and graphical transport-map analysis of ambipolar schottky-barrier thin-film transistors based on a parallel array of Si nanowires, Nano Lett. 15 (2015) 4578–4584.

[38] M. Schwarz, T.D. Vethaak, V. Derycke, A. Francheteau, B. Iniguez, S. Kataria, A. Kloes, F. Lefloch, M. Lemme, J.P. Snyder, W.M. Weber, L.E. Calvet, The Schottky barrier transistor in emerging electronic devices, Nanotechnology 34 (2023) 352002.

[39] D. Martin, A. Heinzig, M. Grube, L. Geelhaar, T. Mikolajick, H. Riechert, W. M. Weber, Direct probing of Schottky barriers in Si nanowire schottky barrier field effect transistors, Phys. Rev. Lett. 107 (2011) 216807.

[40] R.A. Schlitz, D.E. Perea, J.L. Lensch-Falk, E.R. Hemesath, L.J. Lauhon, Correlating dopant distributions and electrical properties of boron-doped silicon nanowires, Appl. Phys. Lett. 95 (2009) 162101.

[41] Y. Shan, S.J. Fonash, Self-assembling silicon nanowires for device applications using the nanochannel-guided "grow-in-place" approach, ACS Nano 2 (2008) 429–434.

[42] O.M. Nayfeh, D.A. Antoniadis, S. Boles, C. Ho, C.V. Thompson, Formation of single tiers of bridging silicon nanowires for transistor applications using vapor–liquid–solid growth from short silicon-on-insulator sidewalls, Small 5 (2009) 2440–2444.

[43] K. Takei, T. Takahashi, J.C. Ho, H. Ko, A.G. Gillies, P.W. Leu, R.S. Fearing, A. Javey, Nanowire active-matrix circuitry for low-voltage macroscale artificial skin, Nat. Mater. 9 (2010) 821–826.

[44] W.S. Wong, S. Raychaudhuri, R. Lujan, S. Sambandan, R.A. Street, Hybrid Si nanowire/amorphous silicon FETs for large-area image sensor arrays, Nano Lett. 11 (2011) 2214–2218.

[45] M. Mongillo, P. Spathis, G. Katsaros, P. Gentile, S. De Franceschi, Multifunctional devices and logic gates with undoped silicon nanowires, Nano Lett. 12 (2012) 3074–3079.

[46] J. Yao, H. Yan, C.M. Lieber, A nanoscale combing technique for the large-scale assembly of highly aligned nanowires, Nat. Nanotechnol. 8 (2013) 329–335.

[47] M. Collet, S. Salomon, N.Y. Klein, F. Seichepine, C. Vieu, L. Nicu, G. Larrieu, Large-scale assembly of single nanowires through capillary-assisted dielectrophoresis, Adv. Mater. 27 (2015) 1268–1273.

[48] A. Behroudj, D. Geiger, S. Strehle, Epitaxial bottom-up growth of silicon nanowires on oxidized silicon by alloy-catalyzed gas-phase synthesis, Nano Lett. 19 (2019) 7895–7900.

[49] D. Liu, Z. Shi, L. Zhang, C. He, J. Zhang, M. Cheng, R. Yang, X. Tian, X. Bai, D. Shi, G. Zhang, Reducing the contact resistance of SiNW devices by employing a heavily doped carrier injection layer, Nanotechnology 23 (2012) 305701.

[50] A.A. Shukkoor, S. Karmalkar, Doping dependence of the contact resistivity of end-bonded metal contacts to thin heavily doped semiconductor nanowires, J. Appl. Phys. 122 (2017) 214501.