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ARTICLE

Extremely Uniform Growth Integration of Stacked Silicon Nanowire Channels for High-Performance Transistors via an Embedded-Precursor-Feeding Strategy

Lei Liang, Wentao Qian, Lei Yan, MingYu Xie, Wei Liao, Junyang An, Ruijin Hu,* Junzhuan Wang, and Linwei Yu*

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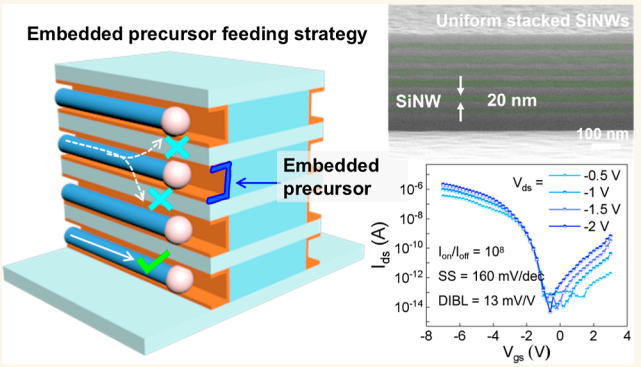
ABSTRACT: Bottom-up catalytic growth has proven to be an exceptionally powerful method for producing ultrathin silicon nanowires (SiNWs) through a low-temperature, high-yield process. However, in order to serve as quasi-one-dimensional (1D) channels for building high-performance field effect transistors (FETs) within monolithic three-dimensional (3D) integration architectures, the diameter uniformity and spatial arrangement of these catalytical SiNWs have to be precisely controlled. In this work, we report on an embedded-precursor-feeding (EPF) strategy to accomplish an extremely uniform growth integration of horizontally stacked SiNWs arrays, with a diameter of D_{nw} = 20 ± 2 nm and a high growth yield >90%. Specifically, these SiNWs were produced via the indium droplet-catalyzed in-plane solid−liquid−solid (IPSLS) mechanism, where the amorphous silicon (a-Si) precursor layer has been embedded within the vertical SiN_x/SiO_2 sidewall grooves through a simple anisotropic etching. It has been found that the removal of the exposed a-Si precursor on the protrusive sidewalls and the exposed areas can completely suppress the undesired growth derailing or track-striding among neighbor SiNWs, as well as the random growth on the top and bottom platforms. Based on these rather uniform SiNW channels, prototype fin-gate FETs were successfully fabricated, achieving a high on/off current ratio of ~10^8 and a subthreshold swing of ~160 mV/dec. This convenient but rather effective EPF strategy represents a key capability to establish the catalytical IPSLS growth as a reliable growth-in-place integration approach to batch-manufacture advantageous SiNW channels for building high-performance FETs in monolithic 3D integration architecture.



KEYWORDS: *catalytical growth, uniformity control, silicon nanowires, in-plane solid−liquid−solid, transistor*

INTRODUCTION

Bottom-up catalytical growth provides a low-temperature and high-yield approach to prepare quasi-one-dimensional silicon nanowire (SiNW) channels for high-performance field-effect transistors (FETs).[4−13] This method is particularly advantageous for monolithic three-dimensional (M3D) integration architecture,[14−17] where multiple device layers are sequentially fabricated and vertically stacked to achieve advanced non-von Neumann paradigms for logic-in-memory[18] and neuromorphic computing.[1,19] This arises from the fact that the bottom-layer devices of the M3D are typically fabricated via conventional top-down methods, which rely on etching into Si wafers or epitaxial Si/SiGe layers to obtain Si channels, requiring temperatures greater than 600 °C,[14,18] as illustrated in Figure 1a. However, to prevent performance degradation in bottom-layer devices, the top-layer crystalline silicon channels should be produced under a low thermal budget of 500 °C[14,18] (Figure 1b).

To this end, low-temperature catalytic growth shows promising potential. For example, vapor−liquid−solid (VLS),[8,12,20−22] a well-established bottom-up method, has

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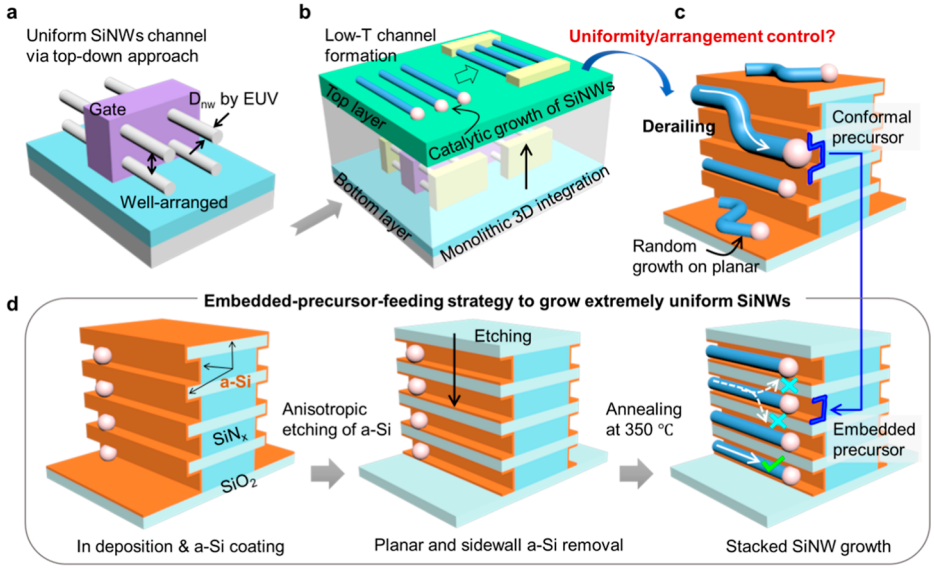

Figure 1. Embedded-precursor-feeding strategy for the growth of uniform stacked SiNWs. (a) Schematic illustration of a gate-all-around field-effect transistor (GAA-FET) with uniform and well-arranged SiNW channels, fabricated by extreme ultraviolet lithography (EUV) and etching of Si/SiGe epitaxial layers. (b) Schematic diagram of the monolithic three-dimensional (3D) integration architecture, where SiNWs grown via a low-temperature catalytic growth are superior channels for top-layer devices. (c) Undesired growth scenarios for the conformal amorphous silicon (a-Si) precursor, including SiNWs derailing and random growth on top/bottom platforms. (d) Fabrication process for achieving extremely uniform SiNWs arrays via the embedded-precursor-feeding strategy.

been extensively used to synthesize SiNW channels for applications in functional electronic and optoelectronic devices, such as logic, memory, sensor, and nanoelectromechanical system components.[8,18,20,22−25] However, the free-standing geometry and random distribution of SiNWs cause a significant challenge in integrating them into scalable devices, which usually feature planar structures. Recently, a relatively new in-plane solid−liquid−solid (IPSLS) mechanism has been developed, in which indium (In) catalyst droplets are guided to move along the edge of the predesignated steps to absorb an amorphous silicon (a-Si) precursor to produce SiNWs on the surface of the substrate at 350 °C.[26−30] Furthermore, the growth can be extended into 3D space, for example, on the vertical sidewall, to produce stacked horizontal SiNWs arrays,[31−36] which can be assembled into the gate-all-around (GAA) configuration to enhance the gate control capabilities. Though decent SiNWs arrays and prototype FETs have been demonstrated,[4,5,37] the controllability over the diameter and the spatial arrangement of the IPSLS mechanism remains inferior to that of top-down approaches. The diameter of SiNW channels for the top-down can be precisely defined by high-resolution lithography such as deep ultraviolet (DUV) or extreme ultraviolet (EUV) lithography.[2,3,17,38−41] But for the IPSLS mechanism, SiNWs may derail from its own track during the growth, as depicted in Figure 1c, resulting in the undesired thick ones and causing the nonideal diameter uniformity and spatial arrangement. Meanwhile, randomly grown SiNWs on the top/bottom platforms further degrade the uniformity due to the lack of restrictions on In droplet size and growth paths.

In this work, we report an embedded-precursor-feeding (EPF) strategy to grow extremely uniform stacked SiNWs arrays on the vertical sidewall of SiN_x/SiO_2 multilayers. By removing the a-Si film from the protrusive SiO_2 sidewall and top/bottom platforms, an embedded precursor configuration is formed within SiN_x grooves, significantly suppressing growth derailing and random growth. Consequently, SiNWs with a diameter of D_{nw} = 20 ± 2 nm and a high growth yield >90% have been achieved. Built upon these SiNW channels, the fin-gate FET demonstrates a high on/off current ratio (I_{on}/I_{off}) of ~10^8 and a subthreshold swing (SS) of ~160 mV/dec.

RESULTS AND DISCUSSION

In order to achieve stacked SiNWs arrays on the vertical sidewalls, multiple layers of SiN_x and SiO_2 were alternately deposited on the silicon wafer precoated with a 500 nm thick SiO_2 layer using a plasma-enhanced chemical vapor deposition (PECVD) system. Then, the multilayers were patterned by lithography and etched with C_4F_8 gas plasma to expose the sidewalls, followed by the selective etching of the SiN_x layer with 85% H_3PO_4 solvents at 165 °C, forming the periodic concave grooves, as illustrated in Figure 1d. After that, the In catalyst stripes were patterned and deposited by electron beam evaporation (EBE) at a title angle, which was followed by the H_2 plasma treatment to transform stripes into discrete droplets and reduce the outer oxide layer. To achieve the embedded precursor configuration, the sample was first conformally coated with a-Si film at 100 °C and then treated with H_2 plasma by the anisotropic etching method at 150 °C. These two steps were alternately repeated over several cycles in the PECVD system to ensure sufficient a-Si within the grooves, while minimizing deposition on the protrusive sidewalls and top/bottom platforms, as illustrated in Figure S1. Finally, the growth was activated at 350 °C under high vacuum, where the In droplets started to absorb the a-Si precursor and move in the grooves to produce SiNWs. A more detailed description of the fabrication procedures is provided in the Methods section of the Supporting Information. Due to the ultrathin a-Si film on the sidewalls, which was insufficient to support the growth, the In droplets tended to be confined to their respective grooves, thus eliminating the track-striding between neighboring grooves.

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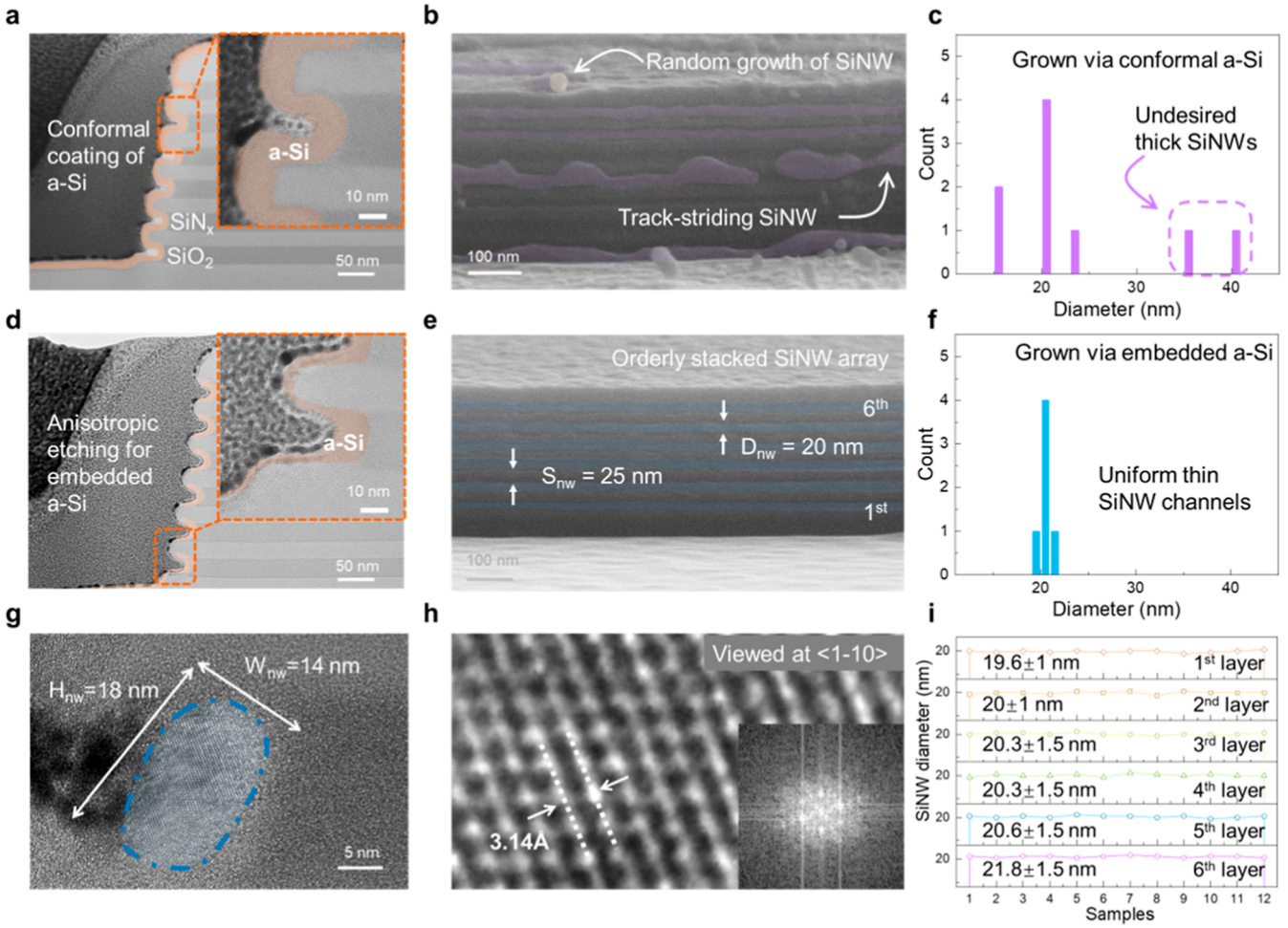

Figure 2. Characterization of SiNWs grown via conformal and embedded a-Si precursors. (a) TEM image of the conformal a-Si layer coating on the sidewall grooves. (b) SEM image of as-grown SiNWs, with track-striding between neighboring grooves. (c) Statistics on the SiNWs diameter. (d) Formation of the embedded precursor via anisotropic etching, showing minimal a-Si on protrusive sidewalls and sufficient a-Si within the grooves. (e) Typical SEM image of uniform stacked SiNWs, with corresponding statistics in (f). (g,h) High-resolution TEM images of the SiNW. (i) Statistics of SiNWs diameters across different layers.

To investigate the influence of the a-Si precursor configuration, stacked SiNWs arrays were grown with both conformally coated and embedded a-Si. Figure 2a,d presents the cross-sectional transmission electron microscopy (TEM) images of the sidewall grooves with the a-Si film highlighted in orange. As demonstrated in Figure 2a, the a-Si film, deposited continuously using PECVD at a low radio frequency (RF) power (~1 W), exhibits a uniform thickness across the upper surface and lower surface, as well as the bottom of the grooves. Thicker a-Si layers are observed on the protrusive sidewalls and the top/bottom platforms. Figure 2b presents the scanning electron microscope (SEM) image of the as-grown SiNWs, where the SiNWs are pseudocolored with purple. A unregular SiNW strides from the fourth groove to the third groove during growth, resulting in an island-chain structure with thicker segments connected by thinner regions. The diameter of these island-chain SiNWs, referring to the height of the island, is significantly larger than that of SiNWs without experiencing track-striding. The track-striding phenomenon between adjacent grooves leads to uncontrollable NW-to-NW spacing and nonuniform SiNWs diameters, as revealed by the statistics in Figure 2c. Moreover, SiNWs can also grow on the top and bottom platforms due to the sufficient a-Si supply, which usually features random growth directions owing to the absence of guiding steps or grooves.

In comparison, by introducing the H_2 plasma anisotropic etching after the deposition of a-Si, the exposed a-Si on protrusive sidewalls and top/bottom platforms is almost removed, leaving a-Si only in the groove bottoms, thus forming an embedded a-Si configuration, as verified in Figure 2d. The track-striding phenomenon is completely suppressed because the a-Si film on the protrusive sidewall is too thin to support In droplets moving across it. Besides, the random growth on top/bottom platforms is also eliminated due to the lack of an a-Si precursor. Consequently, the SiNWs grown with the EPF strategy demonstrate an extremely uniform diameter (D_{nw}) of 20 ± 2 nm and a regular spatial arrangement with a NW-to-NW spacing (S_{nw}) of ~25 nm, as shown in Figure 2e and statistics in Figure 2f. To examine the diameter consistency across different SiNWs arrays, 12 samples of 6-layer stacked SiNWs are randomly chosen for diameter measurement, as plotted in Figure 2i. The diameter of the SiNWs grown via the EPF strategy demonstrates satisfactory uniformity across different samples. The crystallinity and the cross-sectional profile of the SiNWs are investigated by cutting off a slice of the stack array via a focused ion beam (FIB) and

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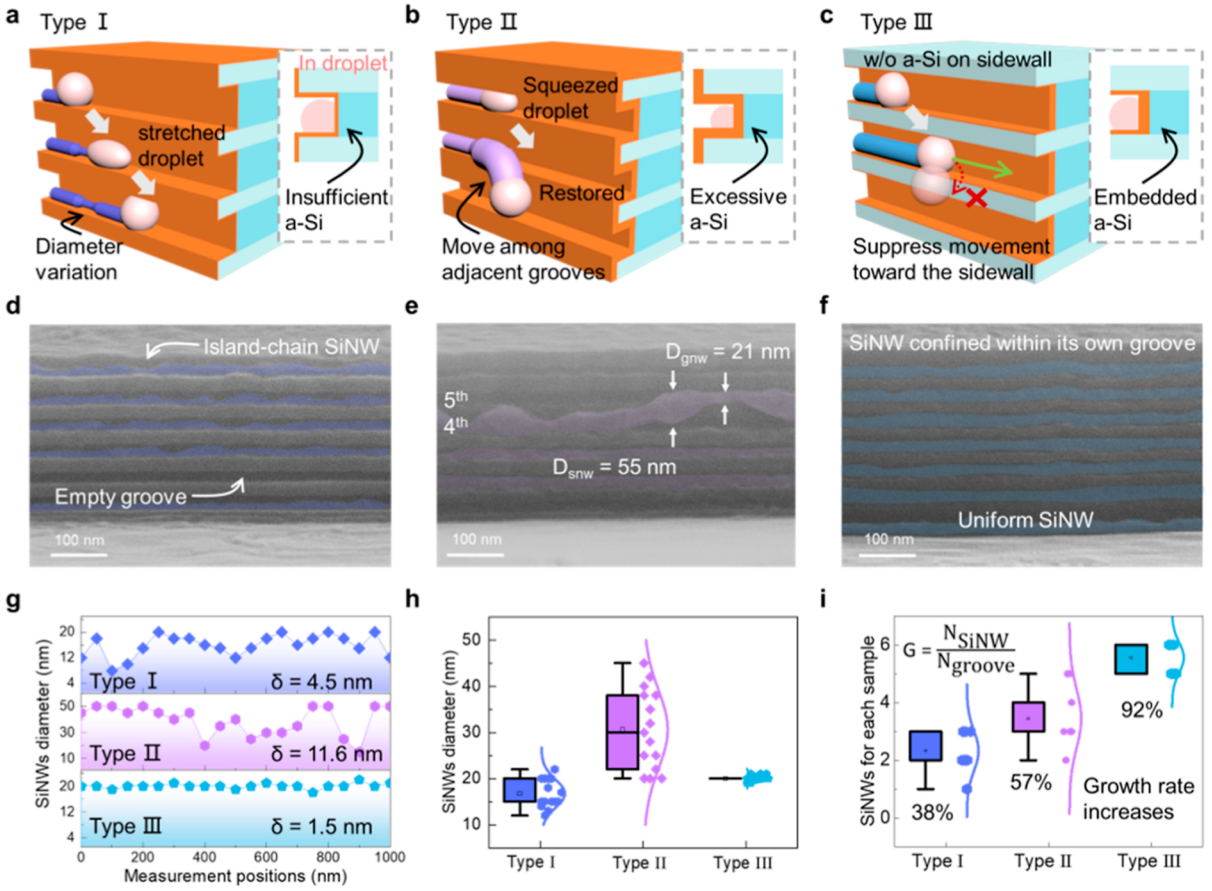

Figure 3. Impact of a-Si configuration on SiNW morphology. (a–c) Schematic illustrations of SiNW growth dynamics under the conditions of insufficient, excessive, and embedded a-Si, respectively. (d–f) SEM images of SiNWs grown via different a-Si configurations, with statistics on diameter and growth rate presented in (g–i).

then analyzed by TEM. Figure 2g shows a typical TEM image of the SiNW grown within the grooves, exhibiting an elliptical shape with a height (H_{nw}) of 18 nm and a width (W_{nw}) of 14 nm. High-resolution TEM confirms that SiNW is monocrystalline, with a lattice fringe spacing of 3.14 Å corresponding to the Si(111) plane and a growth direction along Si < 110>. Although Si < 110> is more commonly observed, other growth directions along Si < 100> and Si < 211> are also found, as indicated by the statistics in Figure S2. Nevertheless, these results experimentally prove that the EPF strategy is an efficient and practical method for improving the diameter uniformity of the catalytically grown stacked SiNWs.

The key to growing uniform stacked SiNWs is to obtain a suitable a-Si configuration that establishes growth balance and simultaneously suppresses undesired derailing. During IPSLS growth, the soft liquid catalyst In droplet, capable of deformation, is sandwiched between the front In/a-Si and the rear SiNW/In interfaces. When growth balance is established by synchronized propagation of the front In/a-Si absorption interface and the rear SiNW/In deposition interface, the In droplet retains a spherical morphology during the growth, thus producing SiNWs with a consistent diameter proportional to the size of the In droplet. On the other hand, when the a-Si precursor is too thin to provide sufficient Si atoms (type I a-Si configuration), the moving speed of the front absorption interface accelerates, while the rear deposition interface slows down. As a result, the In droplet is forced to elongate, producing a SiNW segment with a smaller diameter, as illustrated in Figure 3a. However, due to Plateau–Rayleigh instability,[42] the elongated geometry, which is energetically unfavorable, eventually reverts to its initial spherical shape. This periodic deformation of the In droplets results in island-chain SiNWs, as demonstrated in Figure 3d. Additionally, the ultrathin a-Si film often fails to supply sufficient Si atoms to trigger the growth, causing a low growth rate (G) where G is the ratio of the number of SiNWs (N_{SiNW}) to the number of grooves (N_{groove}).

In comparison, when an excessive a-Si film is conformally coated on the sample (type II a-Si configuration), with a thickness comparable to the height of grooves (H_{groove}), the In droplet is squeezed to fit in the grooves, producing SiNWs with a diameter (D_{gnw}) equal to that of H_{groove}. During the growth, the front absorption interface moves more slowly than the rear deposition interface due to the excessive a-Si supply, squeezing the middle In droplets and leading to strain accumulation. To relieve strain, the droplet tends to turn/step out of the groove and move to the protrusive sidewalls, restoring the spherical shape, as shown in Figure 3b. With sufficient a-Si on the sidewalls, a SiNW segment with a diameter (D_{snw}) much larger than that of D_{gnw} is produced. The In droplet is then captured by the lower groove and squeezed in to continuously lead the growth. A typical SEM image of the SiNWs array grown via the excessive a-Si layer is provided in Figure 3e, where a SiNW derails from the fifth groove, slides down the sidewall to produce a thick segment, and then squeezes into the fourth groove. Additionally, the derailing of SiNW inevitably results in

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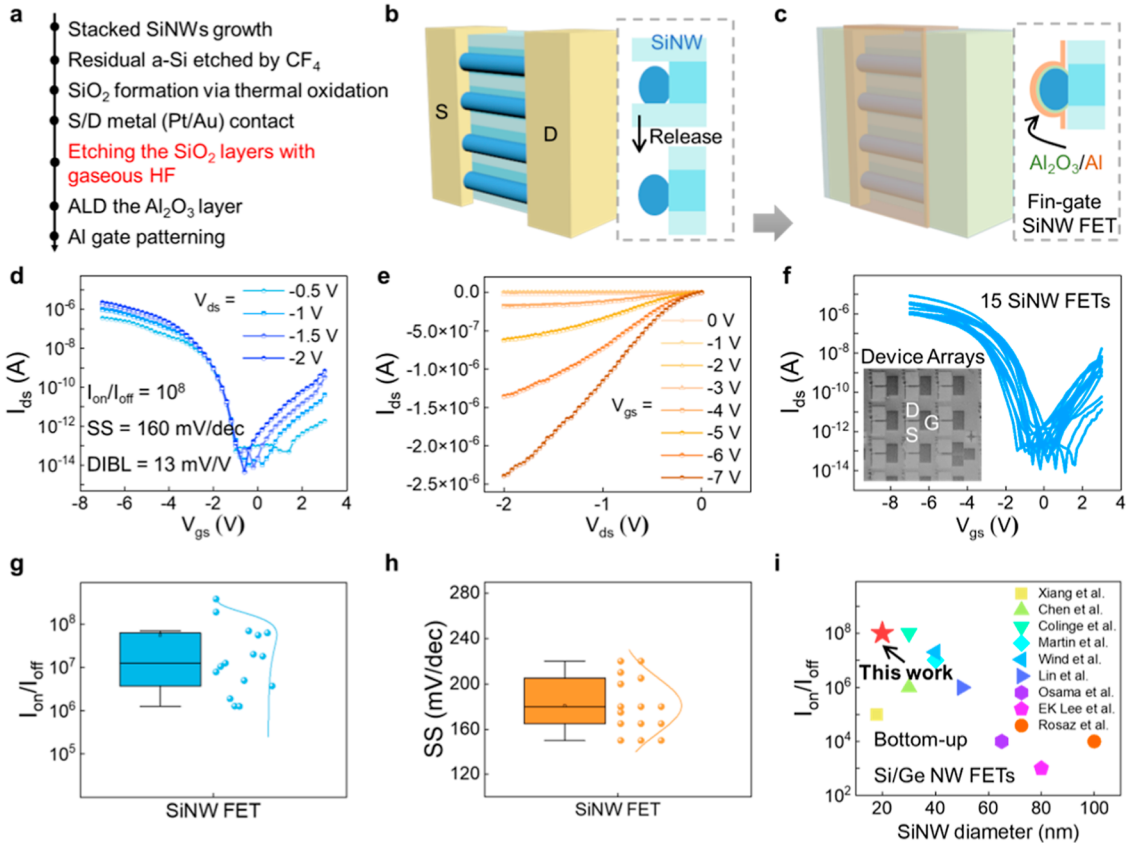

Figure 4. Device performance of SiNW fin-gate FETs. (a) Key fabrication steps for SiNW FETs. (b,c) Illustration of the fin-gate FET structure. (d,e) Transfer and output characteristics. (f) I_{ds}–V_{gs} curve for 15 devices. (g,h) Statistics of the on/off current ratio and SS. (i) Performance comparison of devices built upon silicon/germanium nanowires prepared by bottom-up approaches.

empty grooves, which reduces the growth rate. Neither the type I nor the type II a-Si configuration can enable a uniform stacked SiNWs array or a high growth rate.

Notably, the a-Si configuration should meet two criteria to achieve the uniform growth integration of horizontally stacked SiNWs arrays: first, a-Si in the grooves must be sufficient but not excessive, and second, a-Si on the protrusive sidewalls should be minimal to avoid the track-striding among neighboring grooves. Thus, a tailored a-Si configuration, where a-Si film is embedded into the grooves with almost none on the sidewalls and top/bottom platforms (type III a-Si configuration) via the EPF strategy, is more advantageous to achieve an extremely uniform growth. As illustrated in Figure 3c, compared to the type II a-Si configuration, the a-Si film on the upper surface and the lower surface of the groove is significantly thinner due to the lateral H_2 plasma etching, while the a-Si at the groove bottom remains intact owing to the thin and deep groove structure. As a result, the a-Si supply is more likely sufficient but not excessive, decreasing the possibility of In droplet turning. More importantly, the absence of an a-Si film on the sidewall eliminates the driving forces required for directional In droplet migration, causing In droplets to be limited within grooves, which produces SiNWs with a consistent diameter rather than the island-chain structures grown via type I and type II a-Si configurations, as indicated by the SEM image in Figure 3f and statistics in Figure 3g,h. Moreover, since the EPF strategy confines In droplets within their respective groove, eliminating interference within adjacent grooves, a higher growth rate of about 90% can be achieved, as presented in Figure 3i. By simply incorporating an extra etching step, both the diameter uniformity and the growth rate can be effectively improved, offering a practical strategy to enhance the reliability of catalytical growth for batch-manufacturing 3D stacked SiNWs channels.

The prototype Schottky barrier FETs with a fin-gate structure were fabricated based on the uniform stacked SiNWs arrays, following the procedures listed in Figure 4a. After the remaining a-Si was etched by CF_4 plasma in a reactive ion etching (RIE) system, a thin SiO_2 layer was formed via thermal oxidation to reduce the interface state between SiNWs and the high-k dielectric layer. Next, source/drain (S/D) electrodes (Pt/Au: 5/55 nm) were patterned by lithography with a 1.5 μm separation and deposited via an EBE system, where the thin SiO_2 layer in the S/D region was etched by HF solution before metal film deposition. Then, the protrusive sidewalls (light green ~SiO_2) were removed by gaseous HF in a homemade system (Figure S3), to release the SiNWs channels (blue region) from the grooves, as illustrated in Figure 4b. Subsequently, a 15 nm Al_2O_3 layer (green region) and 45 nm Al gate (orange region) were covered onto the SiNW channels to form a fin-gate structure, which can provide enhanced electrostatic gate control, as indicated in Figure 4c.

The typical transfer and output characteristics of the stacked SiNWs FET are provided in Figure 4d,e, showing a high I_{on}/I_{off} of ~10^8, an SS of 160 mV/dec, and a drain-induced barrier lowering (DIBL) of ~13 mV/V. To evaluate device consistency, 15 devices were randomly selected and measured, with their characteristics depicted in Figure 4f and statistics on I_{on}/I_{off} and SS plotted in Figure 4g,h. All these devices exhibit $I_{on}/I_{off} > 10^6$ and SS < 230 mV/dec. Compared to other FETs

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ACS Nano XXXX, XXX, XXX−XXX

based on catalytic synthesized Si/Ge NWs, as summarized in Figure 4i, our devices demonstrate superior electrical properties in terms of channel diameter and I_{on}/I_{off}.[7,10,12,26,43−47] These results indicate that the stacked SiNWs arrays grown via the EPF strategy can serve as the preferable channel material for constructing high-performance top-layer devices in M3D integration architecture.

CONCLUSION

In conclusion, we have developed a reliable catalytic method to produce extremely uniform stacked SiNW arrays, built upon the IPSLS mechanism, via an embedded-precursor-feeding strategy at a growth temperature of 350 °C. By removing the exposed a-Si precursor on protrusive sidewalls and top/bottom platforms, the derailing phenomenon and random growth on platforms have been significantly suppressed, achieving extremely uniform stacked SiNWs with a diameter of 20 ± 2 nm and a regular 3D spatial arrangement with an NW-to-NW spacing of ∼25 nm. Prototype FETs based on stacked SiNWs demonstrate a remarkable I_{on}/I_{off} of $\sim 10^8$ and a decent SS of 160 mV dec^{-1}. These results provide a simple yet efficient method to improve the reliability of catalytic growth, which shows promising applications in the M3D architecture and sensors.

EXPERIMENTAL SECTION

Sidewall Grooves Formation. First, the substrate was cleaned with acetone, ethanol, and deionized water, respectively. Then, the sample was loaded into the PECVD system for SiNx/SiO_2 multilayers deposition at 300 °C. A SiNx layer was deposited with a gas of SiH_4, NH_3, and N_2, while a SiO_2 layer was deposited with a gas of SiH_4, NO_2, and N_2. Next, the SiNx/SiO_2 multilayers sample was patterned by photoresist via lithography, followed by C_4F_8 plasma etching in the ICP system. The exposed vertical sidewalls were immersed in the H_3PO_4 solution to form the sidewall grooves.

SiNWs Growth. The region for the In catalyst in the sample was patterned by lithography followed by EBE evaporation. Then, the sample was loaded into the PECVD system for H_2 plasma treatment. After that, the a-Si film precursor was deposited by silane plasma and etched by H_2 plasma with periodic cycles. Finally, the active In droplets can absorb the nearby precursor and move along the groove to form stacked SiNWs.

Device Fabrication. The remnant a-Si film was etched by H_2 plasma and stacked SiNWs were annealed at high temperature. Stacked SiNWs arrays on the sidewalls were patterned to define a source-drain region, and Pt/Au electrodes were deposited by the EBE system. After that, the SiO_2 layer was removed by the HF gas etching system, followed by the Al_2O_3 dielectric layer via the ALD system. Finally, the top gate Al electrode was evaporated by a sputtering system.

More details are available in the Supporting Information and previous literature.

ASSOCIATED CONTENT

Data Availability Statement

All data are available in the main text or the Supporting Information.

Supporting Information

The Supporting Information is available free of charge at https://pubs.acs.org/doi/10.1021/acsnano.5c09735.

Procedure of forming the embedded a-Si precursor configuration, statistics on the growth direction of SiNWs, illustration of the homemade gaseous HF etching system, and more details about SiNWs growth and device fabrication (PDF)

AUTHOR INFORMATION

Corresponding Authors

Ruijin Hu − *College of Physical Science and Technology/Microelectronics Industry Research Institute, Yangzhou University, 225002 Yangzhou, P. R. China;* orcid.org/0009-0006-5973-6954; Email: huruijin@yzu.edu.cn

Linwei Yu − *School of Electronics Science and Engineering/National Laboratory of Solid-State Microstructures, Nanjing University, 210093 Nanjing, P. R. China; ZJU-Hangzhou Global Scientific and Technological Innovation Centre, Hangzhou 311200 Zhejiang, P. R. China;* orcid.org/0000-0002-0801-5210; Email: yulinwei@nju.edu.cn

Authors

Lei Liang − *School of Electronics Science and Engineering/National Laboratory of Solid-State Microstructures, Nanjing University, 210093 Nanjing, P. R. China; ZJU-Hangzhou Global Scientific and Technological Innovation Centre, Hangzhou 311200 Zhejiang, P. R. China*

Wentao Qian − *School of Electronics Science and Engineering/National Laboratory of Solid-State Microstructures, Nanjing University, 210093 Nanjing, P. R. China*

Lei Yan − *School of Electronics Science and Engineering/National Laboratory of Solid-State Microstructures, Nanjing University, 210093 Nanjing, P. R. China;* orcid.org/0000-0002-6776-2400

MingYu Xie − *School of Electronics Science and Engineering/National Laboratory of Solid-State Microstructures, Nanjing University, 210093 Nanjing, P. R. China*

Wei Liao − *School of Electronics Science and Engineering/National Laboratory of Solid-State Microstructures, Nanjing University, 210093 Nanjing, P. R. China;* orcid.org/0009-0006-8804-9395

Junyang An − *School of Electronics Science and Engineering/National Laboratory of Solid-State Microstructures, Nanjing University, 210093 Nanjing, P. R. China;* orcid.org/0009-0008-2522-5165

Junzhuan Wang − *School of Electronics Science and Engineering/National Laboratory of Solid-State Microstructures, Nanjing University, 210093 Nanjing, P. R. China*

Complete contact information is available at: https://pubs.acs.org/10.1021/acsnano.5c09735

Author Contributions

J. W. and L.Y. proposed and supervised the project. R. H. and L.Y. designed the experiments. L. L. performed the sample fabrication and device measurement. W. Q., L. Y., M. X., and J. A. contributed to the data analysis. R. H. and L.Y. co-wrote the paper. All authors discussed the results and commented on the paper.

Notes

The authors declare no competing financial interest.

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