Chip

Research Article

MICRO-NANOELECTRONICS

DOI: 10.1016/j.chip.2024.100098

Channel-bias-controlled reconfigurable silicon nanowire transistors via an asymmetric electrode contact strategy

Wentao Qian, Junzhuan Wang*, Jun Xu & Linwei Yu*

School of Electronic Science and Engineering/National Laboratory of Solid-State Microstructures, Nanjing University, Nanjing 210093, China

*E-mails: wangjz@nju.edu.cn (Junzhuan Wang), yulinwei@nju.edu.cn (Linwei Yu)

Cite as: Qian, W., Wang, J., Xu, J. & Yu, L. Channel-bias-controlled reconfigurable silicon nanowire transistors via an asymmetric electrode contact strategy. *Chip* **3**, 100098 (2024).
https://doi.org/10.1016/j.chip.2024.100098

Received: 15 March 2024

Accepted: 3 June 2024

Published online: 8 June 2024

Reconfigurable field-effect transistors (R-FETs) that can dynamically reconfigure the transistor polarity, from n-type to p-type channel or vice versa, represent a promising new approach to reduce the logic complexity and granularity of programmable electronics. Although R-FETs have been successfully demonstrated upon silicon nanowire (SiNW) channels, a pair of extra program gates is still needed to control the source/drain (S/D) contacts. In this work, we propose a rather simple single gate R-FET structure with an asymmetric S/D electrode contact, where the FET channel polarity can be altered by changing the sign of channel bias V_{ds}. These R-FETs were fabricated upon an orderly array of planar SiNW channels, grown via in-plane solid-liquid-solid mechanism, and contacted by Ti/Al and Pt/Au at the S/D electrodes, respectively. Remarkably, this channel-bias-controlled R-FET strategy has been successfully testified and implemented upon both p-type-doped (with indium dopants) or n-type-doped (phosphorus) SiNW channels, whereas the R-FET prototypes demonstrate an impressive high $I_{on/off}$ ratio of > 10^6 and a steep subthreshold swing of 79 mV/dec. These results indicate a rather simple, compact and generic enough R-FET strategy for the construction of a new generation of SiNW-based programmable and low-power electronics.

Keywords: Catalytic Si nanowires, Asymmetric electrodes, Reconfigure transistor

INTRODUCTION

Efficient p-type and n-type doping control in the channel of field-effect transistors (FETs) provides the key basis for the implementation of complementary metal–oxide–semiconductor (CMOS) logics with quasi-zero static power consumption, high integration density and stability[1–5]. Usually, this logic polarity of FETs is static and could be determined by the dopant type in the channel. In pursuit of the reconfigurability of more functional logic gates and designing the prototype platforms, there have been increasing research interests and efforts devoted to reconfigurable FET (R-FET) devices by using a wide range of channel/contact materials, including planar polycrystalline silicon[6,7], one-dimensional (1D) nanowires (NWs)[8–12], carbon nano-tubes (CNTs)[13,14], and two-dimensional thin film[15–17]. Actually, these R-FET units can also be considered as the finest logic grain in programmable electronics, following the evolution line of field-programmable gate array dated back to 1984[18]. It has been envisioned that the capability of altering the n-/p-type polarity of FET at runtime, as illustrated schematically in Fig. 1a, will bring in a new dimension for achieving more diverse and flexible logic implementation, a higher function density of integrated circuits, as well as a more convenient platform for rapid testification and prototyping[19–21].

The first R-FET device was demonstrated based on a silicon nanowire (SiNW)-channel FET in 2011, with two separately controlled independent gates located at the metal-semiconductor Schottky contacts[22]. The following R-FET devices[10,23] usually adopted two extra program gates (PGs) that need to be fabricated and positioned exactly over the Schottky-contact interfaces between the metal electrode and the SiNW channels, in addition to the conventional center control gate, as indicated in Fig. 1b. Although adding the role of the two PG electrodes is critical to effectively tune the barrier profile and thickness of the Schottky barrier (SBs), it will also increase the structural complexity of R-FET manufacturing and require the precise alignment of PG electrodes over the SB silicide /SiNW interface, which is typically formed during silicide formation annealing, and this increases the processing uncertainty or technical challenges.

So far, most of these pioneering R-FET devices have been prototyped upon catalytic SiNWs, which serve as ideal quasi-1D semiconducting channels[9,22–25], owing to their excellent electrostatic channel controls and the high-yield growth fabrication of ultrathin high crystallinity 1D channels with diameter < 30 nm, as well as the material compatibility to the mainstream Si technology. Whereas, in view of scalable electronic device integration, there still remains a technical challenge that all of these catalytic SiNWs are grown via a vapor-liquid-solid (VLS) method[26–28], which absorbs gaseous precursor to produce vertical SiNWs. Then, these standing VLS SiNWs still

 DOI: 10.1016/j.chip.2024.100098

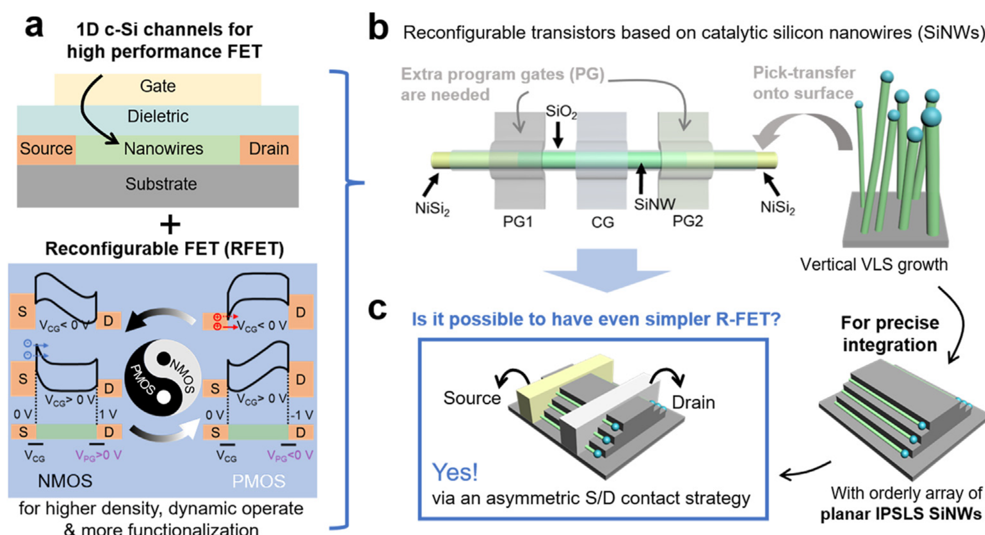

Fig. 1 | Schematic diagram of reconfigurable FET (R-FET). **a**, The construction and mechanism of R-FET with ultrathin SiNW channels for programmable electronics. **b,** The device configuration of R-FET devices, with conventional control gate (CG) and a pair of extra program gates (PGs), built upon catalytic SiNW channels, grown via VLS procedure and then pick-and-transferred onto planar surface. **c,** The new single-gate R-FET structure, proposed in this work, achieved by adopting asymmetric contacts at the source-drain electrodes with different metals, built upon an orderly array of planar SiNWs grown via IPSLS mode and self-positioned on the terrace steps on slopes. Abbreviations: FET, field-effect transistor; IPSLS, in-plane solid-liquid-solid; SiNW, silicon nanowire; VLS, vapor-liquid-solid.

need to be picked, transferred, and re-arranged onto the substrate surface to serve as orderly 1D channels for device fabrication, which is unfortunately not compatible to the planar electronic integration.

In this work, we propose a rather simple single-gate R-FET structure, where the FET polarity can be altered by simply changing the sign of the channel bias of V_{ds}. Specifically, the R-FET devices were constructed upon orderly planar SiNW channels, grown via an in-plane solid-liquid-solid (IPSLS) mechanism[29–34] that allows for a precise guided growth of SiNWs into pre-designed locations. Then, the SiNW channels were connected to the source/drain (S/D) electrodes by adopting different metals to form an asymmetric contact configuration, with only a single gating electrode, as schematically illustrated in Fig. 1c. This rather simple channel-bias-controlled R-FET strategy has been successfully testified on both the p-type- or n-type-doped SiNW channels, without the need of any PG electrodes, indicating a rather convenient and generic approach to implement reconfiguration logics. In comparison to the other dual-gate R-FETs[22–24,35,36], this single-gate configuration, based on self-aligned and scalable catalytic SiNW channels, represents a more compact R-FET device design that can be rather beneficial for seeking higher integration density.

RESULTS AND DISCUSSIONS

The R-FET devices were fabricated upon an n^+-doped wafer substrate coated with 500 nm SiO_2. Fig. 2a–c depict schematically the guided growth of parallel IPSLS SiNWs along the 3 mini-steps formed on terrace slopes, which involves first the formation of a guiding terrace with step height and width of ~120 nm and ~200 nm, respectively (see Fig. 2a); After that, a stripe of catalyst indium (In) was patterned and deposited at the ends of the guiding terrace, with an In stripe width of 6 μm width and nominal thickness of 5 nm (Fig. 2b); Subsequently, the sample was loaded into a plasma-enhanced chemical vapor deposition (PECVD) chamber to produce parallel crystalline SiNWs along the guiding steps via the IPSLS growth mode, with a typical diameter of 30–40 nm which is related to the size of the leading In droplets, as seen for example in the SEM inset of Fig. 2c. It is worthy to note that the diameter of the IPSLS SiNWs can be further reduced to < 20 nm with a higher uniformity with the aids of sidewall or surface guiding grooves[37–39]. More experimental details of the guiding terrace formation and the IPSLS growth of SiNWs are provided from our previous works[39–43]. At the end of SiNW growth, the remnant a-Si precursor film was selectively etched off, followed by a 10 min annealing process @850 ^{o}C in dry O_2 atmosphere to form a SiO_2 layer of ~10 nm thick.

Prior to proceeding to the fabrication of R-FET, it is noteworthy that the doping polarity of the as-grown SiNWs can be effectively controlled to p-type or n-type, by using intrinsic or n-doped a-Si precursors, respectively. It has been known and verified in our previous works that the incorporation of In atoms into c-SiNW channels can serve as p-type dopants, and thus give rise to p-type doping in the channels[32,44], while pre-doping in a-Si layer with phosphorus atoms can reverse the doping polarity to n-type[45]. After contacting the planar SiNWs with a symmetric S/D metal electrode of Ti/Al for n-type SiNWs, or Pt/Au for p-type SiNWs as illustrated in Fig. 2d, an Al_2O_3 dielectric layer of 25 nm thickness was coated by atomic layer deposition (ALD). Note that the contact metals of Ti and Pt are not supposed to form significant alloy phase or inter-diffuse/mixing at 200 ^{o}C[46,47], followed by patterning and depositing 60 nm thick Al as the top gate (Fig. 2d–f), with the SEM image of the typical S/D electrodes shown in Fig. 2g. In this junctionless Schottky barrier FET configuration, both the phosphorus-doped N-type channel and the indium-doped p-type channel FETs have been successfully fabricated, with an $I_{on/off}$ ratio of > 10^6 and subthreshold swing (*SS*) of 165 mV/dec for the n-type FET, while $I_{on/off}$ ratio > 10^6 and *SS* ~261 mV/dec for the p-type FET, as shown in Fig. 2h and Fig. 2i, respectively.

The R-FET device based on asymmetric S/D metal contact was first testified on In-doped p-type SiNW channels, where as depicted in Fig. 3a, Ti/Al and Pt/Au metals were evaporated and patterned at drain and source electrodes, respectively, with a channel length of 2 μm. The

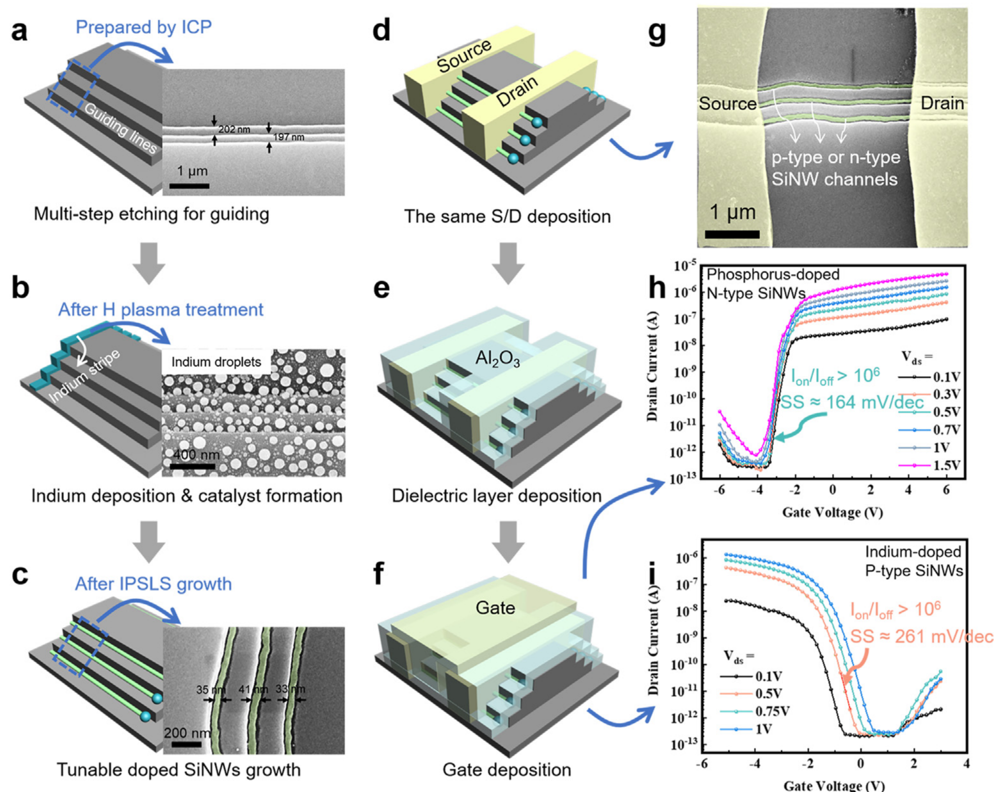

Fig. 2 | IPSLS SiNW growth diagram and fabrication of complementary FETs. **a–c**, Illustrate the formation of guiding terrace, the deposition of catalyst In stripe and the growth of IPSLS SiNWs, with corresponding SEM images in the insets. **d–f**, Depict the fabrication procedure of the SiNW FET, contacted by symmetric S/D electrode with the same metal, whereas **g** shows the typical SEM image after the deposition of S/D electrodes upon 3 parallel SiNWs. **h, i**, present, respectively, the transfer characteristics of the FETs, built upon phosphorus-doped n-type or indium-doped p-type SiNW channels. Abbreviations: FET, field-effect transistor; IPSLS, in-plane solid-liquid-solid; SEM, scanning electron microscopy; SiNW, silicon nanowire; S/D, source/drain.

typical I_{ds}–V_{ds} output characteristic of the SiNW R-FET is presented in Fig. 3b, together with a schematic energy profile shown in the inset, where due to the large work function difference between the Ti/Al contact at ~4.3 eV and the p-type SiNW channel at ~5.1 eV, a relatively large SB (~0.8 eV) was formed at the drain/SiNW contact. In comparison, the Pt/Au electrode has a deeper work function at ~5.15 eV close to the valence band top of c-SiNW and thus forms a quasi-Ohmic contact at the source electrode. Under positive channel bias, the transport current can be turned on $V_{ds} > 3.8$ V due to the exponential increase of tunneling current through the thinning SB region, as indicated in the inset of Fig. 3b.

Interestingly, with a positive channel bias of $V_{ds} > 0$ V, a p-type metal–oxide–semiconductor (PMOS)-like transfer characteristic has been observed in the SiNW-FET, as shown in Fig. 3c. This can be understood with the asymmetric band profile depicted in Fig. 3e, where the hole carriers tend to inject from the Ti/Al drain electrode to the Pt/Au source electrode, under a positive channel bias, by tunneling through the triangle SB. When applying a negative gating voltage, the energy band of the SiNW channel will not only be drawn up, leading to an increase of the SB barrier height, but also make this triangle barrier become thinner that greatly facilitates the hole tunneling. Note that, considering that the large energy discrepancy of work function between Pt/Au electrodes and the conduction band bottom is roughly > 1 eV, the injection of minority electrons from the Pt/Au source electrodes into the p-type SiNWs is strongly suppressed and negligible, under the situation as schematically depicted in Fig. 3e. On the contrary, when applying a positive gating bias, it will lower the SB height but make it thicker, and that will suppress the hole tunneling current. Therefore, when the charge carrier of hole tends to flow from the drain to the source under a positive channel bias, via a tunneling injection from the metal drain electrode, the SiNW FET demonstrates a PMOS behavior as witnessed indeed in the transfer characteristics shown in Fig. 3c.

When the channel bias is reversed to be negative, that is, $V_{ds} < 0$ V, the holes tend to be injected from the source electrode and thus need to climb over the large SB, from the SiNW side into the drain electrode, via a thermionic emission (instead of tunneling). In this situation, a negative gating voltage will not only increase the SB height but also push the hole in the SiNW channel further away from the SB junction, which thus will suppress the thermionic emission, as depicted in Fig. 3f by the purple-line band profile. On the contrary, when applying a positive gating voltage, it will reduce the SB height, which is beneficial for the thermal emission of holes over the SB and thus turn on the transport current. So, under a negative channel bias, the SiNW FET will behave as an n-type metal–oxide–semiconductor (NMOS) device, as seen indeed from the transfer characteristics shown in Fig. 3d.

In addition, the threshold voltages in both the NMOS and PMOS modes are found to shift under different channel biases of V_{ds}, which is similar to the drain-induced barrier-lowering (DIBL) effect in conventional MOSFETs. However, the threshold shifting observed here is related to the fact that the thickness of the SB can be reduced under

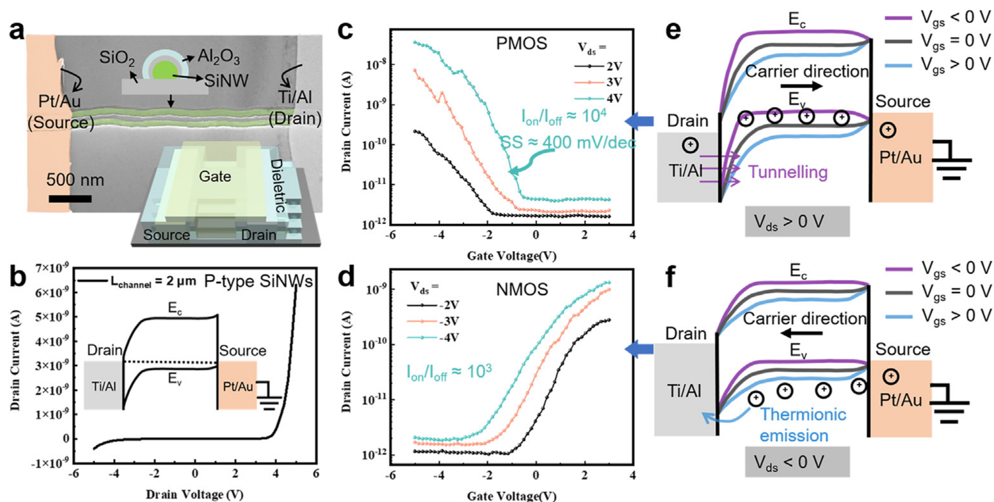

Fig. 3 | Reconfigurable FET (R-FET) built on In-doped p-type SiNW channels. **a**, The SEM image and schematic diagram of the R-FET, with a p-type SiNW channel contacted by asymmetric source-drain metal electrodes of Ti/Al@drain and Pt/Au@source (GND). **b**, A typical output characteristic of the R-FET with an energy band diagram for $V_{ds} = 0$ V and $V_{gs} = 0$ V. **c**, **d**, The transfer characteristics of the R-FET working in PMOS and NMOS modes under channel bias of $V_{ds} > 0$ V and $V_{ds} < 0$ V, respectively, whereas **e** and **f** diagram the variations of the band-gap profiles, as well as the different hole carrier injection direction/mechanisms, under different gating voltages, for the PMOS and NMOS modes, respectively. Abbreviations: FET, field-effect transistor; NMOS, n-type metal−oxide−semiconductor; PMOS, p-type metal−oxide−semiconductor; SiNW, silicon nanowire.

increased V_{ds} bias, making it more transparent for the holes to tunnel through, and thus leading to a right-shifting of threshold voltage as seen for example in Fig. 3c. Despite of this slightly different underlying mechanism, this phenomenon can also be regarded as a special kind of DIBL effect, which will limit the scalability of the SB-FETs. A better solution to this issue is to adopt a more advanced gate-all-around FET configuration, which is known to offer the strongest electrostatic control to counter the short-channel effect.

In comparison, the R-FET working in PMOS mode (under $V_{ds} > 0$ V) demonstrates a higher on current of $>10^{-8}$ A, a higher $I_{on/off} > 10^4$ and a steeper SS ~ 400 mV/dec than that achieved under NMOS-mode FET (under $V_{ds} < 0$ V), while both of them achieve a low off current down to ~pA. These different transfer behaviors could be assigned to the fact that the tunneling injection through the triangle SB in PMOS mode is exponentially dependent on the SB thickness, which can be efficiently controlled and tuned by the applied gating voltage (Fig. 3e) in PMOS mode, compared to the thermal emission injection in NMOS mode.

In order to further testify the potential or the universality of this asymmetric contact strategy for building R-FET, the same asymmetric source-drain electrodes have been fabricated upon a phosphorus-doped n-type SiNW channel, with a channel length of approximately 460 nm defined by using electron beam lithography, as shown in the SEM image of Fig. 4a. Similarly, a large SB (~1 eV) is supposed to form under the contact of Pt/Au to the n-type SiNW channel but now at the conduction band for the majority carriers of electrons (in contrast to the SB in valence band for holes in R-FET with p-type SiNW channel), while the contact at Ti/Al electrode becomes quasi-Ohmic due to the close alignment of the work functions of the source electrode with the n-type SiNW. Asymmetric output characteristic is indeed obtained and shown in Fig. 4b, with an energy band diagram shown in the insert. When a negative channel bias was applied to Pt/Au, the transport current can be turned on $V_{ds} < -2$ V, which is also ascribed the exponential increase of tunneling current through the sharper SB region.

In analogy to the previous analysis, when a positive channel bias $V_{ds} > 0$ V is applied, a PMOS-like transfer characteristic has been observed in the R-FET with n-type SiNW channel, as shown in Fig. 4c. However, according to the asymmetric band profile depicted in Fig. 4e, it is the major carrier of electrons that moved in the direction from source to drain electrodes that need to climb over the large SB via a thermionic emission process. So, in this situation, a positive gating voltage will increase the SB height, propel the electrons away from the SB, and thus suppress the thermionic emission current, as highlighted in Fig. 4e by the band profile in blue. On the contrary, when a negative gating voltage is applied, it will reduce the SB height, boost the thermionic emission, and thus turn on the transport current of electrons. In this way, under a positive channel bias, the SiNW FET will behave as a PMOS device, as observed indeed from the transfer characteristics shown in Fig. 4c.

When the channel bias V_{ds} is reversed to be negative, the electrons tend to be injected from the drain electrode into the channel via a tunneling through the thinning triangle SB region rather than the thermionic emission. Under this situation, a negative gating voltage will not only draw up the band of the whole SiNW channel, leading to a decrease of the SB barrier height, but also make it thicker, and that will suppress the electrons tunneling current. Reversely, a positive gating bias now will make the energy band bend downward further, which will not only increase the SB height but also make it much thinner to quickly turn on the electrons tunneling current. Therefore, under this negative-channel-bias situation, the SiNW FET demonstrates a NMOS-like behavior, as shown in Fig. 4d.

Remarkably, the R-FET devices with n-type SiNW channels can achieve a much higher on/off current modulation of $> 10^6$, two orders' magnitude higher than that achieved in p-type SiNW channels, while the off current is also reduced to approaching 0.1 pA. Similarly, the FET in NMOS mode with tunneling electron injection demonstrates a better performance than that in PMOS mode with thermionic injection; particularly, the NMOS-like device achieves an excellent on/off current ratio of $> 10^6$ and a rather steep SS of ~79 mV/dec under channel bias $V_{ds} = -3$ V.

It is also noteworthy that the on currents for these specific R-FETs working in NMOS and PMOS modes are not always matched, particularly for the devices demonstrated in Fig. 3, which could be a critical

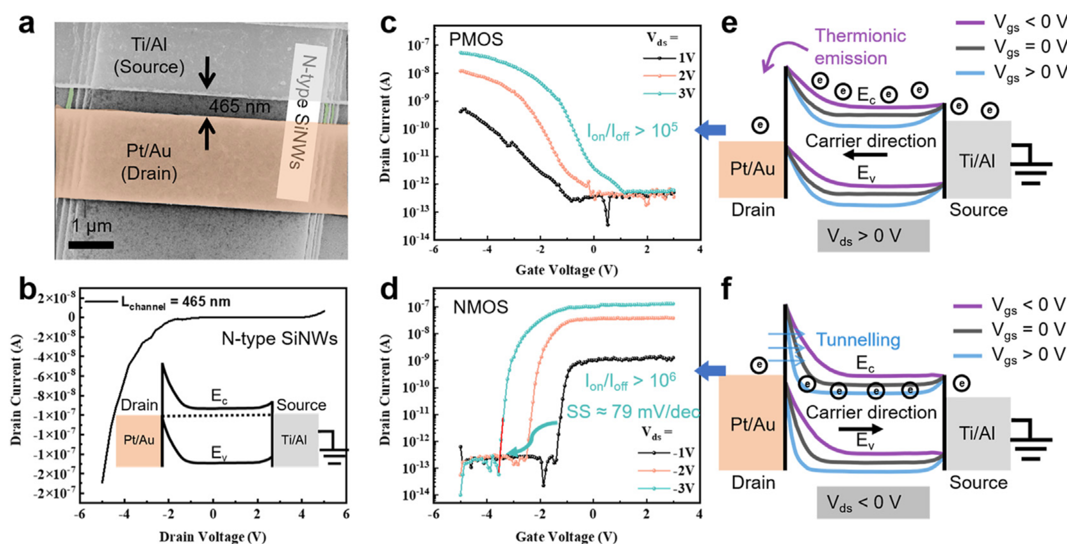

Fig. 4 | Reconfigurable FET (R-FET) built on phosphorus-doped n-type SiNW channels. **a**, The false-colored SEM image of the R-FET, with an n-type SiNW channel contacted by asymmetric source-drain metal electrodes of Ti/Al@Source (GND) and Pt/Au@Drain. **b**, A typical output characteristic of the R-FET with an energy band diagram for $V_{ds} = 0$ V & $V_{gs} = 0$ V. **c**, **d**, The transfer characteristics of the R-FET working in PMOS and NMOS modes under channel bias of $V_{ds} > 0$ V and $V_{ds} < 0$ V, respectively, whereas **e** and **f** diagram the variations of the band gap profile, as well as the different electron carrier injection direction/mechanisms, under different gating voltage, for the PMOS and NMOS modes, respectively. Abbreviations: FET, field-effect transistor; NMOS, n-type metal–oxide–semiconductor; PMOS, p-type metal–oxide–semiconductor; SEM, scanning electron microscopy; SiNW, silicon nanowire.

issue for the construction of CMOS logics. In principle, this issue can be addressed via 1) a fine-tuning of the work function of the SiNW channel, which is possible as a continuously tunable p-/n-doping control has been demonstrated in our previous work[45] or 2) the work function of electrode contacts can also be modified by choosing different metal or alloy S/D electrodes. Both of these approaches will allow one to effectively adjust the SB heights at the S/D electrodes and thus balance the injection and emission of the electron and hole carriers.

CONCLUSIONS

In summary, a rather simple asymmetric contact strategy has been established to fabricate single-gate R-FET logic solely controlled by altering the sign of the channel bias of V_{ds}, without the need of any extra PGs and high-precision gate-interface alignment, based on orderly SiNW channels grown via an IPSLS mechanism. This channel-bias-controlled R-FET strategy has been successfully testified on both the p-type- or n-type-doped SiNW channels and demonstrate an impressive high $I_{on/off}$ ratio of > 10^6 and a steep *SS* of 79 mV/dec. These results indicate a rather convenient and compact approach to implement R-FETs based on the beneficial catalytic SiNW channels for exploring a new generation of programmable and low-power logics and memories.

METHODS

Substrate preparation and guided edges formation wafer Substrates with 500 nm SiO_2 were cleaned by using acetone, isopropanol, and deionized water in ultrasonic for 5, 5, and 3 min, respectively. For oblique sidewall terrace formation, photoresistor (AZ5214) stripes of 3 μm wide and 1.8 μm thickness were patterned upon the substrates, followed by a cyclic plasma etching in inductively coupled plasma (ICP) system that alternated anisotropic C_4F_8 plasma (1.8 mTorr, 40 W, 50s) and isotropic O_2 plasma (30.1 mTorr, 50 W, 80 s) for 3 times to form oblique sidewall terrace with of 3 mini-steps. The O_2 plasma can erode the photoresistor to retreat and expose the underlying oxide layer.

Guided growth of SiNWs along the terrace The samples were first loaded into a PECVD system for H_2 plasma treatment (100 sccm, 140 Pa, 40 W) to reduce the surface oxide layer of the In stripes @250 °C (higher than the melting point of In, ~157 °C), and transferred them into discrete In droplets. Then, after cooling the substrate to ~100 °C below the melting point of In droplets, a thin film of a-Si precursor layer of ~15 nm thickness was coated by using silane plasma (10 sccm, 20 Pa, 20 W). Upon annealing at 350 °C in vacuum, the In droplets became molten again and started to absorb the a-Si precursor layer and precipitate crystalline SiNWs along the guiding steps. At the end of the SiNW growth, the remnant a-Si precursor film was selectively etched off by using CF_4 plasma (30 sccm, 4 Pa, 8 W) in reactive ion etching (RIE) system, followed by an O_2 plasma (10 sccm, 3 Pa, 40 W) to remove the produced carbon-compound resultant.

N-doped a-Si precursor For the pre-doping in a-Si layer, a mixture of PH_3 (2% diluted in H_2) and SiH_4 gases was used to add phosphorus atoms into the a-Si layer, which can reverse the doping polarity to n-type. In this work, a mixture gas of PH_3 (0.6 sccm, 20 Pa, 20 W) and SiH_4 (6 sccm, 20 Pa, 20 W) was used to deposit n-doped a-Si layer @100 °C, and then produce the n-type SiNWs with phosphorus atoms concentration of ~6×10^{19} cm^{-3}.

REFERENCES

1. Wanlass, F. & Sah, C. Nanowatt logic using field-effect metal-oxide semiconductor triodes. In *1963 IEEE International Solid-State Circuits Conference. Digest of Technical Papers,* 32–33 (IEEE, 1963). https://doi.org/10.1109/ISSCC.1963.1157450.

2. Ghani, T. et al. A 90 nm high volume manufacturing logic technology featuring novel 45 nm gate length strained silicon CMOS transistors. In *2003 IEEE International Electron Devices Meeting*, 11.6.1−11.6.3 (IEEE, 2003). https://doi.org/10.1109/IEDM.2003.1269442.
3. Wang, D., Sheriff, B. A. & Heath, J. R. Complementary symmetry silicon nanowire logic: power-efficient inverters with gain. *Small* **2**, 1153−1158 (2006). https://doi.org/10.1002/smll.200600249.
4. Rustagi, S. C. et al. CMOS inverter based on gate-all-around silicon-nanowire MOSFETs fabricated using top-down approach. *IEEE Electron Device Lett.* **28**, 1021−1024 (2007). https://doi.org/10.1109/Led.2007.906622.
5. Van, N. H. et al. High performance Si nanowire field-effect-transistors based on a CMOS inverter with tunable threshold voltage. *Nanoscale* **6**, 5479−5483 (2014). https://doi.org/10.1039/c3nr06690h.
6. Lin, H. C., Yeh, K. L., Huang, R. G., Lin, C. Y. & Huang, T. Y. Schottky barrier thin-film transistor (SBTFT) with silicided source/drain and field-induced drain extension. *IEEE Electron Device Lett.* **22**, 179−181 (2001). https://doi.org/10.1109/55.915606.
7. Zhang, D., Chow, T. & Wong, M. A polycrystalline silicon thin-film transistor with self-aligned metal electrodes formed using aluminum-induced crystallization. *IEEE Trans. Electron Devices* **55**, 2181−2186 (2008). https://doi.org/10.1109/Ted.2008.926742.
8. Wessely, F., Krauss, T. & Schwalke, U. CMOS without doping: multi-gate silicon-nanowire field-effect-transistors. *Solid-State Electron* **70**, 33−38 (2012). https://doi.org/10.1016/j.sse.2011.11.011.
9. Heinzig, A., Mikolajick, T., Trommer, J., Grimm, D. & Weber, W. M. Dually active silicon nanowire transistors and circuits with equal electron and hole transport. *Nano Lett.* **13**, 4176−4181 (2013). https://doi.org/10.1021/nl401826u.
10. Zhang, J., Tang, X. F., Gaillardon, P.-E. & De Micheli, G. Configurable circuits featuring dual-threshold-voltage design with three-independent-gate silicon nanowire FETs. *IEEE Trans. Circuits Syst. I: Regul. Pap.* **61**, 2851−2861 (2014). https://doi.org/10.1109/Tcsi.2014.2333675.
11. Wind, L. et al. Nanoscale reconfigurable Si transistors: from wires to sheets and unto multi-wire channels. *Adv. Electron. Mater.* **10**, 2300483 (2024). https://doi.org/10.1002/aelm.202300483.
12. Simon, M. et al. Top-down fabricated reconfigurable FET with two symmetric and high-current on-states. *IEEE Electron Device Lett.* **41**, 1110−1113 (2020). https://doi.org/10.1109/Led.2020.2997319.
13. Yang, X. & Mohanram, K. Modeling and performance investigation of the double-gate carbon nanotube transistor. *IEEE Electron Device Lett.* **32**, 231−233 (2011). https://doi.org/10.1109/Led.2010.2095826.
14. Lu, G. T. et al. Reconfigurable tunneling transistors heterostructured by an individual carbon nanotube and MoS_2. *Nano Lett.* **21**, 6843−6850 (2021). https://doi.org/10.1021/acs.nanolett.1c01833.
15. Chang, Y.-M. et al. Reversible and precisely controllable p/n-Type doping of $MoTe_2$ transistors through electrothermal doping. *Adv. Mater.* **30**, 1706995 (2018). https://doi.org/10.1002/adma.201706995.
16. Sun, X. et al. Reconfigurable logic-in-memory architectures based on a two-dimensional van der Waals heterostructure device. *Nat. Electron.* **5**, 752−760 (2022). https://doi.org/10.1038/s41928-022-00858-z.
17. Peng, R. et al. Programmable graded doping for reconfigurable molybdenum ditelluride devices. *Nat. Electron.* **6**, 852−861 (2023). https://doi.org/10.1038/s41928-023-01056-1.
18. Rodriguez-Andina, J. J., Moure, M. J. & Valdes, M. D. Features, design tools, and application domains of FPGAs. *IEEE Trans. Ind. Electron.* **54**, 1810−1823 (2007). https://doi.org/10.1109/Tie.2007.898279.
19. Rai, S. et al. Designing efficient circuits based on runtime-reconfigurable field-effect transistors. *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.* **27**, 560−572 (2019). https://doi.org/10.1109/Tvlsi.2018.2884646.
20. Bae, J.-H. et al. Reconfigurable field-effect transistor as a synaptic device for XNOR binary neural network. *IEEE Electron Device Lett.* **40**, 624−627 (2019). https://doi.org/10.1109/Led.2019.2898448.
21. Pan, C. et al. Reconfigurable logic and neuromorphic circuits based on electrically tunable two-dimensional homojunctions. *Nat. Electron.* **3**, 383−390 (2020). https://doi.org/10.1038/s41928-020-0433-9.
22. Heinzig, A., Slesazeck, S., Kreupl, F., Mikolajick, T. & Weber, W. M. Reconfigurable silicon nanowire transistors. *Nano Lett.* **12**, 119−124 (2011). https://doi.org/10.1021/nl203094h.
23. Mongillo, M., Spathis, P., Katsaros, G., Gentile, P. & De Franceschi, S. Multifunctional devices and logic gates with undoped silicon nanowires. *Nano Lett.* **12**, 3074−3079 (2012). https://doi.org/10.1021/nl300930m.
24. Park, S. J. et al. Reconfigurable Si nanowire nonvolatile transistors. *Adv. Electron. Mater.* **4**, 1700399 (2018). https://doi.org/10.1002/aelm.201700399.
25. Jeon, D.-Y., Park, S. J., Pregl, S., Mikolajick, T. & Weber, W. M. Reconfigurable thin-film transistors based on a parallel array of Si-nanowires. *J. Appl. Phys.* **129**, 124504 (2021). https://doi.org/10.1063/5.0036029.
26. Cui, Y., Zhong, Z., Wang, D., Wang, W. U. & Lieber, C. M. High performance silicon nanowire field effect transistors. *Nano Lett.* **3**, 149−152 (2003). https://doi.org/10.1021/nl025875l.
27. Weber, W. M. et al. Silicon nanowires: catalytic growth and electrical characterization. *Phys. Status Solidi* (B) **243**, 3340−3345 (2006). https://doi.org/10.1002/pssb.200669138.
28. Wong, W. S., Raychaudhuri, S., Lujan, R., Sambandan, S. & Street, R. A. Hybrid Si nanowire/amorphous silicon FETs for large-area image sensor arrays. *Nano Lett.* **11**, 2214−2218 (2011). https://doi.org/10.1021/nl200114h.
29. Yu, L. W., Alet, P.-J., Picardi, G. & Cabarrocas, P.R. I. An in-plane solid-liquid-solid growth mode for self-avoiding lateral silicon nanowires. *Phys. Rev. Lett.* **102**, 125501 (2009). https://doi.org/10.1103/PhysRevLett.102.125501.
30. Yu, L. & Cabarrocas, P.R. I. Initial nucleation and growth of in-plane solid-liquid-solid silicon nanowires catalyzed by indium. *Phys. Rev. B* **80**, 085313 (2009). https://doi.org/10.1103/PhysRevB.80.085313.
31. Yu, L., Oudwan, M., Moustapha, O., Fortuna, F. & Cabarrocas, P.R. I. Guided growth of in-plane silicon nanowires. *Appl. Phys. Lett.* **95**, 113106 (2009). https://doi.org/10.1063/1.3227667.
32. Yu, L. et al. Growth-in-place deployment of in-plane silicon nanowires. *Appl. Phys. Lett.* **99**, 203104 (2011). https://doi.org/10.1063/1.3659895.
33. Yu, L. & Cabarrocas, P.R. I. Growth mechanism and dynamics of in-plane solid-liquid-solid silicon nanowires. *Phys. Rev. B* **81**, 085323 (2010). https://doi.org/10.1103/PhysRevB.81.085323.
34. Yu, L. & Cabarrocas, P.R. I. Morphology control and growth dynamics of in-plane solid-liquid-solid silicon nanowires. *Phys. E: Low-Dimens. Syst. Nanostructures* **44**, 1045−1049 (2012). https://doi.org/10.1016/j.physe.2011.06.005.
35. Zhang, J., Gaillardon, P.-E. & De Micheli, G. Dual-threshold-voltage configurable circuits with three-independent-gate silicon nanowire FETs. In *2013 IEEE International Symposium on Circuits and Systems (ISCAS)*, 2111−2114 (IEEE, 2013). https://doi.org/10.1109/ISCAS.2013.6572291.
36. Zhang, J., De Marchi, M., Gaillardon, P. E. & De Micheli, G. A. Schottky-barrier silicon FinFET with 6.0 mV/dec subthreshold slope over 5 decades of current. In *2014 IEEE International Electron Devices Meeting*, 13.4.1−13.4.4 (IEEE, 2014). https://doi.org/10.1109/IEDM.2014.7047045.
37. Hu, R. et al. Unprecedented uniform 3D growth integration of 10-layer stacked Si nanowires on tightly confined sidewall grooves. *Nano Lett.* **20**, 7489−7497 (2020). https://doi.org/10.1021/acs.nanolett.0c02950.
38. Hu, R. et al. Ultra-confined catalytic growth integration of sub-10 nm 3D stacked silicon nanowires via a self-delimited droplet formation strategy. *Small* **18**, 2204390 (2022). https://doi.org/10.1002/smll.202204390.
39. Qian, W. et al. Converging-guiding-track design enables 100% growth deployment rate of ultrathin monocrystalline silicon nanowire channels. *Appl. Phys. Lett.* **122**, 173101 (2023). https://doi.org/10.1063/5.0142492.
40. Xu, M. et al. Operating principles of in-plane silicon nanowires at simple step-edges. *Nanoscale* **7**, 5197−5202 (2015). https://doi.org/10.1039/c4nr06531j.
41. Xu, M. et al. High performance transparent in-plane silicon nanowire Fin-TFTs via a robust nano-droplet-scanning crystallization dynamics. *Nanoscale* **9**, 10350−10357 (2017). https://doi.org/10.1039/c7nr02825c.
42. Xue, Z. et al. Deterministic line-shape programming of silicon nanowires for extremely stretchable springs and electronics. *Nano Lett.* **17**, 7638−7646 (2017). https://doi.org/10.1021/acs.nanolett.7b03658.
43. Wu, X. et al. 3D sidewall integration of ultrahigh-density silicon nanowires for stacked channel electronics. *Adv. Electron. Mater.* **5**, 1800627 (2019). https://doi.org/10.1002/aelm.201800627.
44. Chen, W. et al. Incorporation and redistribution of impurities into silicon nanowires during metal-particle-assisted growth. *Nat. Commun.* **5**, 4134 (2014). https://doi.org/10.1038/ncomms5134.
45. Sun, Y. et al. Unexpected phosphorus doping routine of planar silicon nanowires for integrating CMOS logics. *Nanoscale* **13**, 15031−15037 (2021). https://doi.org/10.1039/d1nr03014k.
46. Xu, L. L., Wang, J., Liu, H. S. & Jin, Z. P. Thermodynamic assessment of the Pt-Si binary system. *Calphad* **32**, 101−105 (2008). https://doi.org/10.1016/j.calphad.2007.07.010.
47. Roy, S., Divinski, S. V. & Paul, A. Reactive diffusion in the Ti−Si system and the significance of the parabolic growth constant. *Philos. Mag.* **94**, 683−699 (2013). https://doi.org/10.1080/14786435.2013.859759.

MISCELLANEA

Acknowledgments The authors acknowledge the financial supports received from the National Key Research Program of China under granted No. 92164201, National Natural Science Foundation of China for Distinguished Young Scholars No. 62325403, National Natural Science Foundation of China under Nos. 62104100 and 61921005, and 61974064.

Author contributions Linwei YU: Writing—review and editing, Writing—original draft, Visualization, Validation, Supervision, Resources, Project administration, Methodology, Investigation, Funding acquisition, Formal analysis, Data curation, Conceptualization. Jun Xu: Writing—review and editing, Resources, Funding acquisition. Junzhuan Wang: Writing—review and editing, Project administration, Investigation, Funding acquisition, Data curation. Wentao Qian: Writing—original draft, Visualization, Validation, Methodology, Investigation, Formal analysis, Data curation, Conceptualization

Declaration of Competing Interest The authors declare no competing interests.

© 2024 The Author(s). Published by Elsevier B.V. on behalf of Shanghai Jiao Tong University. This is an open access article under the CC BY-NC-ND license (http://creativecommons.org/licenses/by-nc-nd/4.0/).