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Exceptionally Matched p-SiNW/n-IGZO Complementary Field-Effect Transistors for Monolithic 3D Logic

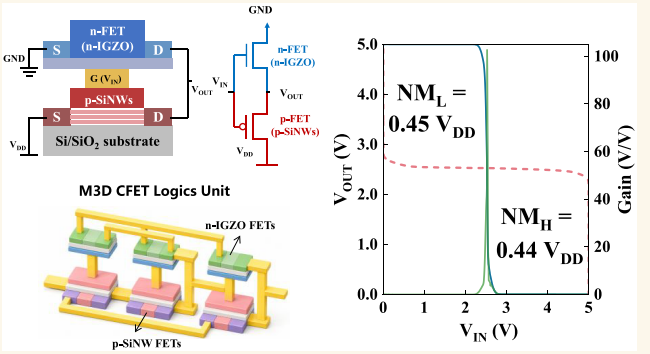
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ABSTRACT: Monolithic three-dimensional (M3D) complementary field-effect transistors (CFETs) provide a route toward a higher logic density by vertically stacking complementary devices within the same footprint. Their realization through heterogeneous integration requires p- and n-channel transistors that are both individually high-performing and electrically matched. Here, we demonstrate high-performance heterogeneous Si/oxide M3D CFETs by vertically integrating p-type silicon nanowire (p-SiNW) FETs with n-type indium gallium zinc oxide (n-IGZO) transistors. The site-controlled p-SiNWs are formed through a scalable in-plane solid−liquid−solid (IPSLS) process without postgrowth hydrogen passivation, facilitating subsequent oxide−semiconductor integration. The vertically integrated p- and n-channel devices exhibit closely matched current-driving capabilities, near-zero threshold voltages, and subthreshold swings of 120 and 133 mV dec^{-1}, respectively. This exceptional p/n matching enables sharp and well-balanced switching, yielding a peak voltage gain of 103 V/V at V_{DD} = 5 V, a normalized gain of 20.6 V^{-1}, and large, nearly symmetric noise margins (NM_L = 0.45 V_{DD} and NM_H = 0.44 V_{DD}). The architecture is further extended to NOR, NAND, and OR gates with experimentally verified logic operations. These results establish a high-performance heterogeneous Si/oxide integration platform for dense and robust M3D complementary logic.



KEYWORDS: *M3D integration, complementary FET (CFET), silicon nanowires, IGZO transistors, heterogeneous CMOS logic*

INTRODUCTION

The rapid growth of data-centric computing is driving an urgent demand for logic technologies with higher integration density,[1,2] lower power consumption,[3,4] and shorter interconnect delays.[5−7] Monolithic three-dimensional (M3D) integration addresses the limitations of conventional lateral scaling by sequentially fabricating and vertically interconnecting multiple active device tiers on a single wafer.[8−10] In particular, complementary field-effect transistor (CFET) architectures, in which p- and n-channel devices are vertically aligned within the same footprint, offer a promising route toward ultimate CMOS density scaling.[11−14] Their practical implementation, however, requires a high-performance p-channel technology that is simultaneously compatible with low-temperature processing, large-area manufacturing, and close vertical integration with n-type oxide transistors.[15−19]

Heterogeneous integration offers an attractive strategy for M3D CFETs by combining semiconductor materials with complementary electronic advantages. Oxide semiconductors, particularly indium gallium zinc oxide (IGZO), are promising n-channel materials because of their high on/off current ratios, low off-state currents, and compatibility with low-temperature and large-area fabrication.[20−23] However, high-performance complementary logic requires not only strong individual devices but also close p−n electrical matching. Well-aligned threshold voltages, subthreshold characteristics, and current-driving capabilities are essential for sharp switching and a high voltage gain. P-type oxides generally suffer from limited carrier transport, whereas emerging low-dimensional semiconductors, including tellurium-based materials and carbon nanotubes, often involve complex material synthesis, transfer, or high-resolution patterning.[24−27] Meanwhile, hydrogen released from low-temperature polycrystalline silicon (LTPS) can diffuse into oxide semiconductors, degrading their electrical performance and stability. Consequently, hydrogen-related process incompatibility represents a hidden integration ceiling on vertically stacked 3D Si/oxide logic.[28−30]

Silicon nanowires (SiNWs) offer strong electrostatic control and dimensional scalability, but their integration into M3D

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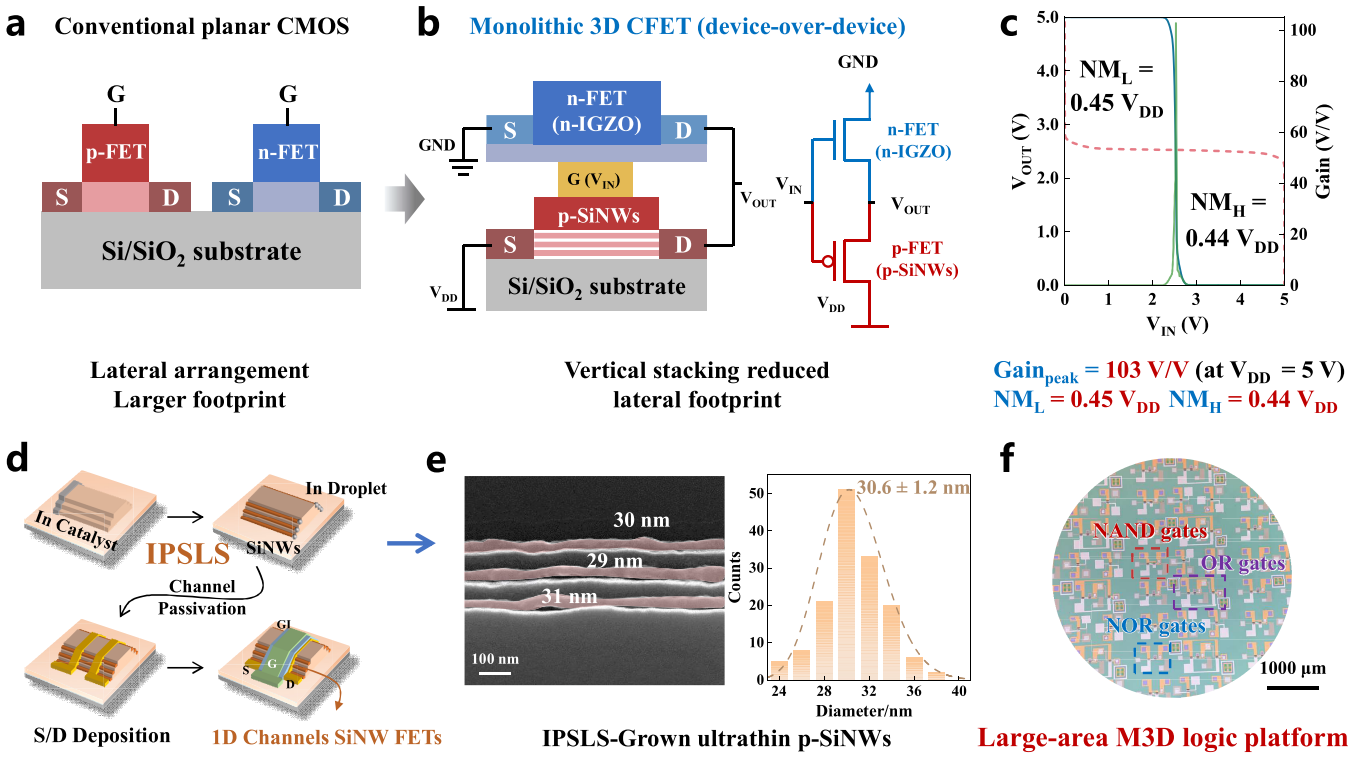


Figure 1. Heterogeneous p-SiNW/n-IGZO platform for monolithic 3D complementary logic. (a) Schematic comparison between conventional planar CMOS with laterally arranged p- and n-channel transistors. (b) Schematic of the device-over-device p-SiNW/n-IGZO M3D CFET inverter, consisting of a bottom-tier p-SiNW FET and a top-tier n-IGZO transistor with shared input and output nodes. (c) Voltage-transfer and gain characteristics of the M3D CFET inverter. (d) Schematic fabrication process of IPSLS-grown p-SiNW FETs. (e) Scanning electron microscope (SEM) image and diameter distribution of IPSLS-grown ultrathin p-SiNWs. (f) Large-area layout of the M3D complementary logic platform integrating NAND, NOR, and OR gates.

electronics requires a growth and fabrication scheme that is compatible with sequential processing. In-plane solid−liquid−solid (IPSLS) growth enables ordered, site-controlled SiNW arrays to be formed through a lithography-compatible process, providing a scalable route to high-performance p-type SiNW FETs. Importantly, the SiNW channels do not require postgrowth hydrogen passivation, facilitating subsequent oxide−semiconductor integration by minimizing hydrogen-induced degradation in IGZO.[31,32] The combination of strong SiNW electrostatics[33] and reduced hydrogen-related process incompatibility[34,35] therefore provides a compelling p-channel solution for heterogeneous Si/oxide M3D integration.[36,37] The p-SiNW/n-IGZO material combination enables well-balanced complementary characteristics while supporting a sequential vertical integration. Moreover, the site-controlled SiNW growth and sputter-deposited IGZO are compatible with large-area, array-level fabrication, offering a practical route to heterogeneous M3D integration. Here, we vertically integrate p-SiNW FETs with n-IGZO transistors to realize M3D CFETs with closely matched current-driving capabilities and subthreshold swings (SS) of 120 and 133 mV dec^{-1}, respectively. This excellent p/n matching enables a high inverter gain with a large value of 103 V/V and nearly symmetric noise margins of NM_L = 0.45 V_{DD} and NM_H = 0.44 V_{DD}. This architecture is further extended to NOR, NAND, and OR gates, establishing a high-performance heterogeneous Si/oxide platform for scalable M3D complementary logic.[38,39]

RESULTS AND DISCUSSION

Figure 1 presents the concept, device architecture, and scalable implementation of the heterogeneous p-SiNW/n-IGZO M3D CFET platform. As illustrated in Figure 1a, conventional planar CMOS places the p- and n-channel transistors laterally on the same substrate, resulting in a relatively large lateral footprint. In contrast, the M3D CFET architecture vertically stacks the complementary devices in a device-over-device configuration, substantially reducing the lateral footprint. Figure 1b shows the proposed heterogeneous CFET inverter, in which the p-SiNW FET forms the bottom tier and the n-IGZO transistor is monolithically integrated above it. The two devices share the input and output nodes, forming a vertically integrated complementary inverter. Owing to the high performance and close p/n matching, the inverter achieves a peak gain of 103 V/V at V_{DD} = 5 V and nearly symmetric noise margins of 0.45 V_{DD} and 0.44 V_{DD} (Figure 1c).

The bottom-tier p-type devices are enabled by the IPSLS growth of site-controlled SiNWs, as schematically illustrated in Figure 1d. Multistep guiding trenches are first patterned on a silicon oxide substrate to define the lateral growth direction of SiNWs. A thin indium (In) catalyst layer (~5 nm) is then deposited on one side of the patterned steps and treated by H_2 plasma in a PECVD chamber at 250 °C to form discrete catalytic droplets. After depositing an amorphous Si (a-Si) precursor layer (~9 nm) at 100 °C, the substrate is annealed at ~300 °C under vacuum, during which the molten In droplets absorb the surrounding a-Si along the guiding trenches and crystallize well-aligned SiNWs. The source/drain, gate

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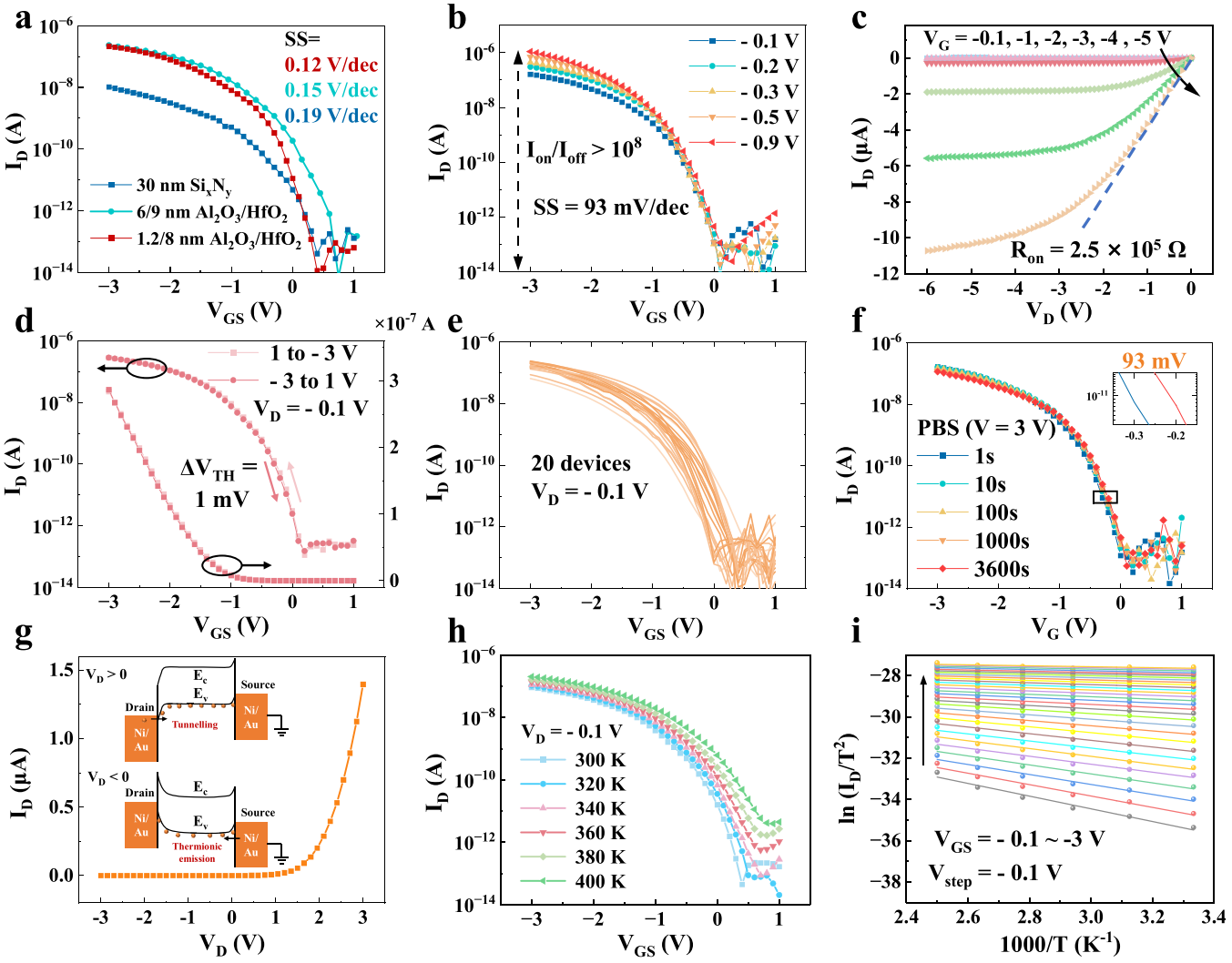


Figure 2. Electrical characteristics of p-SiNW FETs. (a) Comparison of p-SiNW FETs with different gate dielectrics. (b) Transfer characteristics measured under different V_D. (c) Output characteristics of the p-SiNW FET under different V_{GS}. (d) Hysteresis transfer characteristics of the p-SiNW FET. (e) Transfer characteristics of 20 p-SiNW FETs. (f) Positive-bias stress at 3 V for 3600 s. (g) Output characteristics of the p-SiNW FET with schematic band diagrams illustrating the Ni/Au-SiNW Schottky contact. (h) Temperature-dependent transfer characteristics measured at V_D = −0.1 V. (i) Arrhenius plots of ln (I_D/T^2) versus 1000/T at different V_{GS} values based on the thermionic emission model.

dielectric, and gate electrode were subsequently deposited to complete the p-SiNW FETs. The resulting SiNWs exhibit uniform ultrathin dimensions, with representative diameters of approximately 30 nm and a statistical average of 30.6 ± 1.2 nm (Figure 1e). Combined with lithography-compatible device fabrication and subsequent n-IGZO integration, the approach enables large-area implementation of vertically integrated complementary circuits. Figure 1f shows the large-area M3D logic platform containing NAND, NOR, and OR gates, demonstrating the scalability of the heterogeneous Si/oxide architecture from individual CFETs to integrated complementary logic.[40−42]

Figure 2a compares p-SiNW FETs with different gate dielectrics, including 1.2/8 nm Al_2O_3/HfO_2, 6/9 nm Al_2O_3/HfO_2, and 30 nm Si_xN_y. A 60 nm-thick nickel (Ni) metal gate is employed to modulate the channel conductance, with 15/30 nm nickel/gold (Ni/Au) bilayers functioning as the source and drain (S/D) contacts. The three devices exhibit subthreshold swings (SS) of 0.12, 0.15, and 0.19 V dec^{-1}, respectively. Compared with the FET employing Si_xN_y as the gate dielectric, the devices with high-k Al_2O_3/HfO_2 gate dielectrics deliver higher on-state currents (I_{ON}). Moreover, reducing the thickness of the Al_2O_3/HfO_2 dielectric stack results in a steeper subthreshold transition and sharper device turn-on. The higher dielectric constant and reduced dielectric thickness increase the gate capacitance, allowing more direct modulation of the channel barrier. Figure 2b shows the representative transfer characteristics measured at different drain voltages (V_D) of a SiNW FET employing the 1.2/8 nm Al_2O_3/HfO_2 gate dielectric stack. The device exhibits effective gate modulation, with a minimum SS of 93 mV dec^{-1} at V_D = −0.2 V. As V_D becomes more negative, I_{ON} gradually increases, whereas off-state current (I_{OFF}) remains below 10^{-13} A, yielding a maximum I_{ON}/I_{OFF} exceeding 10^8. The weak dependence of I_{OFF} on drain bias indicates strong gate control over channel conduction, supporting robust switching for complementary logic applications. Figure 2c presents the output characteristics of the p-SiNW FET measured at gate voltages ranging from −0.1 to −5.0 V. As V_G becomes more negative, the magnitude of drain current (I_D) progressively increases, confirming the typical p-type gate-modulated behavior. At low |V_D|, I_D increases approximately linearly

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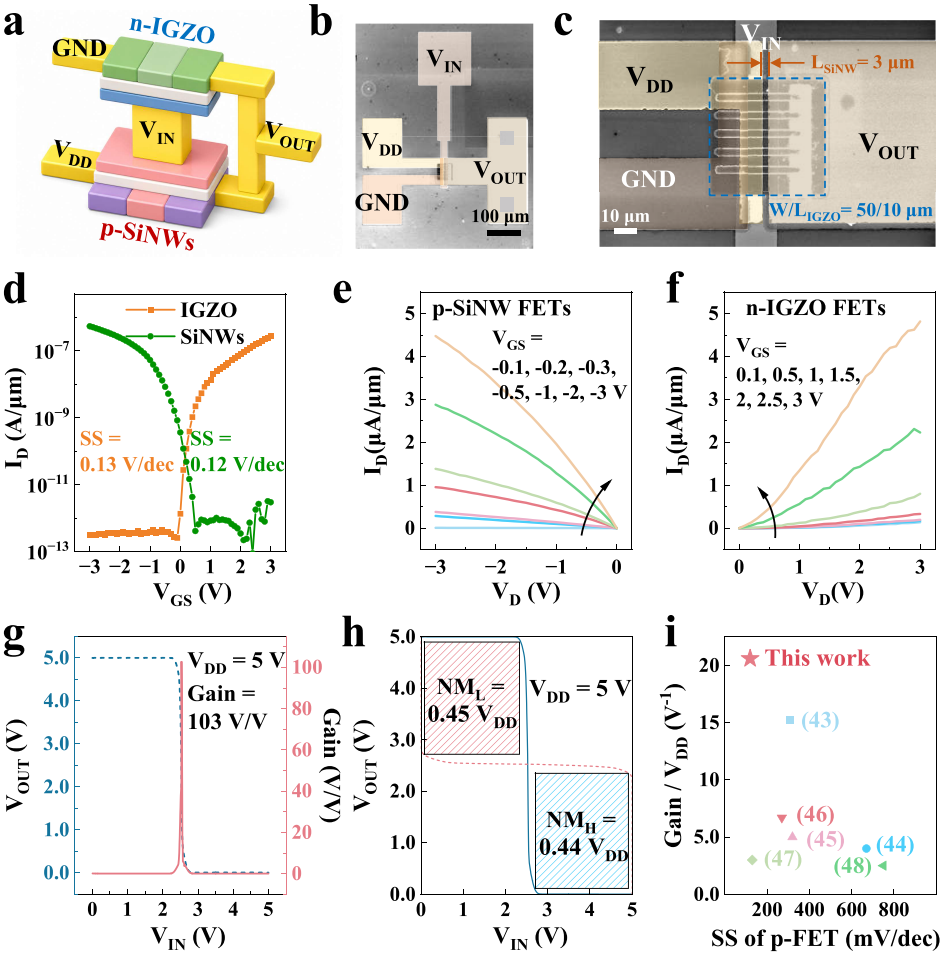


Figure 3. Electrical performance of the M3D p-SiNW/n-IGZO CFET inverter. (a) Schematic illustrations of the vertically stacked inverter. (b) SEM image of the fabricated M3D stacked inverter and (c) enlarged view of the stacked channel region. (d) Transfer characteristics of the p-SiNW and n-IGZO transistors extracted from the stacked inverter. Output characteristics of (e) p- and (f) n-channel devices. (g) Voltage transfer characteristics and voltage gain of the M3D stacked inverter, reaching a maximum value of 103 V/V at V_{DD} = 5 V. (h) Noise margin analysis at V_{DD} = 5 V, yielding NM_L = 0.45 V_{DD} and NM_H = 0.44 V_{DD}. (i) Performance comparison of BEOL-compatible p-type SiNW FETs for M3D CFET applications.

with V_D, indicating effective hole injection in the on-state. With increasing $|V_D|$, the I_D gradually approaches saturation, and a linear fit in the on-state yields an on-resistance of approximately 2.5×10^5 Ω.

Beyond their basic electrical characteristics, the p-SiNW FETs exhibit good hysteresis, device-to-device uniformity, and bias stability. The dual-sweep transfer characteristics in Figure 2d show a threshold voltage shift (ΔV_{TH}) of only 1 mV, indicating limited charge trapping at the SiNWs/high-k interface. Figure 2e compares 20 devices measured at V_D = −0.1 V, revealing highly uniform transfer characteristics with V_{TH} = −0.67 ± 0.05 V and SS = 128.7 ± 23.0 mV dec^{-1}, while the corresponding I_{ON} and I_{ON}/I_{OFF} are (1.73 ± 0.45) × 10^{-7} A and (1.19 ± 1.11) × 10^7, respectively, as statistically summarized in Figure S1. Under positive-bias stress (PBS) at V_G = 3 V, the ΔV_{TH} remains limited to 93 mV after 3600 s, as shown in Figure 2f. The corresponding negative bias stress (NBS) measurement in Figure S2 yields a shift of −138 mV, demonstrating exceptional bias stability under both stress polarities (Figure S3) and validating the high quality of the SiNW channel and interface.

To clarify the carrier transport mechanism and Schottky barrier modulation in IPSLS-grown p-type SiNW FETs, we analyzed the metal/SiNW contact and temperature-dependent electrical characteristics. Figure 2g illustrates the band alignment at the Ni/Au-SiNW contact. Because the work function of Ni (5.0 eV) is close to the valence-band edge of crystalline Si (5.17 eV), a finite Schottky barrier for holes is formed at the contact interface. Under positive channel bias, the drain-side barrier is sufficiently narrowed, allowing hole tunneling into the valence band of the SiNW and resulting in a rapid increase in drain current. In contrast, under a negative drain bias, hole injection is dominated by thermionic emission from the source-side contact, leading to a low reverse current of approximately 10^{-10} A. To further quantify the gate-controlled Schottky barrier, temperature-dependent transfer characteristics were measured at V_D = −0.1 V, as shown in Figure 2h. The I_D increases monotonically with temperature, accompanied by a pronounced rise in I_{OFF}, confirming the contribution of thermally activated hole emission. Conversely, the transfer characteristics measured at V_D = +0.1 V show negligible temperature dependence in the off-current regime (Figure S4), supporting that the transport is overwhelmingly governed by carrier tunneling. Based on the thermionic emission model, the temperature-dependent drain currents were replotted as Arrhenius curves of ln (I_D/T^2) versus 1000/

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Table 1. Performance Comparison of Representative Complementary Inverters for M3D Logic Integration

	this work	43	44	45	46	47	48
n-channel (method)	IGZO (Sputter)	IGZO (Sputter)	IGZO (ALD)	IGZO (Sputter)	IGZO (solution processed)	MoS_2 (CVD + EBL)	Bi_2S_3 (thermal evaporation)
p-channel (method)	SiNWs (IPSLS w/o EBL)	$Te_{0.8}Se_{0.2}$ (Sputter)	TeO_x (Sputter)	CNT (spin-coating)	CuSnX (solution processed)	WSe_2 (CVD + EBL)	Te (thermal evaporation)
SS (V/decade)	0.13 (n)	0.08 (n)	0.12 (n)	0.13 (n)	/ (n)	0.13 (n)	0.52 (n)
	0.12 (p)	0.31 (p)	0.67 (p)	0.32 (p)	0.27 (p)	0.13 (p)	0.75 (p)
gain (V/V)	103 (@5 V)	38 (@2.5 V)	12 (@3 V)	25 (@5 V)	20 (@3 V)	9 (@3 V)	~10 (@4 V)
gain/V_{DD} (V^{-1})	20.6	15.2	4	5	6.7	3	~2.5

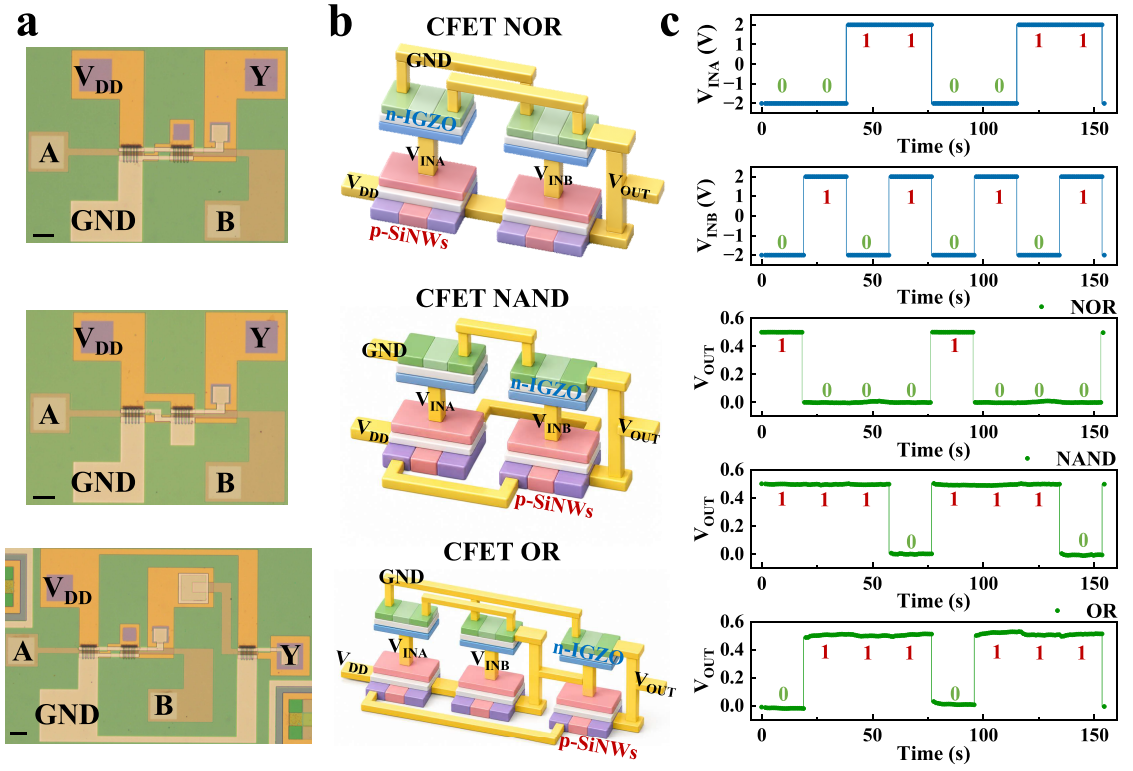


Figure 4. Monolithically integrated M3D p-SiNW/n-IGZO CFET logic gates. (a) Optical images and (b) schematic illustrations of the vertically stacked CFET NOR, NAND, and OR gates (scale bar: 50 μm). (c) Dynamic input and output voltage waveforms at V_{DD} = 0.5 V, confirming correct logic operation for all three M3D CFET gates.

T at different V_{GS} values (Figure 2i). The extracted Schottky barrier height varies linearly with V_{GS} (Figure S5), and the effective gate-modulated Schottky barrier height of 85 meV at V_{GS} = 0 V was obtained by extrapolation. Collectively, these results reveal a well-controlled Schottky contact and efficient gate modulation of the injection barrier, underscoring the potential of IPSLS-grown p-type SiNW FETs as robust building blocks for complementary logic and monolithic three-dimensional integration.

Building on the high-performance, hydrogen-free p-type SiNW FETs, we developed a vertically stacked Si/oxide CFET platform for M3D heterogeneous complementary logic integration. Figure 3a,b shows a schematic illustration and a representative SEM image of the fabricated M3D stacked inverter, respectively, while Figure 3c presents an enlarged view of the vertically stacked channel region. The top coplanar bottom-gate IGZO transistor has a channel width/length of 50/10 μm, while the underlying p-SiNW FET has a channel length of 3 μm. As detailed in Figure S6, the bottom-tier p-SiNW FET is first formed with a 1.2/8 nm Al_2O_3/ HfO_2 high-k gate stack and a Ni top gate, followed by deposition of a 9/6 nm HfO_2/Al_2O_3 bilayer as the gate dielectric for the top n-IGZO transistor. A via hole through the stacked dielectrics enables one Al source/drain electrode of the IGZO transistor to contact the bottom-tier electrode, forming the shared V_{OUT} node. Benefiting from the hydrogen-free fabrication of the underlying p-SiNW FET, the vertically integrated IGZO TFT is protected from hydrogen-induced degradation and retains high-performance characteristics, including a low SS of approximately 0.13 V dec^{-1} and an I_{ON}/I_{FF} exceeding 10^7. The device also maintains stable operation under ±3 V gate-bias stress, with ΔV_{TH} limited to −0.20 V under NBS and 0.29 V under PBS after 3600 s, as shown in Figure S7.

The intrinsic electrical characteristics of the complementary transistors extracted from the stacked inverter are summarized in Figure 3d–f. At $|V_D|$ = 0.1 V, the p-SiNW and n-IGZO devices exhibit closely matched on-state current densities, near-zero threshold voltages, and comparable subthreshold swings of 120 and 133 mV dec^{-1}, respectively (Figure 3d). Their output characteristics in Figure 3e,f further reveal similar current-driving capabilities over the measured bias range. These results demonstrate effective p/n codesign and electrical

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matching, providing the basis for symmetric switching, high voltage gain, and large noise margins. The resulting M3D stacked inverter exhibits clear logic inversion with a sharp transition at V_{DD} = 5 V, as shown in Figure 3g, and achieves a maximum voltage gain of 103 V/V. This high gain reflects the well-balanced electrical characteristics of the high-performance p-SiNW FETs and coplanar bottom-gate n-IGZO transistors. As shown in Figure 3h, the inverter also delivers large and nearly symmetric noise margins of NM_L = 0.45 V_{DD} and NM_H = 0.44 V_{DD}. The static power consumption characteristics of the inverter are presented in Figure S8, with a minimum static power consumption of only 8.2 pW. Together, the steep voltage-transfer transition, high gain, and large noise margins demonstrate reliable logic operation and strong immunity to input noise, supporting scalable high-density and low power consumption M3D complementary logic.

Figure 3i and Table 1 compare the performance of the demonstrated M3D p-SiNW/n-IGZO inverter with representative CFETs incorporating BEOL-compatible p-type semiconductor channels. A key advantage of this work is the IPSLS-grown p-SiNW FET, which combines scalable BEOL-compatible fabrication with a small subthreshold swing of 120 mV dec^{-1}, closely matching the 133 mV dec^{-1} of the n-IGZO transistor, together with well-balanced p/n current-driving capability. This close matching in both electrostatic control and driving current enables balanced switching and a steep voltage-transfer transition. Consequently, the inverter achieves a peak gain of 103 V/V at V_{DD} = 5 V, corresponding to a normalized gain of 20.6 V^{-1}, demonstrating that the high-voltage efficiency originates from effective p/n device matching rather than simply from the increased supply voltage.

Building on this high-performance M3D stacked inverter, the vertically platform is further extended to implement complementary logic gates, including NOR, NAND, and OR architectures. Figure 4a,b presents the optical images and schematic illustrations of the fabricated gates, while Figure 4c shows the dynamic output waveforms at V_{DD} = 0.5 V. The desired Boolean logics are implemented by arranging the p-SiNW pull-up network and n-IGZO pull-down network in complementary series and parallel configurations. Specifically, in the NOR gate, parallel n-IGZO transistors provide a discharge path if either input is high, whereas series p-SiNW transistors maintain the output at a high level only when both inputs are low. In the NAND topology, series n-IGZO transistors discharge the output only when both inputs are high, while parallel p-SiNW transistors maintain a high output if either of the inputs is low. The OR gate is implemented by combining a NOR configuration with an inverter stage and converting the NOR output into the desired OR logic level. The measured dynamic waveforms closely follow these complementary switching mechanisms, demonstrating that the stacked p-SiNW/n-IGZO CFET architecture supports multi-input logic with reliable voltage levels and fast transitions. These results indicate that the platform can be extended beyond single inverters to compact, high-density, M3D complementary logic circuits.

Notably, IPSLS-grown p-SiNWs offer strong advantages for monolithic 3D integration in terms of process compatibility and scalability. Their low-temperature formation enables high-performance p-FETs without high-temperature dopant activation or advanced lithography such as EBL. More importantly, the hydrogen-free process prevents hydrogen release from the bottom p-type tier, thereby protecting subsequently integrated oxide transistors and enabling true vertical Si/oxide stacking. These features relax the thermal and patterning constraints on top-tier fabrication and facilitate large-area heterogeneous integration. Although the present devices employ moderate dimensions (IGZO W/L = 50/10 μm), vertical integration inherently reduces lateral footprint. Further scaling could be achieved by combining IPSLS-grown p-SiNWs with low-dimensional n-type semiconductors, including two-dimensional materials, toward smaller and higher-density CFET architectures.

CONCLUSIONS

In summary, we demonstrate high-performance M3D complementary logic by vertically integrating IPSLS-grown p-SiNW FETs with n-IGZO transistors. The complementary devices exhibit closely matched current-driving capabilities and steep switching characteristics, with subthreshold swings of 120 and 133 mV dec^{-1} for the p- and n-channel transistors, respectively. This excellent p/n electrical matching translates directly into outstanding circuit performance: the M3D CFET inverter achieves a peak voltage gain of 103 V/V at V_{DD} = 5 V (gain/V_{DD} = 20.6 V^{-1}), together with large and nearly symmetric noise margins of NM_L = 0.45 V_{DD} and NM_H = 0.44 V_{DD}. The architecture is further extended to NOR, NAND, and OR gates with experimentally verified logic operations, demonstrating its scalability beyond a single inverter. Importantly, the IPSLS process provides a scalable and lithography-compatible p-SiNW technology without postgrowth hydrogen passivation, enabling close integration with oxide semiconductors while reducing hydrogen-related process incompatibility. These results establish a high-performance heterogeneous Si/oxide integration platform that combines strong device-level matching with robust circuit-level operation, opening a compelling route toward dense and scalable M3D complementary electronics.

EXPERIMENTAL SECTION

Fabrication of p-SiNW FETs

SiNW FETs were fabricated on silicon substrates with a 500 nm thermally grown SiO_2 layer. The guiding channel patterns were defined using an AZ5124 photoresist and transferred into the SiO_2 layer by inductively coupled plasma (ICP) etching with three alternating cycles of C_4F_8 and O_2 gases, forming three-step guiding trenches. A thin indium (In) catalyst layer was subsequently deposited by a thermal evaporation.

The growth of SiNWs was carried out in a single plasma-enhanced chemical vapor deposition (PECVD) system, which included hydrogen plasma treatment, deposition of an amorphous silicon (a-Si) precursor layer, and vacuum annealing at approximately 300 °C to induce solid−liquid−solid crystallization and lateral SiNW growth along the guiding channels. After SiNW formation, a thermal oxidation process at 550 °C for 2 h or 850 °C for 2 min was performed. Source and drain electrodes were then defined by electron-beam evaporation (EBE) of 15/30 nm Ni/Au. Gate dielectrics consisting of Al_2O_3/HfO_2 stacks were deposited by atomic layer deposition (ALD), or alternatively, Si_xN_y layers were deposited by PECVD for comparison. Finally, Ni gate electrodes were deposited by magnetron sputtering to complete the p-SiNW FETs.

Fabrication of Monolithically Stacked M3D CFET Inverters and Gates

For M3D CFET inverters and gates, the bottom-tier p-SiNW FETs were fabricated following the same procedure described above, except that a thinner gate dielectric stack of 1.2/8 nm Al_2O_3/HfO_2 was employed. Subsequently, a 9/6 nm HfO_2/Al_2O_3 gate dielectric stack

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was deposited by ALD to serve as the gate insulator for the top-tier n-type IGZO transistor. Vertical via holes defining the shared V_{OUT} were formed by reactive ion etching (RIE) through the stacked dielectric layers (1.2/17/6 nm $Al_2O_3/HfO_2/Al_2O_3$). Aluminum electrodes were then deposited by magnetron sputtering to define the GND electrode and the inverter V_{OUT} connection. Finally, an approximately 20 nm-thick IGZO film was deposited by magnetron sputtering under the conditions of Ar/O_2 atmosphere with a gas flow ratio of 10/1 sccm at a pressure of 5 Pa, with a target composition of In:Ga:Zn = 1:1:1, followed by annealing in an N_2 ambient environment at 300 °C for 1 h.

■ ASSOCIATED CONTENT

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

Supporting Information

The Supporting Information is available free of charge at https://pubs.acs.org/doi/10.1021/acsnano.6c16739.

Statistical distributions of threshold voltage, subthreshold swing, I_{ON}, and I_{ON}/I_{OFF} (Figure S1); bias-stress stability of p-SiNW FETs under negative-bias stress (NBS) for 3600 s (Figure S2); extracted threshold voltage shifts from the PBS and NBS transfer characteristics (Figure S3); temperature-dependent transfer characteristics of p-SiNW FETs at V_D = 0.1 V (Figure S4); extracted Schottky barrier height as a function of V_{GS}, yielding an effective gate-modulated barrier height of 85 meV at V_{GS} = 0 V (Figure S5); schematic illustration of the fabrication process for monolithically stacked p-SiNW/n-IGZO CFET inverters (Figure S6); bias-stress stability of the bottom-gate coplanar IGZO transistor (Figure S7); and measured static power consumption of the inverter (Figure S8) (PDF)

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Author Contributions

L.Y., Z.Y., and L.W. carried out the experiments, analyzed the data, and wrote the manuscript. W.Q., W.L., and J.W. participated in the data analysis. W.Q. and L.W. contributed to the electrical measurement. L.Y., J.W., and Z.Y oversaw all phases of the research and revised the manuscript. All authors participated in the writing and revision of the manuscript.

Notes

The authors declare no competing financial interest.

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