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Polarity-Addressed Reset Stabilizes Schottky SiNW-FET Reservoir Computing for Continuous Event-Stream Inference

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ABSTRACT

In-materia reservoir computing is typically benchmarked in segmented regimes where implicit re-initialization masks long-term state accumulation. Under continuous, nonstationary drive, however, multi-timescale device dynamics can retain activity-dependent residuals that fail to relax to a reproducible baseline, leading to drift and accuracy loss. We introduce reset-aware physical reservoir computing, where electrical reset is promoted to an addressable, input-decoupled system operation that can be sparsely triggered by online drift statistics. Trap-engineered Schottky silicon nanowire FETs (SiNW-FETs) realize this concept: interfacial trap kinetics and Schottky-barrier modulation yield multi-timescale fading memory, while source–drain polarity reversal provides a device-native erase path independent of gate updates. Using the in-plane solid–liquid–solid (IPSLS) growth mechanism, aligned SiNW arrays with diameters of ~20 nm are obtained and integrated into a complementary metal-oxide semiconductor (CMOS) compatible, addressable 4×4 top-gated SiNW-FET array. On a standard event-based gesture-recognition benchmark under continuous streaming inference, sparse reverse-bias erase suppresses drift and sustains >90% accuracy, whereas erase-free streaming drops abruptly by ~20% during prolonged operation. These results establish a CMOS-compatible in-materia reservoir with explicit, controllable state management for robust continuous event-driven inference.

1 | Introduction

With the accelerating development of artificial intelligence and the ubiquity of Internet-of-Things sensing, edge systems are increasingly confronted with growing spatiotemporal data streams under stringent constraints on energy, latency, and memory. This tension amplifies the von Neumann data-movement bottleneck and motivates neuromorphic, non-von Neumann computing paradigms for near-sensor information processing [1–4]. Physical reservoir computing (RC) provides an attractive framework for edge temporal processing: intrinsic device dynamics can function as a hardware "temporal kernel," embedding short-term history directly into physical states without heavy buffering, while training remains confined to a lightweight readout (Figure 1a) [5–7]. Across diverse material and device platforms—including memristor, ferroelectric, and phase-change/filamentary systems—physical reservoirs have demonstrated strong performance on temporally structured tasks, supporting the feasibility of computation in the substrate [8–15]. In particular, under continuous streaming inputs, the reservoir's state evolution can itself carry temporal encoding, alleviating reliance on explicit memory and iterative digital recurrence [5, 6, 16].

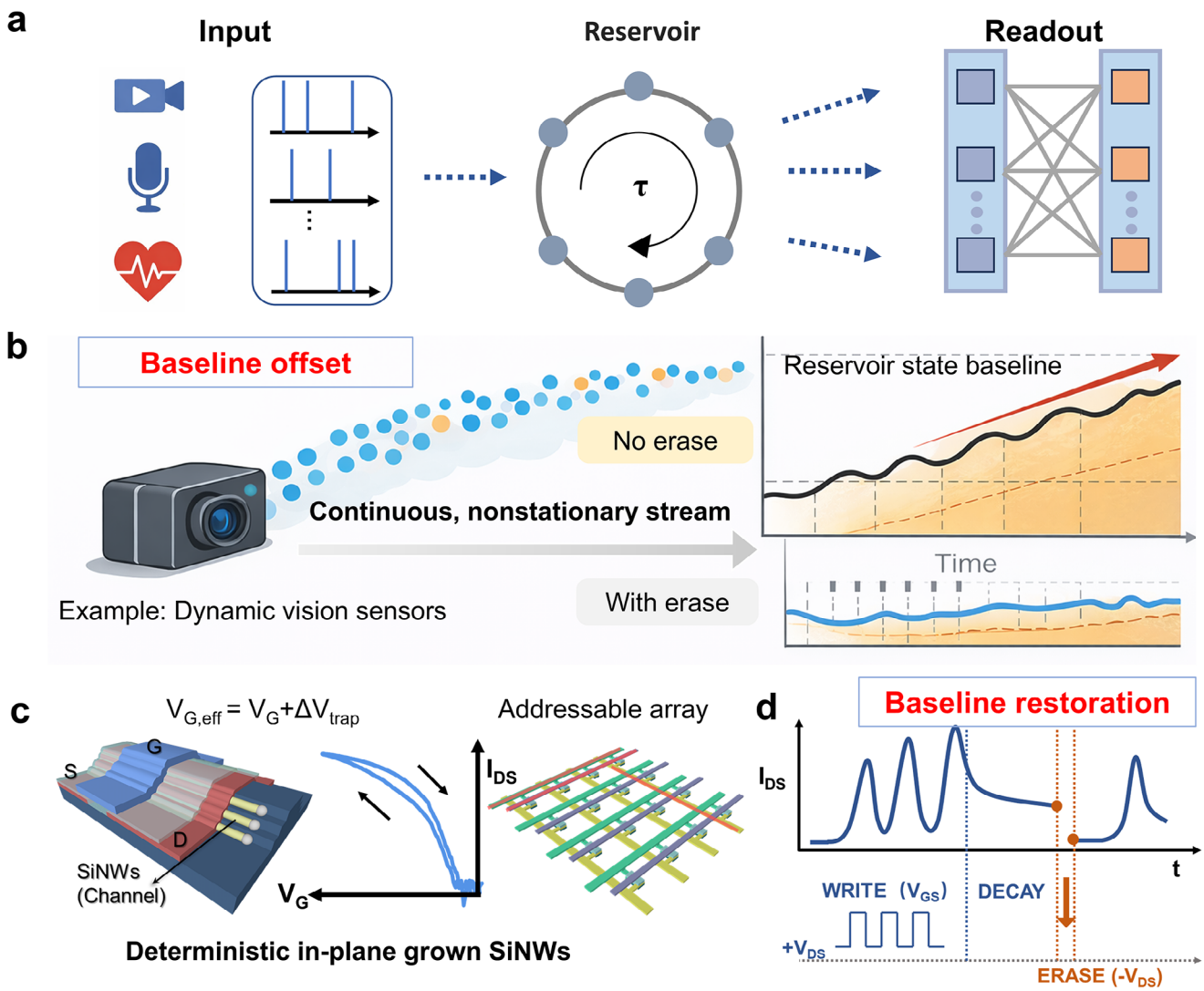

FIGURE 1 | Reset-aware streaming physical reservoir computing (RC) with an addressable trap-engineered Schottky SiNW-FET array. (a) Concept of RC. (b) Continuous, nonstationary DVS streams can induce baseline drift in device state; sporadic erase events bound the baseline during long-horizon inference. (c) IPSLS-grown in-plane SiNW arrays enable deterministic placement and lithography-defined routing for addressable node integration. Trap-assisted modulation of effective gate bias (ΔV_{trap}) and Schottky barrier provides a history-dependent device state. (d) Decoupled write/erase operation: gate-pulse write increases state, intrinsic relaxation yields residual memory, and reverse-bias erase rapidly restores the baseline.

Yet translating physical RC from offline, segmented demonstrations to deployable continuous-time inference exposes a critical and often underappreciated bottleneck: state management under nonstationary drive [5]. In realistic streaming operation, input statistics drift with environment and activity (e.g., bursty event rates, flicker, and illumination changes) [17, 18]. Multi-timescale reservoirs can therefore accumulate activity-dependent residual states that do not passively relax to a stable, reproducible canonical baseline (Figure 1b) [15, 19]. Such residual accumulation manifests as baseline offsets and decision-boundary drift, so that even when short, segmented evaluations appear stable, long-horizon online separability can progressively degrade [20]. This failure mode is frequently obscured because many evaluations implicitly assume reinitialization between samples—via software reset, segmented protocols, or idle gaps long enough for relaxation [19, 21]. In edge settings, however, buffering and pausing are costly, increasing latency and memory footprint, reducing throughput, and potentially offsetting the hardware-efficiency motivation of in-materia processing [22, 23].

Existing mitigation strategies address parts of this problem but rarely satisfy both system-level practicality and device-level nativeness. Software reinitialization or per-segment normalization can restore a baseline, but at the price of segmentation and buffering. Fixed washout periods or idle gaps rely on passive relaxation, which can be insufficient for reservoirs with slow components and introduces unavoidable dead time [19, 21, 24]. Algorithmic compensation (e.g., adaptive normalization, homeostatic regulation, or drift-aware readout updates) can reduce sensitivity to offsets, but pushes complexity back to the algorithm and may entangle correction with the encoding pathway [25, 26]. Although hardware resets have been demonstrated in several platforms, many are coupled to the same actuation channel used for state updates, making it difficult to invoke reset sparsely as an independent system action without simultaneously perturbing

the write gain or update rule [21, 27, 28]. Motivated by this gap, we formalize an operational requirement—reset controllability—defined as an explicit, electrically addressable erase operation that is decoupled from input-driven state updates, can be triggered sparsely based on online drift statistics, and preserves the temporal richness of the reservoir.

From a device standpoint, three-terminal transistors offer additional control freedom relative to two-terminal elements: the gate independently modulates the channel potential and carrier distribution, while the source–drain bias shapes the lateral field profile and when transport is contact-limited, can also modulate the dominant injecting junction [16, 29, 30]. This separation enables, in principle, port-level decoupling between write/update and erase/reset operations, providing a hardware interface for sparsely invoked state management. Within transistor-based reservoirs, one-dimensional nanowires (NWs) are particularly attractive because their strong electrostatic coupling and high interface sensitivity can generate pronounced nonlinearity and multi-timescale dynamics, offering a promising route toward low-power physical RC implementations [29, 31, 32]. However, translating these device-level advantages into deployable, array-scale capability is often limited by scalable integration pathways [33, 34]. Top-down patterning and etching can provide planar NWs and interconnects with controlled geometry and placement, but nanoscale definition typically requires high-resolution patterning (e.g., electron-beam lithography, EBL) together with tighter process windows and higher fabrication cost [35, 36]. Bottom-up routes such as vapor–liquid–solid (VLS) growth or metal-assisted chemical etching can produce ultrathin nanowires more economically, but the resulting NWs usually require transfer-and-place assembly and re-alignment on planar substrates [37–39]; deterministic positioning and array-level uniformity remain challenging, and achieving reliable contacting often demands more stringent alignment and fine electrode definition, further increasing process complexity and overall cost [40–42]. These considerations indicate that a deployable NWs physical-RC platform should simultaneously provide deterministic array placement and alignment, lithography-compatible addressable interconnects, and an electrically decoupled reset channel, so that reset can operate as a sparsely invoked primitive at the node or sub-array level.

In-plane solid–liquid–solid (IPSLS) growth mechanism offers an optional pathway toward these requirements by enabling, in conjunction with conventionally lithographed step/edge guidance structures, selective growth and alignment of silicon nanowires (SiNWs) at predefined locations, thereby facilitating integration with lithography-defined, addressable contacts and interconnects [43–47]. Building on this platform, we implement a reset-aware physical RC paradigm using a trap-engineered Schottky SiNW field-effect transistor array (SiNW-FETs) (Figure 1c). Interfacial trap kinetics coupled to Schottky-barrier modulation provide intrinsic multi-timescale fading memory. Crucially, reversing the drain polarity reverse-biases the dominant injecting junction to establish a dedicated erase/reset pathway that is decoupled from gate-actuated write/update (Figure 1d), yielding an intrinsic "gate-write / polarity-erase" separation. This separation allows state management in streaming protocols to be invoked sparsely as an independent system action without altering the input-encoding rule. In addition, rapid thermal processing tunes the trap contribution, enabling access to a hysteresis-suppressed, logic-like stable regime and a hysteretic, trap-enabled neuromorphic regime on the same platform. To evaluate continuous-time operation under event-driven inputs, we adopt a fixed physical time base to map event activity to gate-pulse updates and use dynamic vision sensor (DVS) streams as a representative and demanding case. We benchmark segmented evaluation with per-segment reinitialization against true streaming inference and show that condition-triggered sparse V_{DS} erase suppresses residual accumulation and baseline drift under nonstationary streams. With minimal reset overhead, the proposed approach preserves long-term baseline stability and state separability, thereby instantiating reset controllability as a practical device–array–system primitive for deployable physical reservoir computing.

2 | Results and Discussion

2.1 | IPSLS-Integrated SiNW-FET Array

Using the IPSLS growth mechanism, we realize a lithography-defined, addressable 4 × 4 top-gated SiNW-FET array, in which the source (S), drain (D), and gate (G) routing is clearly resolved at the array level (Figure 2a). The complete IPSLS-based fabrication workflow is detailed in Figure S1, establishing a scalable and complementary metal-oxide semiconductor (CMOS) compatible process route for deterministic nanowire placement, lithography-defined contacts, and array-level interconnection. A representative unit cell (Figure 2b, top) confirms good alignment between the patterned electrodes and the channel region, while the magnified channel view (Figure 2b, bottom) shows three directionally grown SiNW layers bridging the source–drain gap, substantiating spatially deterministic control of nanowire growth trajectories enabled by IPSLS. Leveraging the stackable growth capability of IPSLS, the number of parallel SiNWs can be further increased, providing a straightforward route to boost the drive current (Figure S2a); additional array-level morphology views after via opening are shown in Figure S2b. Structural and compositional characterization of representative IPSLS-grown SiNWs is summarized in Figure 2c and Figure S3. Cross-sectional transmission electron microscopy (TEM) indicates nanoscale diameters (~20 nm), and the diffraction pattern confirms crystalline Si. Statistical analysis of 55 individual SiNWs further gives an average diameter of 22.5 ± 4 nm (Figure S4), confirming the dimensional uniformity of the grown SiNW channels. The device stack (Figure 2d) consists of a Ti/Au top gate, an Al_2O_3/HfO_2 gate dielectric, Pt/Au source–drain contacts, and a SiNW channel on SiO_2, implying that transport can be influenced by both contact injection and interfacial charge trapping/detrapping processes.

Electrical uniformity across the array is demonstrated in Figure 2e, which summarizes the transfer characteristics of all 16 devices measured at V_{DS} = 0.1 V, showing consistent p-type gate modulation across the array (statistics in Figure S5). The p-type gate modulation of the SiNW-FETs is mainly associated with acceptor-type In incorporation during IPSLS growth. The devices achieve an ON/OFF current ratio of approximately 10^6 with an off-state current on the order of 10^{-12} A, and the minimum subthreshold swing reaches about 180 mV/dec. Further performance improvements are expected through established structural optimizations, such as step-necking and gate-all-around

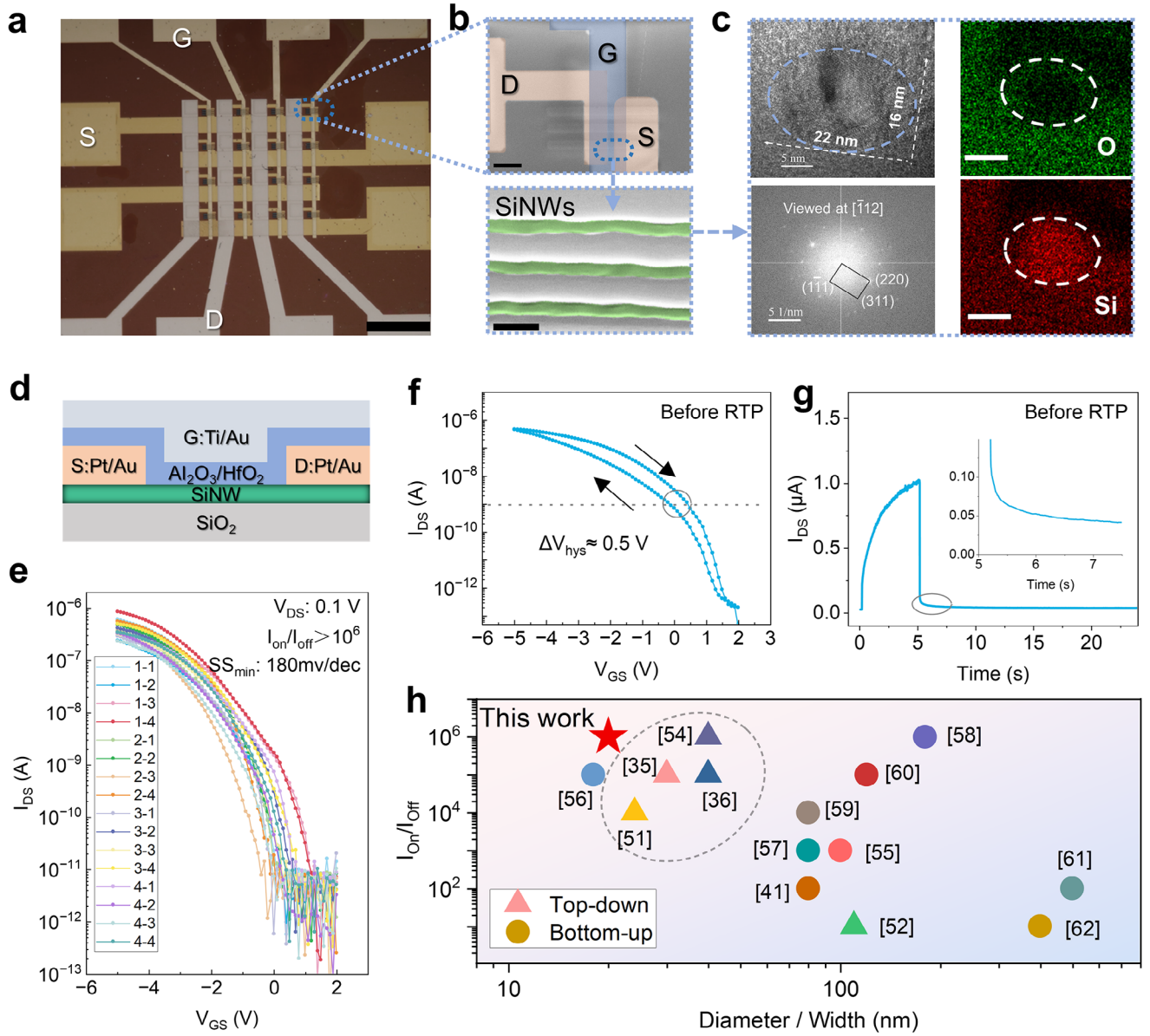

FIGURE 2 | Deterministic IPSLS-integrated SiNW Schottky-barrier FET array and thermally tunable functional bifurcation. (a) Optical micrograph of the lithography-defined, addressable 4 × 4 top-gated SiNW-FET array showing the source (S), drain (D), and gate (G) routing layout (scale bar, 200 μm). (b) Representative unit-cell SEM images showing lithography-registered alignment between electrodes and the channel region (top, scale bar, 10 μm) and three directionally grown/stacked SiNW layers bridging the source–drain gap (bottom, scale bar, 100 nm). (c) Structural and compositional characterization of representative IPSLS-grown SiNWs, including cross-sectional TEM (typical diameter ~16–22 nm), SAED and elemental maps (scale bar, 10 nm). (d) Device stack schematic (Ti/Au top gate, Al_2O_3/HfO_2 gate dielectric, Pt/Au source–drain contacts and SiNW channel on SiO_2). (e) Transfer characteristics of all 16 devices measured at V_{DS} = 0.1 V, demonstrating uniform p-type gate modulation across the array. (f) Before RTP, the bidirectional transfer sweep (+2 → -5 → +2 V) measured at V_{DS} = 0.1 V exhibits pronounced hysteresis (ΔV_{hys} = 0.5 V). (g) The pulse response shows clear potentiation and post-pulse relaxation. (h) Comparison of nanowire FET platforms reported for neuromorphic computing.

geometries, which can strengthen electrostatic control [44, 45]. Notably, the memory characteristics can be thermally tuned. Before RTP, the bidirectional transfer sweep (+2 → −5 → +2 V) measured at V_{DS} = 0.1 V exhibits a pronounced hysteresis window (ΔV_{hys} = 0.5 V; Figure 2h); correspondingly, the pulse response shows clear current potentiation during gate stimulation followed by a discernible post-pulse relaxation tail (Figure 2i). In contrast, after rapid thermal processing (RTP, 300°C, 2 min), the hysteresis window is markedly narrowed (ΔV_{hys} = 0.05 V), indicating a hysteresis-suppressed operating regime more suitable for stable logic-like operation (Figure S6a); consistently, the gate-pulse-induced transient response exhibits only a weak memory component, with the current rapidly relaxing back to baseline after stimulus removal (Figure S6b). This RTP-dependent suppression of hysteresis is further supported by capacitance-based electrical measurements. The normalized C–V characteristics of dielectric-only control samples show that RTP reduces the bias-dependent capacitance modulation and forward/reverse sweep hysteresis of the Al_2O_3/HfO_2 stack, while the voltage-dependent loss factor is also strongly suppressed after RTP (Figure S7).

These results provide electrical evidence for a reduced trap-related dielectric response after RTP, consistent with prior reports that moderate-temperature annealing can passivate interface and border traps and mitigate hysteresis in high-k gate stacks [48–50]. Together, these RTP-dependent contrasts delineate two thermally selectable operating modes: a hysteresis-suppressed, logic-like regime after RTP and a hysteretic, trap-enabled neuromorphic regime before RTP. The hysteresis window remains stable over repeated cycling (Figure S8), supporting the reproducibility of the memory behavior. Bias dependence is further summarized in Figure S9: under positive drain bias, the hysteresis window increases with V_{DS}, whereas under negative drain bias the overall current magnitude is reduced while a finite hysteresis remains, consistent with polarity-dependent contact injection and barrier modulation in p-type Schottky-barrier transistors. Gate leakage was monitored simultaneously during transfer measurements and remained well below I_{DS} over the full bias range (Figure S10), confirming negligible dielectric leakage in the Al_2O_3/HfO_2 stack.

Finally, we benchmark this platform against previously reported nanowire-based neuromorphic transistors (Figure 2h; Table S1 and Note S1) [35, 36, 41, 51–62]. Enabled by the IPSLS mechanism, we simultaneously realize ultrasmall-diameter SiNWs (~20 nm), a high ON/OFF ratio of $\sim 10^6$, and lithography-registered, addressable interconnect routing at the array level. In contrast to top-down schemes that define nanowires via nanoscale patterning/etching, IPSLS preserves the intrinsic advantages of growth-derived 1D nanowires. In contrast to conventional bottom-up approaches that rely on transfer and post hoc alignment, IPSLS leverages deterministic placement and directionally guided growth to substantially improve compatibility with lithography-defined interconnects. Consequently, IPSLS provides an alternative integration route that combines key attributes of both dominant paradigms, thereby better supporting the construction of scalable, array-scale addressable device platforms and establishing a robust hardware basis for systematic investigations of pulse-level state dynamics.

2.2 | Pulse-Programmable Dynamics

Figure 3 quantifies pulse-level state dynamics primarily in the hysteretic, before-RTP devices and distills them into device operations for reset-aware physical RC under continuous-time drive. Unless otherwise specified, pulsed measurements in Figure 3 are performed on the before-RTP regime; forward drain bias is used for read/update, and polarity reversal provides an electrically addressable reset channel. Figure 3a first establishes amplitude programmability: increasing the magnitude of negative gate pulses (V_G = −1 V to −5 V) yields progressively larger pulse-evoked $I_{DS}(t)$ excursions together with a higher elevated post-stimulus level, indicating a retained state component beyond the instantaneous field effect. Figure 3b demonstrates duration programmability, where increasing the pulse width systematically strengthens the accumulated state and prolongs its persistence, providing a continuous tuning knob from short-lived dynamics to more retained residuals. Figure 3c reveals rate dependence at fixed pulse amplitude: shortening the inter-pulse interval (0.05–0.5 s) strengthens temporal summation and accelerates the approach to saturation, whereas longer intervals allow more relaxation between pulses and thus reduce net accumulation, implementing a direct "rate-to-state" transduction well matched to event-stream encoding. Beyond gate programmability, forward drain bias provides an independent handle to scale update strength, as increasing V_{DS} enhances both the pulse-evoked response and the retained component at fixed gate-pulse conditions (Figure S11), consistent with strengthened contact injection and barrier modulation under larger forward bias. Under reverse drain bias, the device operates in a more contact-limited, off-state–dominated regime: the overall current magnitude is reduced, and the long-lived post-pulse tail becomes much less pronounced, yet cumulative modulation during a pulse train can still be observed as the pulse number increases (Figure S12). In this regime, state accumulation is expressed primarily as an enhancement of the in-train dynamic response, rather than being converted into an explicit steady residual conductance after the train. Figure 3d isolates the effect of pulse count by terminating the write train and tracking the ensuing relaxation, thereby extracting the fading-memory kernel of the hysteretic regime. The post-stimulus decay is well captured by a bi-exponential form, revealing a fast component on the order of τ_{fast} = 0.12 s and a slower component on the order of τ_{slow} = 1.4 s. τ_{fast} remains nearly invariant whereas τ_{slow} increases modestly (Figure S13), consistent with progressively engaging slower relaxation pathways under stronger accumulated stimulation. Although multi-timescale fading memory benefits temporal feature embedding, the persistence of residual state implies that passive relaxation alone may not reliably recover a unique canonical baseline between successive segments in streaming, motivating an explicit reset operation for deployable continuous-time inference [5, 19].

Figure 3e,f demonstrates the system-level consequence of residual state under streaming drive by comparing two identical write segments with and without an inserted erase window. With polarity-programmed erase ($-V_{DS}$ during reset), the readout baseline is actively restored and the second segment starts from a reproducible initial condition, as highlighted by a markedly reduced residual offset ΔI; without erase, the second segment inherits the prior history and continues to accumulate. The selectivity of the array-level reset addressing was further verified by a source-biasing control experiment, where the floating-source condition showed no measurable reset disturbance in the unselected state (Figure S14). Figure 3g summarizes erase controllability as a phase map using a normalized baseline-restoration metric, $E_{base} = (I_{after1}-I_{re})/(I_{after1}-I_0) = 1-(I_{re}-I_0)/(I_{after1}-I_0)$, where I_0 is the pre-write baseline (Pre-read1), I_{after1} is the post-write baseline (Post-read1), and I_{re} is the recovered baseline after erase (Pre-read2). By definition, $E_{base} = 1$ denotes full return to the initial baseline, thereby converting device behavior into a directly usable system-level design rule (e.g., selecting reset strength and latency from the E_{base} = 1 contour), with an analogous gate-erase controllability map shown as a strategy control in Figure S15. Beyond baseline recovery, a deployable reset primitive should additionally minimize inadvertent reprogramming of the write/update rule. We therefore quantify "trajectory fidelity" by aligning identical pulse indices across the two write segments and evaluating $R_k = I_{max,\,post}(k)/I_{max,\,pre}(k)$ (k = 1–5); under erase settings selected to yield comparable baseline recovery (E_{base} = 1), $-V_{DS}$ erase preserves the subsequent pulse-write trajectory with only only percent-level deviation, whereas gate-only erase requires substantially stronger actuation and induces noticeably larger trajectory distortion (Note S2 and Table S2), consistent with

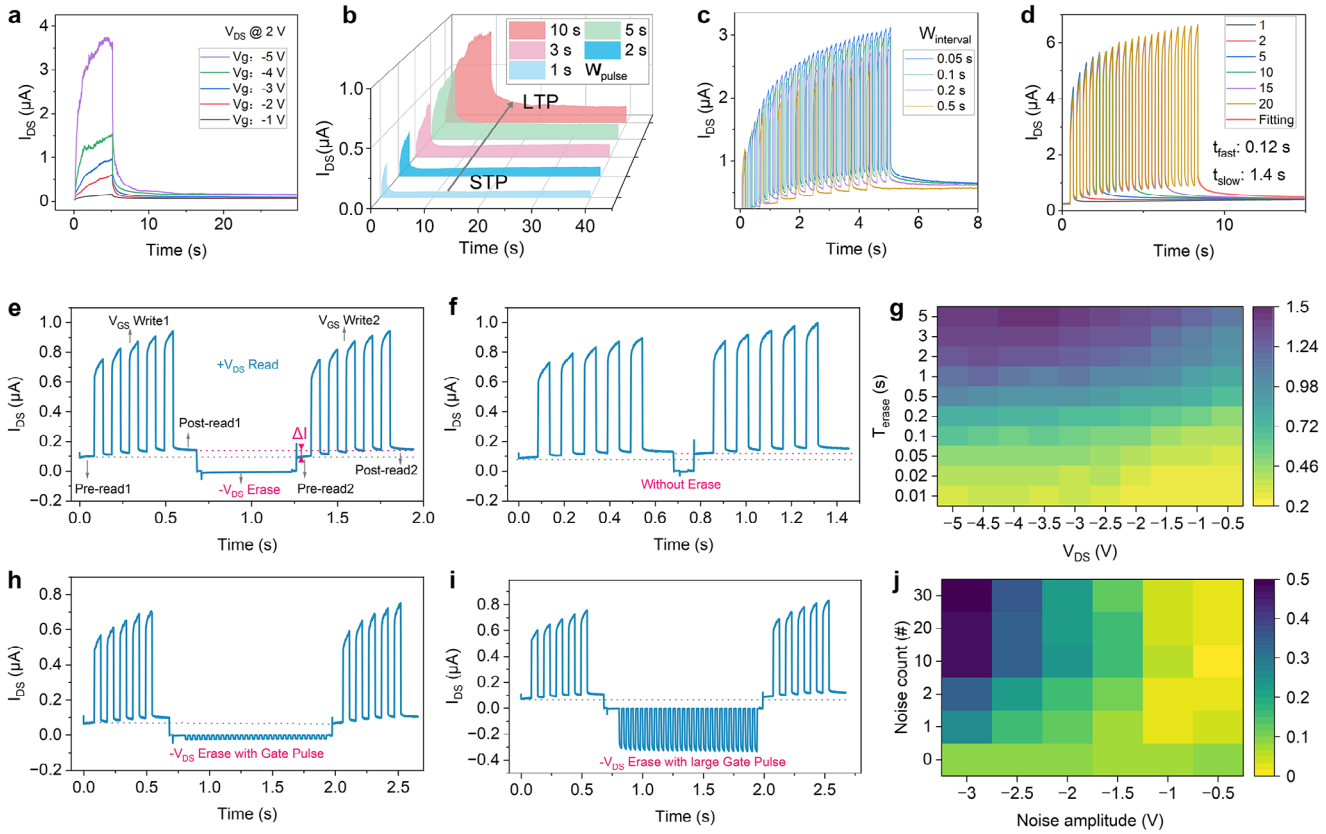

FIGURE 3 | Pulse-programmable dynamics and polarity-programmed erase/reset in the SiNW Schottky-barrier FET. (a) Transient drain-current responses recorded at $V_{DS} = +2$ V under gate stimuli with different amplitudes ($V_G = -1$ to -5 V), showing tunable pulse-evoked enhancement and residual state after stimulus removal. (a) Pulse-width dependence of the transient response under otherwise identical conditions, illustrating duration-controlled state accumulation. (c) Frequency (inter-pulse-interval) dependence measured at a fixed pulse width (0.1 s), where shorter intervals promote temporal summation and faster saturation. (d) Pulse-count dependence (fixed pulse width of 0.1 s) and the subsequent relaxation after the pulse train; the decay is fitted with a bi-exponential function to extract dual timescales. (e) Two-cycle write–erase–rewrite protocol demonstrating decoupled actuation channels: gate-pulse write/update under $V_{DS} > 0$ and polarity-programmed erase under $V_{DS} < 0$ restore the baseline between segments (ΔI denotes residual baseline offset). (f) Control experiment without erase, where the second write segment continues from the elevated residual state, evidencing cumulative baseline drift. (g) Erase-window map quantifying baseline restoration as a function of erase bias magnitude ($V_{DS} < 0$) and erase duration (T_{erase}). (h, i) Erase robustness test in which gate perturbation pulses are applied during the erase window (treated as interference), evaluating interference immunity of V_{DS} -driven reset. (h) Representative trace; (i) enlarged view. (j) Interference susceptibility (write-in risk) map as a function of perturbation amplitude and perturbation pulse number, enabling an application-defined safe/unsafe boundary.

the notion that V_{DS}-programmed reset is more orthogonal to the gate-update pathway.

In deployable RC settings, the reset window may overlap with other control pulses (treated here as interference), rather than being a fully isolated phase [5, 6, 19]. Figure 3h superimposes gate perturbation pulse trains (amplitude $V_{G,\,pert}$, count N_{pert}) during the $-V_{DS}$ erase window. Representative traces confirm that the reset remains functional under moderate perturbations, whereas increasing $|V_{G,\,pert}|$ and/or N_{pert} progressively degrades baseline restoration (Figure 3i). We quantify this interference susceptibility using a normalized residual-baseline metric (W_{in}, smaller is better; definition in Note S3) and summarize it as a 2D phase map over ($V_{G,\,pert}$, N_{pert}) (Figure 3j). Importantly, the map is presented as a continuous susceptibility surface whose iso-contours can be selected according to application-specific interference budgets and scheduling constraints, rather than relying on a single fixed threshold. A high-density scan in the transition regime (Figure S16) corroborates the smoothness and reproducibility of the susceptibility landscape and supports robust iso-contour extraction. Run-to-run repeatability and cycling endurance of the recovered baseline are evaluated in Figure S17. The 50-cycle run-to-run statistics confirm reproducible reset behavior under different hold durations and perturbation/noise conditions (Figure S17a). In addition, the baseline, after-write, and after-reset currents remain stable over more than 50 000 cycles under a representative 0.3 s perturbation-window reset condition, indicating reproducible state restoration without obvious cumulative drift (Figure S17b). Together, Figure 3 establishes drain-polarity–addressable write/update and erase primitives for streaming operation and quantifies their controllability and robustness.

2.3 | Polarity-Dependent Barrier–Trap Write/Erase Mechanism

Figure 4 then elucidates the physical origin of this polarity programmability by connecting the polarity-dependent transport

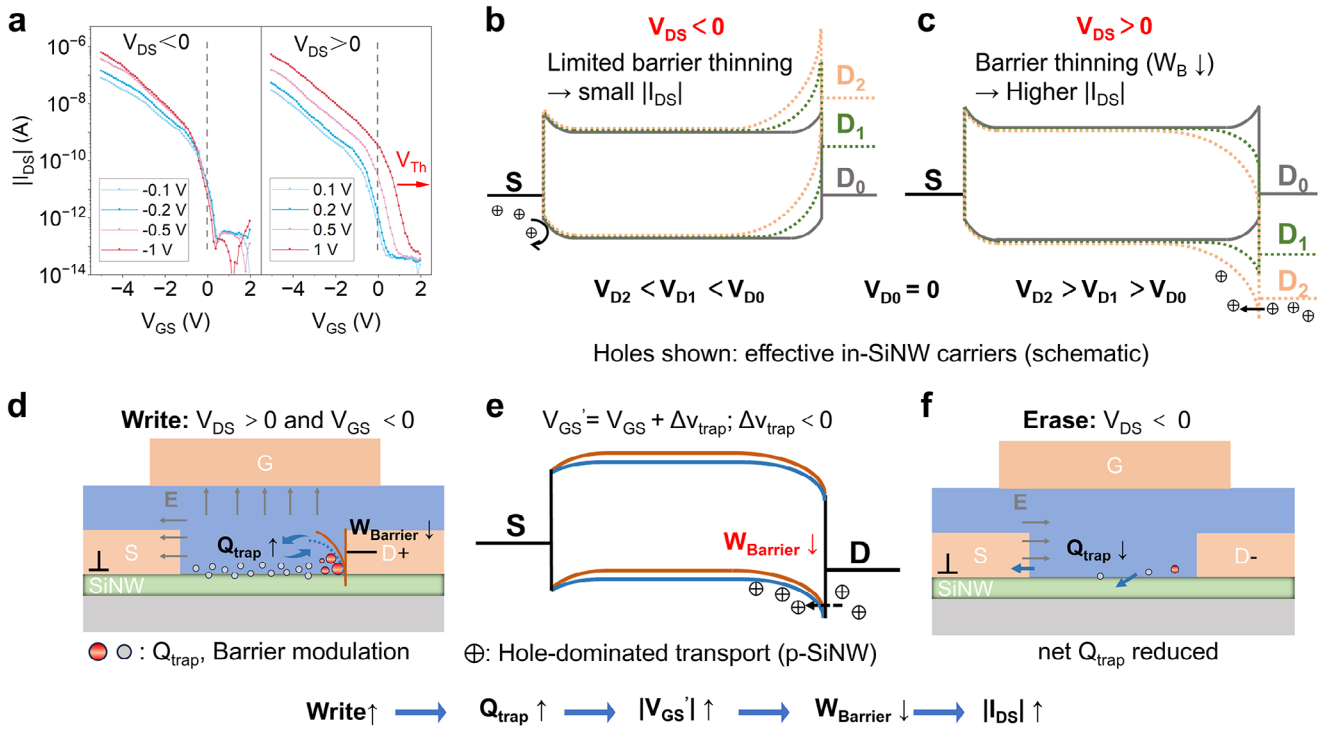

FIGURE 4 | Polarity-dependent transport and barrier–trap–coupled write/update and erase (accelerated reset) mechanism in a p-type SiNW Schottky-barrier FET. (a) Transfer characteristic measured under $V_{DS} < 0$ and $V_{DS} > 0$ (multiple $|V_{DS}|$), showing near-overlapped subthreshold branches and more complete turn-off for $V_{DS} < 0$, whereas $V_{DS} > 0$ produces a pronounced apparent threshold shift and increased $|I_{DS}|$, evidencing polarity-controlled injection/barrier modulation. (b) Schematic band-diagram evolution under $V_{DS} < 0$, where the effective Schottky barrier varies only weakly with $|V_{DS}|$, consistent with weak threshold drift and reduced current. (c) Schematic band-diagram evolution under $V_{DS} > 0$, where forward bias thins the effective injection barrier (enhanced transparency) and yields a clear threshold displacement, rationalizing the choice of $V_{DS} > 0$ as the write/update operating window. (d) Cross-sectional schematic of the write operation ($V_{DS} > 0$, $V_{GS} < 0$), where negative gate pulses drive trap charging (Q_{trap}) near the injecting contact, producing an effective electrostatic shift (ΔV_{trap}) that reduces $W_{barrier}$ and enables conductance potentiation. (e) Band-diagram illustration of the written state, where ΔV_{trap} adds to V_{GS} to form an effective gate voltage V'_{GS}, lifting the channel bands and facilitating hole tunneling via an effectively thinned/lowered injection barrier. (f) Cross-sectional schematic of the erase operation ($V_{DS} < 0$), where polarity reversal promotes state removal by suppressing injection and favoring detrapping/neutralization pathways, restoring the barrier opacity and returning I_{DS} toward its baseline. *Note:* In the schematics, "hole injection" denotes the effective injection across the Schottky barrier into the SiNW valence band; the metal contact serves as an electronic reservoir.

asymmetry of a Schottky-barrier transistor to trap-mediated electrostatic modulation. Figure 4a–c rationalizes why a forward drain bias ($V_{DS} > 0$) is selected as the operating window for gate-pulse write/update in our p-type Schottky-barrier SiNW FET. Figure 4a first exposes a strong polarity asymmetry in the transfer characteristics: under $V_{DS} < 0$, the subthreshold branches largely overlap with more complete turn-off and only a weak apparent-threshold shift as $|V_{DS}|$ increases, whereas under $V_{DS} > 0$ the device exhibits a much larger $|I_{DS}|$ together with an approximately shape-preserving lateral shift in the subthreshold region. This behavior is consistent with contact-controlled transport in Schottky-barrier transistors, where reversing V_{DS} relocates the dominant injecting junction and reshapes the local field distribution that sets the effective barrier width/transparency [63–66]. The output asymmetry summarized in Figure S18 corroborates this contact-limited picture by showing a pronounced rectifying behavior, indicating that the injection barrier is not symmetric under bias reversal. In addition, the time-domain responses in Figure S19 show that under forward bias ($+V_{DS}$) the drain current can gradually increase over time, whereas under reverse bias ($-V_{DS}$) the current remains much smaller and nearly time-invariant, supporting that forward bias places the device in an injection-enhanced, barrier-sensitive operating window. This polarity dependence is further supported by technology computer-aided design (TCAD) results in Figure S20, which reproduce the key trend that the apparent threshold is substantially more stable under $V_{DS} < 0$ but shifts under $V_{DS} > 0$. The band-diagram schematics in Figure 4b,c summarize this selection rule, with additional support from the TCAD results in Figure S21: for $V_{DS} < 0$ the hole-injection direction yields a barrier profile that changes little with $|V_{DS}|$ (Figure 4b), whereas for $V_{DS} > 0$ increasing $|V_{DS}|$ more effectively thins the injecting barrier (reduced $W_{barrier}$) and enhances tunneling/injection (Figure 4c). Consequently, $V_{DS} > 0$ provides both a larger I_{DS} and a stronger sensitivity to barrier modulation, and is therefore chosen for gate-pulse write/update in the pulsed protocols.

Building on this polarity-controlled barrier sensitivity, Figure 4d–f elucidates the write/erase operations in terms of charge exchange with the high-k/interfacial trap reservoir and its coupling to the Schottky injection barrier. The presence of a high-k/interfacial defect reservoir is evidenced by the contrasting

memory windows observed before and after RTP in Figure 2. As shown in Figure 4d, gate-pulse write/update is driven by the combined action of the vertical gate field and the lateral source–drain electric field. The negative gate-voltage pulses modulate the vertical band bending across the SiNW/high-kkk interfacial region and promote charge exchange with the high-k/interfacial trap reservoir, leading to the accumulation of an effective trap-induced electrostatic offset, ΔV_{trap} [67–69]. Meanwhile, under a forward drain bias ($V_{DS} > 0$), the lateral source–drain field redistributes the potential drop along the SiNW and concentrates the local electric field near the barrier-sensitive Schottky contact region. The superposition of the vertical gate field and the lateral drain field forms a contact-localized high-field hotspot, where ΔV_{trap} is strongly coupled to the dominant Schottky-barrier injection pathway and can more effectively increase the injecting-barrier transparency [64, 70]. The corresponding band diagram for the programmed (written) state is summarized in Figure 4e: ΔV_{trap} adds to the applied negative gate bias (V_{GS}) to form an effective gate voltage V'_{GS}, which enhances gate-induced band bending and further thins/lowers the effective injection barrier, resulting in a larger hole-tunneling current. Additional gate-pulse programming tests further show that the slow state can be written even at $V_{DS} = 0$ V, corroborating that the vertical gate field alone is sufficient to update ΔV_{trap} (Figure S22; Note S4). However, the much stronger current gain under $V_{DS} > 0$ indicates that forward drain bias amplifies the written trap state through contact-localized Schottky-barrier coupling. Notably, the sign of V_{DS} reverses the evolution of the low-bias asymmetry $|I_{(+0.05\,V)}/I_{(-0.05\,V)}|$, consistent with the drain-polarity-controlled relocation of the dominant injecting junction and the resulting contact-localized coupling of ΔV_{trap} to the Schottky barrier.

Finally, Figure 4f illustrates the erase operation enabled by polarity reversal to $V_{DS} < 0$. Unlike gate-only erase, polarity reversal does not simply apply an opposite vertical field through the same write terminal. Instead, reversing V_{DS} reconfigures the lateral electric field and potential profile along the SiNW and relocates the high-field, barrier-dominant contact region. Since the interfacial or near-interfacial traps are electrically coupled to the channel and local Schottky-contact electrostatics, their occupancy is affected by the local channel potential, lateral electric field, carrier distribution, and quasi-Fermi-level alignment. Under $V_{DS} < 0$, the previously written trap-charge state in the barrier-coupled region becomes less stable and can relax through field-assisted detrapping, charge re-equilibration with the channel, and/or carrier-assisted neutralization. The resulting reduction of the local ΔV_{trap} restores the Schottky barrier toward a less transparent state and drives the readout current back toward the baseline.

Importantly, this erase process should be understood as a tunable baseline-restoration operation rather than a hard global erasure of all trap states. Complete discharge of distributed traps along the entire channel is not required, because the source–drain current in a Schottky-barrier FET is dominated by the contact-localized injection barrier. Thus, relaxing the trap-induced electrostatic offset in the barrier-dominant region is sufficient to recover the measured current baseline. The reverse-bias amplitude and duration therefore provide reproducible operational control over the ensemble-averaged trap state, as quantified by the E_{base} phase map. This source–drain-terminal reset pathway suppresses detrimental baseline drift while avoiding the strong perturbation of the gate-encoded update trajectory that can occur under gate-only erase. Such tunable baseline restoration is beneficial for reset-aware reservoir computing, because it helps balance long-term drift suppression with the preservation of short-term fading-memory dynamics.

2.4 | Reset-Aware Event-Stream Inference with SiNW-FET Reservoirs

Figure 5 validates a reset-aware streaming physical RC workflow, where the drain-polarity programmability of the SiNW-FET is elevated from a device-level behavior to an explicit state-management operation for long-horizon event-stream inference. Figure 5a outlines the mapping from dynamic vision sensors (DVS) events to device actuation. We evaluate this workflow on the publicly available 128-DVS-Gesture dataset [71]. DVS events are first accumulated onto a fixed physical time base (Δt) so that the discretization remains commensurate with the device's intrinsic relaxation dynamics. The binned event activity is then converted into gate-pulse updates that drive the reservoir under forward drain bias ($V_{DS} > 0$). In the reservoir front-end, each pulse elicits a rapid field-effect transient followed by a slower relaxation tail, and the state is propagated across time (and across segments) through a dual-timescale fading-memory model (τ_{fast}, τ_{slow}), thereby embedding recent event history into a compact, device-shaped temporal representation. A compact convolutional neural network (CNN) readout is trained on these reservoir features. In the simulation, we compare a counts-only baseline without the reservoir, where event-count frames are directly processed by the CNN readout, and no cross-segment physical memory is retained, with two FET-stream settings in which the reservoir state is propagated across segments either by natural decay alone or by natural decay together with an inserted drain-polarity-programmed erase window between adjacent segments (Note S5).

Crucially, the same device provides an explicit reset path that is distinct from the gate-encoding terminal. When needed, a brief reverse-bias hold ($V_{DS} < 0$) actively erases residual state, restoring a reproducible baseline without conflating reset with the input-encoding gate terminal. In the simulation, this erase action is parameterized by a continuous hold duration, t_{erase}, matching the experimentally deployable operation of applying a negative V_{DS} for a controlled time window and enabling budget-constrained reset scheduling. A device-level energy estimate is provided in Note S6, showing a write/update channel power of approximately 0.28 μW under the DVS-Gesture operating condition and a representative reverse-bias erase energy of approximately 2.2 nJ. Since erase is sparsely triggered rather than applied after every input event, the reset-related energy overhead remains limited while allowing a trade-off among device energy, readout reliability, and circuit-level requirements. To emulate true streaming beyond segmented benchmarks, the DVS-Gesture segments are concatenated into recording-level event streams, and the reservoir state is carried across adjacent segments rather than reinitialized.

Figure 5b shows a diagonal-dominant confusion matrix with an overall accuracy of 91.6%, indicating that the SiNW-FET reservoir

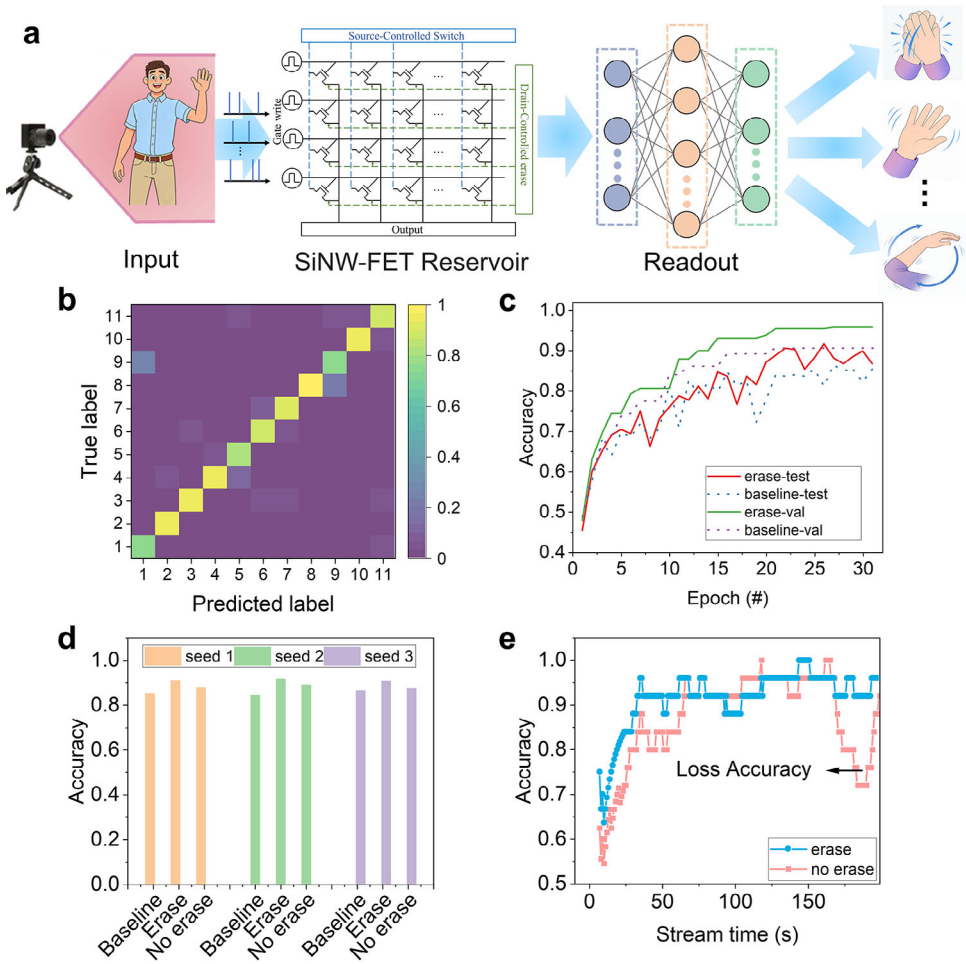

FIGURE 5 | Reset-aware streaming DVS gesture recognition enabled by drain-polarity–programmable SiNW-FET reservoirs. (a) Task-to-device mapping schematic: DVS events are accumulated on a fixed physical time base (Δt) and encoded into gate-pulse updates that write the SiNW–Schottky FET reservoir state under $V_{DS} > 0$; intrinsic dual-timescale decay provides temporal embedding, while an explicit reverse-bias hold ($V_{DS} < 0$) serves as an erase/reset operation for baseline restoration; readout outputs predictions. (b) Confusion matrix for DVS gesture recognition using the reset-aware SiNW-FET reservoir mapping, showing diagonal-dominant class separability. (c) Training accuracy comparison between a conventional baseline pipeline (without the SiNW-FET reservoir front-end) and the erase-enabled SiNW-FET mapping. (d) Accuracy distributions across multiple random seeds comparing baseline, with erase, and no erase protocols, highlighting improved repeatability and reduced sensitivity to initialization with erase. (e) Streaming accuracy trajectories comparing with erase and no erase operation; without erase, residual state accumulation induces drift that can trigger a sudden performance drop, whereas erase maintains long-term baseline stability and sustained accuracy under continuous inference.

front-end yields representations with clear class separability under event-driven inputs. The remaining confusions are mainly concentrated among visually similar gestures, consistent with limited event evidence in certain segments rather than a collapse of temporal encoding. Figure 5c–e then quantifies the impact of state management under continuous streaming. Figure 5c compares the learning behavior of the erase-enabled FET streaming pipeline against the counts-only baseline, showing that introducing the reservoir together with erase improves accuracy and yields smoother convergence. Figure 5d further highlights robustness under seed-to-seed variability, where FET-stream erase consistently outperforms FET-stream no-erase, and both surpass the counts-only baseline. Finally, Figure 5e visualizes the characteristic streaming failure mode without explicit reset: in the no-erase configuration, accuracy can remain competitive initially, but drops by ~20% around ~200 s as residual-state accumulation biases the operating point and induces drift. With erase enabled, occasional reverse-bias resets prevent this runaway baseline shift and maintain stable accuracy over extended streaming, demonstrating that sparse, condition-triggered erase events can suppress long-horizon drift while preserving the temporal dynamics required for computation.

To further characterize robustness under practical nonstationary perturbations, we performed an additional model-based stress test on the clean-trained streaming inference pipeline (Figure S23; Note S7). In this analysis, the readout trained on clean DVS-Gesture streams was evaluated on perturbed streams without retraining. The perturbations were dynamically injected after loading the clean event-count streams, so the original event-count cache was not modified. We considered two representative nonstationary perturbations: slow event-rate drift and burst-like background noise. To connect these input perturbations with the trap-mediated device dynamics, a weak residual-drift coupling was introduced to map the accumulated slow reservoir state to an effective baseline/operating-point shift in the reservoir

feature space. Under a conservative reset policy, the reset-aware configuration produced small positive accuracy changes relative to the no-erase case under both rate drift (+1.51%) and burst-like noise (+1.50%), while reducing residual-tail and baseline-drift metrics. The erase-time overhead remained below 1% for both perturbations (0.64% and 0.56%, respectively). These results further support that the drain-polarity-programmed reset improves streaming robustness by managing internal reservoir-state drift with limited overhead, rather than acting as a generic input-denoising operation.

3 | Conclusion

In-materia reservoir computing faces a deployability bottleneck under nonstationary continuous-time drive, where activity-dependent residual states accumulate, induce baseline drift, and progressively erode long-horizon separability. Multi-timescale reservoirs can encode temporal context, yet their slow components may accumulate activity-dependent residuals that shift the baseline and progressively degrade long-horizon separability during true streaming inference. To address this gap, we introduce reset-aware physical reservoir computing, where electrical reset is promoted to a first-class system operation that is electrically addressable and decoupled from input-driven state updates, enabling sparse invocation to restore a reproducible baseline without altering the encoding rule. Trap-engineered Schottky SiNW-FETs provide a device-native implementation: interfacial trap kinetics coupled to Schottky-barrier modulation yield intrinsic fading memory, while source–drain polarity reversal establishes an orthogonal erase path independent of gate updates. Implemented on an IPSLS-enabled, CMOS-compatible, addressable 4×4 top-gated array, this "gate-write / polarity-erase" interface translates device physics into a practical streaming primitive. On continuous DVS128 Gesture event streams, sparse reverse-bias erase suppresses drift and sustains >90% accuracy over prolonged operation, whereas no-erase streaming degrades by ∼20%. These results highlight decoupled, addressable reset controllability as a promising device–array–system capability for robust, long-horizon event-driven inference.

4 | Experimental Section

4.1 | Device Fabrication of SiNW-FET Arrays (Figure S1)

SiO_2-coated Si wafers were sequentially cleaned in N-methylpyrrolidone, ethanol, and deionized water by ultrasonication, followed by N_2 blow-drying. Guiding-terrace stripe patterns were then defined by standard photolithography. The densely packed inclined guiding terraces were fabricated by an alternating ICP etch–trim process repeated for N cycles, as schematically illustrated in Figure Sx. In each cycle, the exposed SiO_2 region was first etched using a fluorocarbon plasma with a C_4F_8 flow rate of 12.5 sccm, chamber pressure of 1.8 mTorr, RF power of 30 W, ICP power of 400 W, and etching time of 30 s. Subsequently, an O_2 plasma trimming step was performed to laterally shrink the photoresist, using an O_2 flow rate of 30 sccm, chamber pressure of 30 mTorr, RF power of 50 W, ICP power of 0 W, and treatment time of 100 s. In this alternating process, the vertical step height was mainly determined by the anisotropic SiO_2 etching depth in each cycle, whereas the lateral step spacing was controlled by the photoresist trimming amount. Repeating the etch–trim sequence enabled the formation of multiple closely spaced inclined step edges within a single lithographically defined stripe, which served as spatially registered guidance tracks for IPSLS SiNW growth. The terrace number was controlled by the number of etch–trim cycles N. After the terrace patterning process, the substrates were thoroughly cleaned using the same solvent sequence to remove residual photoresist and etching byproducts.

Indium catalyst patterning and IPSLS SiNW growth (Steps II–III). Indium (In) catalyst regions were patterned by photolithography, followed by thermal evaporation of a thin In layer and lift-off to form spatially confined catalyst pads. The substrates were then transferred into a PECVD system for in-plane SiNW growth. Briefly, an H_2 plasma treatment was applied to reduce the native oxide on In and to form isolated In droplets. An ultrathin amorphous Si (a-Si) precursor layer was subsequently deposited, and in-plane solid–liquid–solid (IPSLS) growth was carried out at a growth temperature below 300°C, where In droplets guided by step edges absorb the a-Si precursor and crystallize into directionally aligned SiNWs.

Removal of remnant a-Si and post-growth annealing (Step IV). After growth, the remnant a-Si film was removed by CF_4-based RIE, followed by an O_2 plasma cleaning step to eliminate carbonaceous residues. The SiNWs were then annealed in dry O_2 to stabilize the nanowire surface/oxide and improve device-to-device reproducibility.

Source/drain formation (Step V). Source and drain electrodes were defined by photolithography. Prior to metallization, the exposed SiNW regions were briefly treated with buffered oxide etchant (BOE) to remove native oxide and improve electrical contact. Pt/Au was deposited by electron-beam evaporation (Ti as adhesion layer), followed by lift-off to form the source/drain contacts.

High-k gate dielectric deposition (Step VI). A conformal high-k gate stack consisting of 3 nm Al_2O_3 and 10 nm HfO_2 was deposited by atomic layer deposition (ALD). Unless otherwise stated, devices were used as-fabricated; for the RTP-treated control samples, rapid thermal processing at 300°C for 2 min was performed after dielectric formation.

Dielectric via opening and drain-bus fabrication (Steps VII–VIII). To enable array-level addressing and selective erase control, via windows were patterned on the dielectric to expose the underlying drain pads (and/or designated bus-contact regions). The Al_2O_3/HfO_2 stack in the via regions was etched to open contact holes. Subsequently, the drain bus (drain line) metallization was defined by photolithography and metal deposition to electrically connect drains along the array direction.

Top-gate metallization and array interconnects (Steps VIII–IX). Top-gate electrodes and gate lines were patterned by photolithography, followed by deposition of Ti/Au and lift-off. Finally, lithography-defined interconnects were completed to form the

source, drain, and gate lines of the 4 × 4 SiNW-FET array, enabling addressable operation across the array.

4.2 | Electrical Measurements

All electrical measurements were performed at room temperature using a Keithley 2636B source-measure unit. The electrical measurement protocols were implemented in Python (custom scripts for instrument control and data acquisition). Transfer characteristics were measured by sweeping gate voltage while applying a constant drain bias; output characteristics were obtained by sweeping drain voltage at different gate biases. For pulse measurements, gate pulses were applied to program the device state under forward drain bias ($V_{DS} > 0$, "write/update"), and a reverse drain bias hold ($V_{DS} < 0$) was used as an explicit erase/reset operation between segments to restore the baseline state. The pulse amplitude, width, interval, and pulse number were varied to quantify amplitude-dependent programmability, rate dependence, and dual-timescale decay dynamics.

4.3 | FET-TCAD

We utilized the Silvaco-TCAD simulator to model the p-type SiNW-FET.

4.4 | DVS-Gesture Inference Simulation

The event-stream gesture-recognition simulations were carried out in Python; implementation details are provided in Note S5.

4.5 | AI-Assisted Editing and Schematic Illustration

During the preparation of this manuscript, the authors used ChatGPT (OpenAI) for language polishing (grammar, clarity, and conciseness) and used [IMAGE TOOL] to generate initial drafts of cartoon-style schematic illustrations in Figure 1b and Figure 5a. All AI outputs were reviewed and edited by the authors, who take full responsibility for the content. AI tools were not used to generate, alter, or manipulate any experimental data, results, or data-driven figures.

Author Contributions

L.Y. carried out the experiments, analyzed the data, performed the application-level simulations, and wrote the manuscript. Y.Z., W.T.Q. and X.P.S. participated in the experiments. M.W. participated in the application-level simulations. G.S. contributed to the mechanism analysis. Z.H. performed TCAD simulations. W.L., J.W., and L.Y. supervised all phases of the research and revised the manuscript.

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Conflicts of Interest

The authors declare no conflicts of interest.

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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Supporting Information

Additional supporting information can be found online in the Supporting Information section.

Supporting File: adfm77601-sup-0001-SuppMat.pdf.