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Topical Review

Review on 3D growth engineering and integration of nanowires for advanced nanoelectronics and sensor applications

Ruijin Hu and Linwei Yu

National Laboratory of Solid-State Microstructures/School of Electronics Science and Engineering/ Collaborative Innovation Center of Advanced Microstructures, Nanjing University, 210093 Nanjing, People's Republic of China

E-mail: yulinwei@nju.edu.cn

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Abstract

Recent years have witnessed increasing efforts devoted to the growth, assembly and integration of quasi-one dimensional (1D) nanowires (NWs), as fundamental building blocks in advanced three-dimensional (3D) architecture, to explore a series of novel nanoelectronic and sensor applications. An important motivation behind is to boost the integration density of the electronic devices by stacking more functional units in the *out-of-plane* *z*-direction, where the NWs are supposed to be patterned or grown as vertically standing or laterally stacked channels to minimize their footprint area. The other driving force is derived from the unique possibility of engineering the 1D NWs into more complex, as well as more functional, 3D nanostructures, such as helical springs and kinked probes, which are ideal nanostructures for developping advanced nanoelectromechanical system (NEMS), bio-sensing and manipulation applications. This Review will first examine the recent progresses made in the construction of 3D nano electronic devices, as well as the new fabrication and growth technologies established to enable an efficient 3D integration of the vertically standing or laterally stacked NW channels. Then, the different approaches to produce and tailor more sophisticated 3D helical springs or purposely-designed nanoprobes will be revisited, together with their applications in NEMS resonators, bio sensors and stimulators in neural system.

Keywords: 3D nanostructures, stacked nanowires, helical structure, bio probes and sensors

(Some figures may appear in colour only in the online journal)

1. Introduction

Quasi one-dimensional (1D) nanowires, with typical diameter ranging from tens to hundreds nanometers, have been intensively investigated over decades for the construction of a new generation of high performance field effect transistor (FET) [1–6], NEMS device [7–9], mechanical sensor [10], gas sensors [11–13], nanophotonics [14–16] and bioelectronics [17–19]. These 1D building blocks can be fabricated via either high precision top-down lithogrpahy and etching processes [20–22] or bottom-up self-assembly approaches [7, 23–26]. The latter are mostly catalyzed by nanoscale metal catalyst droplets, via for example the famous vapor–liquid–solid (VLS) mechanism [27, 28]. Indeed, there are already plenty of excellent Reviews on the different growth mechanisms of the 1D NWs in the literature [29, 30], as well as their broard applications in solar cells and photovoltaic [31], MOS capacitors [32], energy storage devices [33, 34]. In this Review, we will focus on the latest progresses on the 3D growth control and engineering of 1D NW building blocks, and their new applications in advanced logics and sensors. Though most of the NW-based electronics and sensors have

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been fabricated/prototyped on planar substrate surface, the potential to assemble and integrate them in the *out-of-plane* or the *z*-axis space, as vertically standing [35–38] or laterally stacked channels [39–41], is attracting more and more research attentions and efforts in recent years. The benefit of such 3D integration of NW channels is apparent, as it enables a new architecture that can substantially reduce the device footprint area, a badly needed capability to boost the integration density further and extend the evolution of Moore's law. However, conventional planar lithogrpahy is difficult or inefficient, if not incapable, to pattern 3D nanostructures, and this challenge invokes the need of developping new fabrication strategy to produce or arrange these tiny 1D building blocks into precise locations in 3D architecture. For example, standing silicon nanowires (SiNWs), grown by bottom-up VLS methods, can serve as ideal vertical channels to construct vertical FETs with advantageous gate-all-around (GAA) configuration [42–44]. Or, the horizontal SiNW channels can be stacked up [5, 45, 46], similar to the fin-FET but now with more efficient channel modulation due to the GAA configuration. The key technologies and the major progresses observed in these fields, as well as the obstacles that hinder their widespread uses, will be examined in the first section of this Review.

In the second half, the focus will be given to an unusal potential of the 1D NWs, which, compared to their 0D dots and 2D sheet counterparts, can be more easily engineered into a series of more fascinating and functional nano complexes, such as tailored bioprobes [47], single or double helices [48–51], elastic 3D springs or even woven into networks [52–55]. These capabilities are indeed outstanding and have developped into vibrant research fields over the last decade, aiming at a new generation of bio probing and sensing technologies [56–58], NEMS or optomechnical resonators [59–61], strechable electronics [52] and even chiral optics [62, 63]. However, most of these geometry engineered 3D NW complex structures cannot, or are difficult to, be fabricated directly via planar lithography and etching procedures. So far, there are two major approaches, recently established, to construct 3D nanostructures. The first one is best represented by the local deposition technology induced by focused ion or electron beams, named as FIBID or FEBID respectively [48, 64]. During a nanoscale additive deposition, the precursor gases are dissociated by the focused electron or ion beams to deposit only at the regions directly under or at the promixity of the focus points. This thus enables a precise 3D piling of different ingredient materials that can be as diverse as metals of Co [65], Au [66], Pt [67] and W [68] or dielectric materials of SiO_2 [69], carbon [70]. Similar approaches are also developed, with the aids of focused laser beams, to print 3D mesoscale structures, but the diameters of the resulted 3D structures are usually much thicker, as limited fundamentally by the laser beam wavelength [71].

The second approach is to rely on self-assembly synthesis, which is usually assisted by using nanotemplate [72] or asymmetrical blocking of nuclei [73] in solution environment. Under proper parametric control, ultra long nanohelices can be easily fabricated in batch at even room temperature [74]. The advantages and drawbacks of these two fabrication approaches will be reviewed and compared, together with their potential applications for chiral optical and elastic functionalities. Then, a new kind of bio prober/sensor applications will be introduced, which are constructed based on properly designed kinked or bent SiNWs. This tailored probe enables a convenient and precise field-effect sensing of the electric potential signals in the targeted cells or environment, which could find a broad range of applications in the emerging fields of bio electronics, nanoscale mapping/imaging and neural-machine interfacing [75]. At the end, the perspective of employing these 3D engineered NW structures for exploring more advanced NEMS, optomechanical, sensors functionalities and stretchable electronics will be presented.

2. Assembling NWs for 3D logics

2.1. Standing NWs as vertical channels

Vertically standing NW array have been widely explored as the advantageous 3D framework for building high performance solar cells [76–78], photodetectors [14], NEMS devices [79], bio-electronics [80], FETs [81], gas sensors [82] and mass sensors [57]. Usually, the vertical NWs or nano pillars are produced via a VLS growth approach [42, 83, 84], where molten catalyst droplets, typically gold (Au), are used to absorb the vapor-phase precursor gases, such as SiH_4, to establish a supersaturation of the dissolved Si atoms in the droplets. Upon that, nucleation and precipitation of crystalline phase will happen usually at the bottom interface, leading to a continuous unidirectional growth of SiNWs. During this course, if the NWs can form an epitaxial contact with the underlying crystalline substrates, most of the SiNWs will grow into self-oriented array, standing on the surface as seen for example in figure 1(a). Though the VLS growth can produce ultrathin SiNWs with diameter down to a few tens of nanometers, the position and orientation control of the as-grown SiNWs are major concerns for achieving a reliable and scalable fabrication of vertical FET devices. On the other hand, orderly array of standing SiNWs or pillars can also be produced via top-down etching in Si wafer substrates, by using inductively coupled plasma (ICP) technology. The ICP dry etching has the advantages of precise position, length and diameter control over the SiNWs, while the challenge is to etch ultrathin nano pillars with a rather high aspect ratio feature and diameter below 100 nm [85].

An outstanding advantage of NW-based FETs is the beneficial GAA configuration, which allows for a maximal capacitive coupling control of the channel current. Standing NWs are particular suitable to fabricate vertical channel GAA FETs, as demonstrated in a series of pioneering works [3, 43, 81, 85, 86], as the vertical NWs can be wrapped around and gated by the surrounding electrode, without the geometric problem encountered for the NWs lying on planar substrate, where forming a surrounding gate is limited, in principle, by the touched bottom NW/substrate interface,

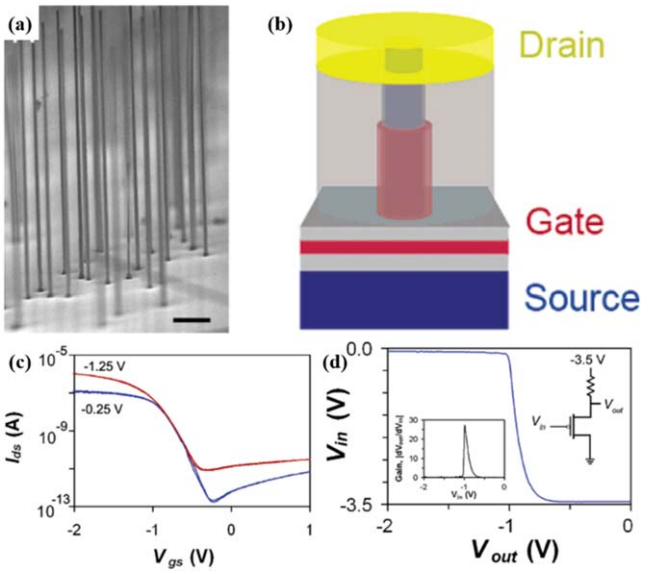


Figure 1. (a) SEM image of the vertical grown SiNWs. (b) Device configuration of vertical GAA FET. (c) Typical transfer curves of the device. (d) Output characteristics of the inverter. Reprinted with permission from [3]. Copyright 2006, American Chemical Society.

unless they are carefully undercut to form suspended NW channels.

A typical vertical channel FET device has been fabricated by Goldberger *et al* [3], as seen in figure 1(a), where the standing SiNW channels were grown by using $SiCl_4$ as precursor and BBr_3 as dopant, via a VLS process catalysed by Au droplets. Scanning electron microscope (SEM) image of the SiNWs and the schematic illustration of the GAA FET devices are shown in figures 1(a) and (b), respectively. Note that, the vertical FET device consists of 20 NWs in parallel as channel with diameter around 30 nm. The dielectric layer is a conformably coated SiO_2 layer of 30 nm thick, with a gate length of 1.0 μm to 1.5 μm. As shown in figure 1(c), the prototype GAA FET device demonstrates typical on/off ratio $>10^5$, SS of 120 mV/dec and average hole mobility of 52 $cm^2\ V^{-1}\ s^{-1}$. In addition, by connecting the FET with a resistor of 200 MΩ, an inverter logic was realized with a voltage gain of ∼28, as shown in figure 1(d).

Heteronanowires, such as Ge/Si core/shell NWs, can also be used as vertical channels for building GAA FET [44], where a high density gas of holes can be accumulated within the Ge NW cores, thanks to the type-II band alignment between c-Si and c-Ge [87]. In this structure, the Ge NWs were first grown via VLS mechanism, standing on the heavily doped Si substrate, followed by an epitaxial growth of a thin layer of Si shell with thickness of ∼2 nm, as seen figure 2(a). By using 10 nm Al_2O_3 as dielectric layer and 50 nm tungsten (W) gate electrode, patterned by SF_6 etching in the reactive ion etching (RIE) system with poly (methyl methacrylate) (PMMA) mask, the gate length is controlled from 414 nm to 772 nm, by varying the thickness of the PMMA layer, as seen in figures 2(c), (d). The Ge/Si NW FETs with a gate length of 544 nm achieved an on current of 750 $\mu A\ \mu m^{-1}$, SS of 125 mV/dec and a hole mobility of 282 $cm^2\ V^{-1}\ s^{-1}$, as seen in figure 2(b), while a pseudo-CMOS inverter logic was also

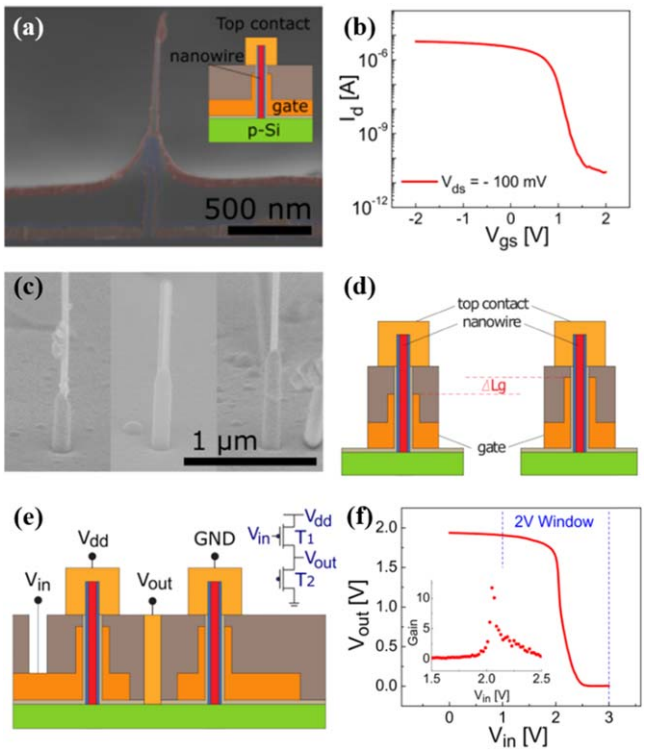


Figure 2. (a) SEM image of vertical FET with different layers highlighted with false colours. (b) Transfer curve of the device. (c) SEM images showing the height of remaining W gate region using different kinds of PMMA. (d) Schematic of devices with different gate lengths. (e) Illustration of inverter consisting of two p-type FETs. (f) Voltage transfer characteristics of the inverter. Reprinted with permission from [44]. Copyright 2016, American Chemical Society.

fabricated by using two p-channel FETs (with a configuration as depicted in figure 2(e)), showing a voltage gain >10 as plotted in figure 2(f).

Despite of the successful demonstration of vertical NW FET prototypes, there are still several drawbacks, at this moment, that hinder a scalable implementation for this 3D FET device: (i) the VLS growth is not fully compatible with the standard Si integration process, particularly for the use of Au as catalyst which is a known to introduce detrimental recombination centres in c-Si [88]; (ii) even the SiNWs can be produced via alternative catalyst metals that are acceptable to Si integration processes, a more stringent diameter and orientation control of the SiNWs has to be established for reliable device application; (iii) more importantly, the electric connection to the 3D vertical FET units is far more complicated and expensive than that in planar device architecture, which has to be largely simplified for practical and economically feasible applications; (iv) finally, the device simulation, design and verification toolkits specified for the 3D FET circuitry are largely lacking or still at infantry stage.

2.2. Stacked NWs as horizontal channels

In face of the technical difficulties encountered in fabricating and integrating upright standing NWs as vertical channels for FET, a more practical and convenient strategy is to stack the

horizontal NW channels in a pile, which can also substantially reduce the footprint area for the FET channels while achieving a large drive current. Note that, this stacked NW configuration can also be viewed as the more advanced 3D channel structure, evolved from the mainstream fin-FET structure. GAA channel architecture has been adopted in the latest technology node at 3 or 5 nm, according to the announcement by Samsung and IBM [89]. The benefit of such stacked channel design is to allow the construction of GAA FET within the mature CMOS logic architecture, which is extremely important for scalable and practical device applications. So far, there are mainly two distinct strategies to batch fabricate such stacked NWs, one is the selectively top-down etching of Si/SiGe multilayers [1] or via template-assisted Bosch-etching [90], and the other relies on a 3D sidewall guided growth of parallel NWs via a relatively new in-plane solid–liquid–solid (IPSLS) mechanism [45, 46, 91]. While the former is dedicated to the cutting-edge microelectronics, the latter is particularly suitable for large area electronics that need to be fabricated at lower temperature over glass/polymer substrates, such as the thin film transistor (TFT) back panel logics in planar display [45].

It is widely known that SiNWs can also be produced via low cost and high yield self-assembly approaches, but the challenge is how to arrange these SiNWs into orderly stacks. Though VLS-grown SiNWs have been transferred and aligned into orderly array on planar surface by different technologies, such as contacting printing [92–94], blow bubble film [95–97] and Langmuir–Blodgett [98–100], or the SiNWs can be grown directly on the vertical sidewalls over the gaps to form suspended bridges [101], integrating these tiny SiNWs as stacked horizontal channels in a 3D architecture remains still an extremely difficult, if not impossible, mission.

This difficulty can be alleviated if the self-assembly growth can be confined tightly to the out-of-plane sidewall surfaces of 3D framework or structures. For example, during an IPSLS growth process, a thin film of solid amorphous silicon (a-Si), instead of silane (SiH_4) gas in typical VLS growth [102], is deposited to serve as precursor for the growth of SiNWs with the aid of nano catalyst droplets of indium (In) or tin (Sn) [53, 102–109]. While this growth is called in-plane, it is by no means limited to planar or flat surfaces. Instead, these in-plane growth of SiNWs can happen on basically any surface, as long as it is pre-coated with a-Si layer, regardless of it being flat, oblique, vertical or curved sidewalls [45, 46]. This unique feature thus enables a new dimension to grow and deploy the SiNWs orderly in 3D architecture.

In general, a typical IPSLS growth of SiNWs will involve four major steps, which include (i) the deposition of a thin film catalyst of In (Sn or their oxide) by using thermal or electron beam evaporation, which is then treated by using H_2 plasma at 200 °C–250 °C in PECVD system to remove the oxide layer and to form discrete In nanodroplets; (ii) after that, an a-Si layer is coated on the surface by SiH_4 plasma at 100 °C–180 °C, followed by (iii) an annealing in vacuum or H_2/N_2 ambient at typically 350 °C. During the annealing, the molten In droplets start to absorb the nearby a-Si layer and produce continuous crystalline SiNWs along their moving courses. At the end, (iv) the remnant a-Si layer can be selectively etched off by low temperature H_2 plasma or RIE etching. Notably, as the SiNWs are tightly confined to the surface coated with a-Si precursor, in a strong contrast to the free growth of VLS SiNWs with gaseous precursor, the in-plane movement of the SiNWs can be effectively attracted and guided by simple step edge lines, pre-patterned on the substrate surface [107]. This thus enables a precise position and orientation control over the in-plane SiNWs [108], which is a fundamental capabilities required to achieve scalable device applications in the mainstream planar electronic architecture [110]. Meanwhile, the in-plane growth is not limited to planar growth, instead as the influence of gravity is negligible compared to the surface and interface tension forces for the tiny droplets, this IPSLS growth of SiNWs, led by catalyst droplets, can be readily extended to any surface that is coated with a-Si thin film supply [45, 46].

For example, Wu *et al* recently demonstated that the in-plane growth of parallel SiNWs can be carried out upon oblique sidewalls, which consist of multiple terraces or mini-steps formed via a simple alternating etching process [45]. Specifically, as depicted in figures 3(a), (b), photoresist strips of 2 μm wide and ~1.5 μm thick were first patterned on SiO_2 substrate. Then, a C_4F_8 plasma etching was applied to etch into the SiO_2 layer to form the first mini-steps, followed by an O_2 plasma burning to narrow the photoresist, causing the edges to retreat inwards. By repeating these two steps alternately for N times, N mini-steps will be produced on the oblique sidewalls, with tunable the step height and width by adjusting the etching and burning durations. Figures 3(c), (d) show the SEM images of an array of pyramids with oblique sidewall of 4-layer terraces, where the height and width of the mini-steps are of 160 nm and 120 nm, respectively. After that, In catalyst strips were deposited crossing the guiding terraces and the SiNWs were produced via standard IPSLS growth procedure. As seen in figures 3(e)–(h), very thin SiNWs can be produced now as a dense array with average diameter of 50 nm and NW-to-NW spacing of <100 nm. Remarkably, these SiNWs can also be released via hydrofluoric acid (HF)-etching to form parallel suspended bridges, with a length of 50 μm supported SiO_2 stakes at the two ends. Prototype fin-FET devices fabricated upon the SiNW array grown on oblique sidewalls demonstrated an impressive on/off current ratio of 10^7, SS of 330 mV/dec, a low leakage current $<10^{-13}$ A [45].

In order to reduce the footprint area of the SiNW further, the authors tried also more aggressive sidewall-confining approach, that is, to pattern the guiding grooves on vertical sidewalls and grow the SiNWs as vertical stacks. This can be accomplished via a selective etching of the exposed and truncated sidewalls of the multilayers of SiO_2/SiN_x, where the oxide layer can be etched off at a higher rate than that for the nitride layer. As shown in figures 4(a), (b), SiO_2 and SiN_x multilayers with suitable thicknesses were first deposited on planar Si wafer substrate, followed by a dry C_4F_8 plasma etching to expose the truncated sidewalls. Then, the samples were dipped into 5% HF solution to develop concave grooves

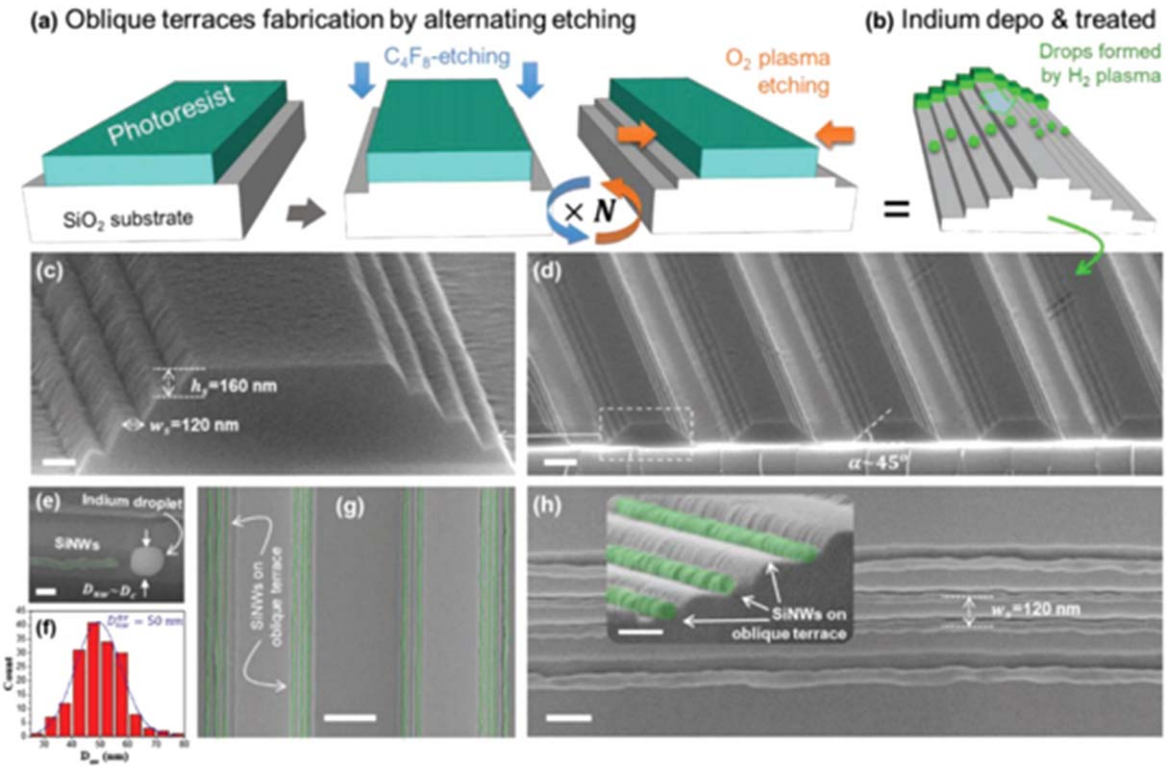


Figure 3. Oblique terrace guided growth of SiNWs. (a)–(b) Fabrication procedure of the oblique sidewall terraces. (c), (d) SEM images of the as-produced empty terraces. (e)–(h) The top-view and side-view SEM images of the SiNWs upon oblique terraces. (f) A statistic over the diameter of SiNWs. Scale bars in (c), (e) and (h) stand for 200 nm, (d) and (g) for 1 μm, the inset of (h) for 100 nm. Reproduced with permission from [45]. Copyright 2019, Wiley-VCH.

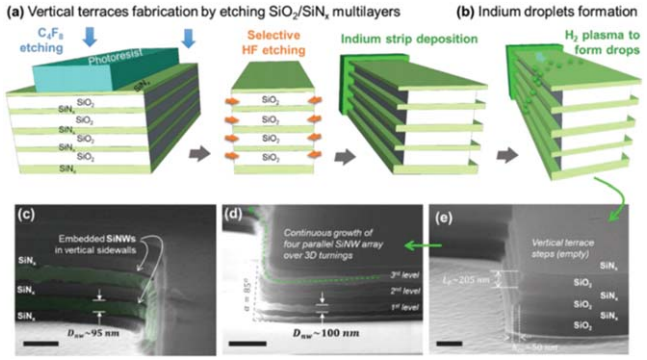


Figure 4. (a), (b) Schematic of the fabrication procedure based on SiO_2/SiN_x multi-layers. (c)–(e) SEM images of the vertical grooves with or without SiNWs. Scale bars in (c)–(e) were 300, 600 and 400 nm. Reproduced with permission from [45]. Copyright 2019, Wiley-VCH.

on the sidewalls. Note that, the height and depth of the concaves can be precisely controlled by tuning the thicknesses of the SiO_2 and SiN_x layers and the HF etching time, respectively. The as-produced sidewall grooves, as seen for example in figure 4(e) with height of 205 nm and depth of ~50 nm, provide ideal guiding tracks for the movement of the In droplets to produce parallel and stacked SiNWs, which, as seen in figures 4(c), (d), can be directed to grow continuously over corners without significant diameter variation. In principle, these 3D stacked SiNWs have roughly the same footprint of a single SiNW on planar surface, which is an important advantage to boost the drive current of GAA FETs while keeping a minimized channel area.

The 3D sidewall growth of stacked SiNWs can also be accomplished upon a more convenient sidewall structure, that is on the Bosch-etched scallop-shaped surface, which can be easily produced during a typical high-aspect ratio etching into c-Si wafer [46]. Importantly, the need for pre-deposited SiO_2/SiN_x multilayers is avoided, as the formation of multiple parallel guiding grooves on vertical sidewall surfaces can now be done in a single etching process. Hu *et al* [46] have demonstrated that, by adjusting the gas flow and passivation conditions in Bosching process, multilevels of sidewall guiding grooves can were fabricated on the vertical sidewalls, with optimal groove height and depth of ~90 nm and ~40 nm, respectively. In addition, to isolate the SiNWs from the c-Si wafer substrate, a thin layer of SiO_2 was oxidized beforehand, as seen in the cross section SEM image shown in figure 5(a) while figure 5(b) shows the deposited In catalyst layer on the sidewall. It should be noted that the diameter of the In droplets should be controlled to be similar to the height or width of the sidewall grooves, in order to achieve a stable guided growth of SiNWs, of which the diameter is proportional to the size of In droplets, as indicated in figure 5(c). As shown in figures 5(d)–(f), a rather high growth rate was achieved on the sidewall grooves, which produces parallel SiNWs with diameter of 55 nm and NW-to-NW spacing of 90 nm. By choosing the c-Si wafer as a convenient vertical sidegate, SiNW FET devices were fabricated that achieved an

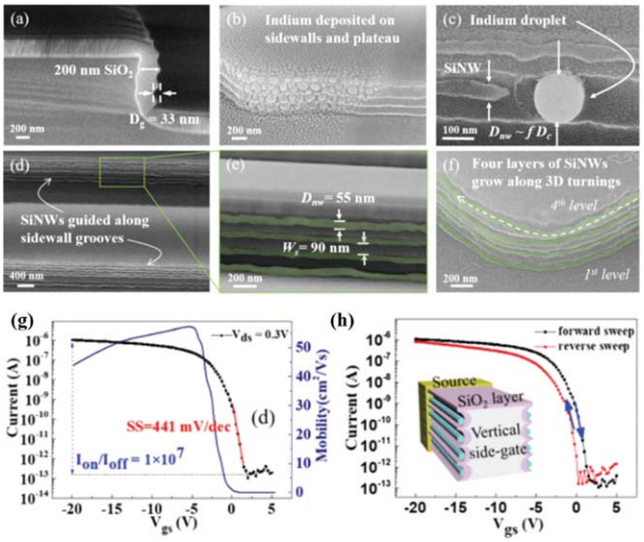


Figure 5. SEM images of (a) the cross-section of the oxidized grooves. (b) after In catalyst deposition. (c)–(f) After SiNW growth. (g) The transfer curve and the extracted hole carrier mobility. (h) The transfer curve measured in forward and backward scans, with the inset showing the cross-section diagram of the vertical side-gate FET structure. Reproduced with permission from [46]. Copyright 2020, The Royal Society of Chemistry.

on/off ratio of 10^7, SS of 441 mV/dec and hole mobility of 57 $cm^2\ V^{-1}\ s^{-1}$, see figures 5(g), (h).

In order to enable the practical application of self-grown SiNW array in semiconductor line in the industry, uniformity of as-grown SiNWs has to be guaranteed since the diameter is the key parameter that controls their physical and electrical properties. Although the possibility of 3D stacked SiNWs array fabricated via IPSLS is demonstrated, the diameter uniformity of the as-grown SiNWs still needs to be greatly improved. Similar to the VLS growth of SiNWs, the diameter of SiNW is determined by the size of the metal catalyst droplets. Hu *et al* [91] shown that a uniform formation of catalyst droplets can be achieved by confining the In atom surface diffusion on the ultra-narrow and uniform sidewall grooves with width smaller than twice of the diffuse length of catalyst adatoms on the surface. Thus, the random agglomeration of the catalyst droplets was suppressed compared with those formed on a planar surface, as indicated in figures 6(a)–(c) with corresponding model illustrations shown in figures 6(d)–(f). To boost the uniformity further, the random size fluctuation arising from the droplet merging between the edge-sitting and groove-sitting droplets can be suppressed by using a thinner nitride layer, as demonstrated in figures 6(d)–(e), while the SiNWs grown under different situations were showcased in figures 6(g)–(i). Statistics of the droplets and the as-grown SiNWs are provided in figures 6(j)–(l), which indicate that with a proper control of the catalyst droplets, an unprecedented uniform 3D integration of 10-layer stacked SiNWs array has been accomplished, with diameter deviation below 9% and NW-to-NW spacing of only 40 nm. Figure 7 shows the typical SEM images of the stacked SiNWs, where the SiNWs were tinted to green for clarification. Besides, the sidewall growth of such uniform SiNWs can be rather stable

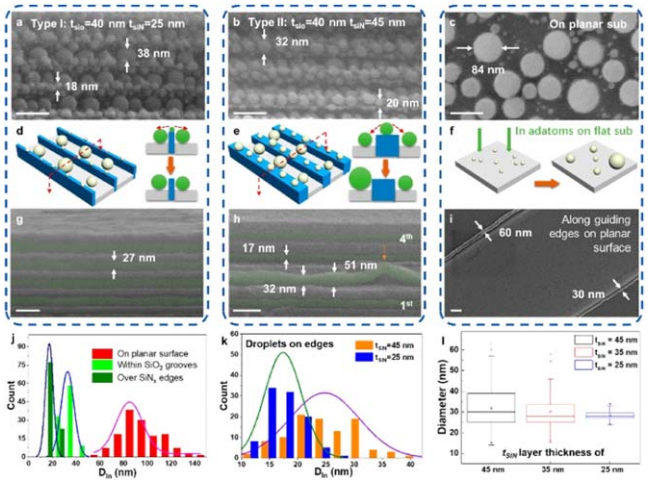


Figure 6. (a)–(c) Typical SEM images of In droplets on the sidewall or on the planar, while the corresponding models for droplets merging during the annealing process are illustrated in parts (d)−(f). (g)–(i) SEM images of SiNWs grown with different nitride edges or on the planar. (j)–(l) Statistics on In droplet size and the diameter of SiNWs. The scale bars in parts a, b, c, g, and h are for 100 nm, and that in part i is for 200 nm. Parts (a)–(j): Reprinted with permission from [91]. Copyright 2020, American Chemical Society.

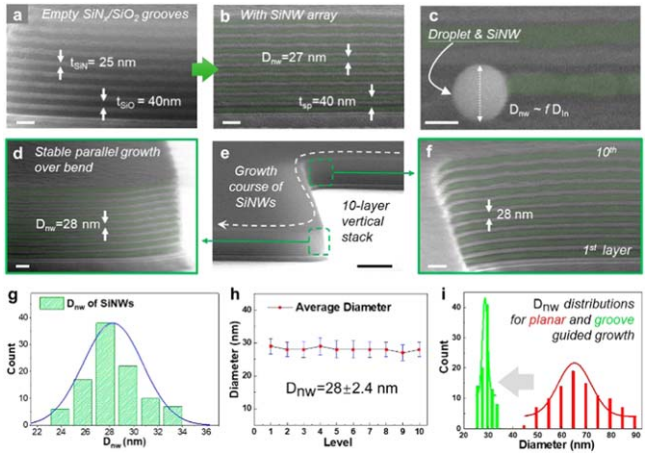


Figure 7. Morphology and statistics of 10-layer stacked SiNWs. (a) Typical SEM image of the empty sidewall grooves. (b) The side-view SEM image of 10-layer stacked SiNWs. (c) The SiNW led by In catalyst droplets, where D_{nw} is proportional to D_{In}. (d)−(f) The continuous growth of SiNWs over turning corners. (g)−(i) Statistics on diameters of SiNWs grown via PSG and planar growth. The scale bars in parts a, b, d, and f are for 100 nm, that in part c is for 50 nm, and that in part e is for 1 μm. Reprinted with permission from [91]. Copyright 2020, American Chemical Society.

as witnessed in figures 7(d)–(f), where ultralong SiNWs are observed to grow more than 40 μm, over two turning corners, without significant change of the diameter, which is in strong contrast to the much thicker reference SiNWs with apparently much larger size dispersion obtained on planar surface via a similar process, as highlighted in figure 7(i). The statistics of SiNW diameter is shown in figures 7(g), (h).

It is important to note that these stacked horizontal SiNWs grown via self-assembly bottom-up approaches can be

produced at a relatively low temperature (350 °C), making them ideal candidates for large area and flexible electronics, without the use of any high-resolution lithography technologies. For example, the in-plane SiNWs have been explored as beneficial channels for building high performance thin film transistors (TFTs) [111], and the tailored SiNWs with elastic geometries can be used for highly stretchable c-Si channels [112] or connected as quasi-continuous network [53]. But there are still several challenges that should be noted, (i) a complete set of doping and passivation control has to be demonstrated, as these are the critical aspects for high performance electronics and for building complementary electronic logics; (ii) in order to achieve high density integration, both the NW-to-NW spacing and the SiNW diameter have to be scaled down while preserving the channel uniformity.

2.3. Compatibility and scalability of 3D-grown NWs

In view of implementing these new 3D NW growth technologies, in vertical or stacked lateral channels, within the standard CMOS fabrication paradigm, there are several critical issues that should be considered and assessed systematically:

(i) First of all, a more comprehensive understanding and a reliable procedure have to been established to prevent/or contain the potential impacts of the use of metal catalyst droplets, which are however indispensible for both the VLS and IPSLS growth of NW structures. Actually, it has been well known that the incorporation of catalyst metal atoms, like Au, into the c-Si will introduce very efficient mid-bandgap recombination centers [88] that are definitely detrimental for high performance front-end logics and thus should be avoided. In this aspect, the use of alternative catalyst of In, Sn, Bi and Ga for both VLS [76, 78, 113] or IPSLS [102, 108, 111, 114, 115] growth of SiNWs are better choices. Particularly, Sn lies in the same Column of Si in the Periodic table, and thus the incorporation of Sn atom has no catalyst-atom-induced doping effect in the c-Si, making it more suitable for both n-type and p-type doping of SiNW channels for CMOS logics.

(ii) Second, even the metal-catalyzed growth approaches are not immediately compatible to the standard fabrication of the front-end logics, they are still ideal channel choices for the the construction of various back-end logics, memory and even sensors. As these back-end devices are supposed to be fabricated directly upon the front-end logics, there is a strigent thermal budget limit, that is, the process temperature of the back-end devices should be lower than $<$450 °C. To this end, the metal droplet catalyzed growth has an outstanding advantage, as most of them can proceed at a relatively low temperature $<$500 °C, particularly for the IPSLS approach where a group of low melting point metals, such as In, Sn and Ga, are used as catalyst [116, 117]. Note that, 3D monolithic stacking integration of logic/memory units in the back-end layer has been widely considered as a promising new architecture to overcome the fundamental limitations in the traditional von-Neumann architecture, and to achieve higher integration density, faster operations and explore new neuromorphic functionalities [118, 119].

(iii) Third, as the most important capability for scalable and reliable device integration, the vertical and lateral SiNW channels have to be precisely controlled and tailored, in terms of the position, diameter, crystalline orientation and doping polarity. The adoption of vertical VLS-grown SiNWs as FET channels requires a complete rearrangement of the contact and gating scheme or device architecture, which are still ongoing and underdeveloping research topics without a mature solution [43]. In comparison, the IPSLS growth of stacked SiNWs offer a more practical routine, which could be directly integrated with the established S/D contact and gating technolgies for GAA-FET device fabrication. To be competitive, scaling the diameter of the IPSLS-grown stacked SiNWs further, down to $\sim$10 nm (at least in dimension) and with a size uniformity comparable to that of the top-down Si/SiGe channels [40, 41] fabricated with the aid of EUV and etching, is a major challenge that demands profound understanding and greatly improved growth dynamic control of the tiny catalyst droplets/NW system.

3. Curved NWs engineered as 3D complexes

3.1. Helical structures

More complicated 3D structures can also be obtained, engineered or assembled based on the 1D NW building blocks. Among them, nano-scale helical structures are finding extensive applications in actuators [120] and sensors [121, 122], optical devices [62, 123], superconductor [48], telecommunication [124], biomedical-robots [122, 125] and NEMS devices [126]. However, fabrication of this 3D nanostructure is rather difficult, if not impossible, by using planar lithography techniques. On the other hand, focused ion beam induced deposition (FIBID) technology [48, 62, 65, 127–130], as a representative of the advanced nanofabrication tools, is able to prepare complicated three-dimensional structures in a small feature size. The FIBID system consists of a gas injection system (GIS) that delivers the precursor gas into the deposition chamber at the certain position and a focused ion beam (FIB) that dissociates the precursor gas. The volatile part is pump out of the chamber while the solid non-volatile part deposits on the substrate to form the specified shape. With the assistant of computer-controlled system, the FIB can scan the desired region automatically and accomplish the programmed structure [131, 132]. To ensure the successful fabrication, the ion current, the beam dwell time, the angle between GIS and substrate and the distance between FIB and substrate should be optimized.

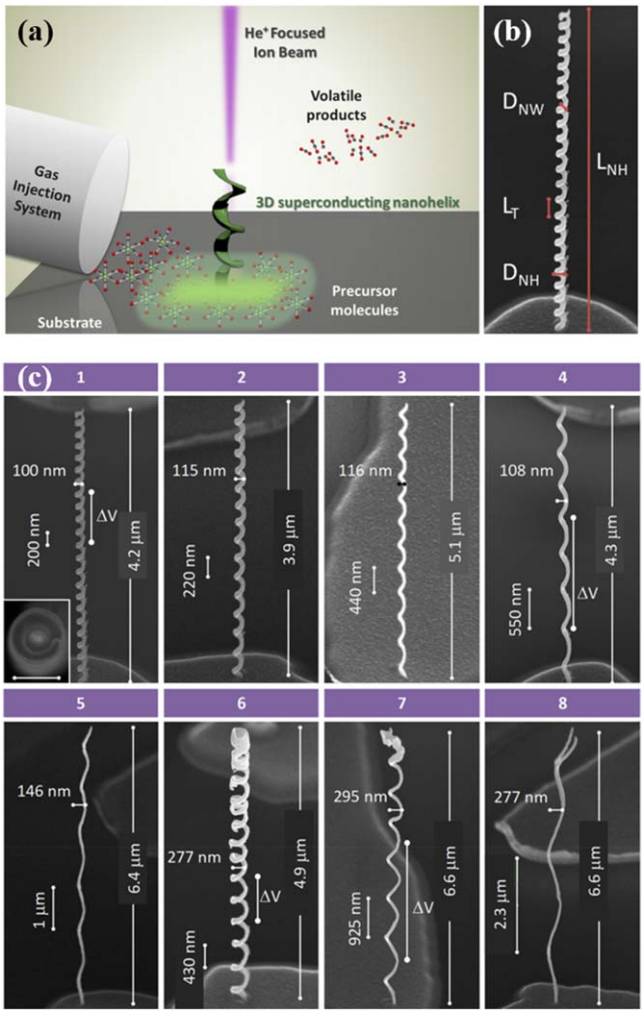


Figure 8. (a) Sketch of the growth of 3D nanohelix. (b) A typical SEM image of the helix. (c) SEM images of nanohelices of several types (from 1–8). Reprinted with permission from [48]. Copyright 2019, American Chemical Society.

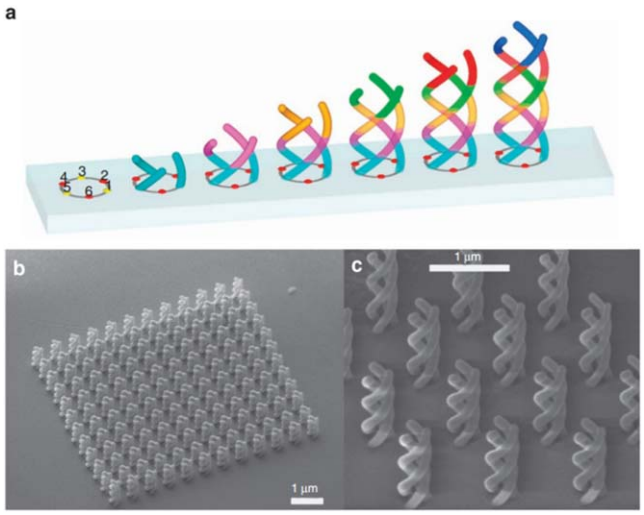


Figure 9. (a) Fabrication scheme to realize triple-helical nanowires. (b), (c) SEM images of the helices array. Reprinted by permission from Springer Nature Customer Service Centre GmbH: Springer Nature, Nature Communications, [62], Copyright © 2015, Nature Publishing Group, a division of Macmillan Publishers Limited. All Rights Reserved.

For instance, Córdoba *et al* [48] prepared the vertical nanohelices with diameter of 100 nm and NW diameter as small as 45 nm using the He^+ gas-FIB source and $W(CO)_6$ precursor. A diagram of the FIBID system and a typical SEM image of the nanohelix were illustrated in figures 8(a), (b). Normally, the helical structure is the key factor that effecting their properties. Eight different types of nanohelices were prepared with pitch from 200 nm to 2.3 μm, helix diameters between 100 nm and 295 nm, helix length up to 6.6 μm, as dipicted in figure 8(c). The pitch of helix can be markedly changed by adjusting the beam dwell time while maintaing the fixed nominal circular diameter, even though the diameter of NW was also emlarged, as shown in figure 8(c) from type 1 to type 5. In addition, the diameter of helix (D_{NH}) can be altered by changing the nominal circular diameter as shown in figure 8(c) from type 6 to type 8.

Not only the individual helical structure but also the triple-helical NW can be prepared by FIBID technique. The multi-helical NW configuration is predicted to have the superiority in obtaining chiro-optical properties including the broadband and high signal-to-noise ratio (S/N) in the visible spectral range compared to the single helical NWs. But the realization of intertwined helical structure is difficult using conventional FIB due to the bind spot existence where the space is occupied with pre-grown NWs. By adopting the tomographic rotatory growth together with FIBID, that is dividing the growth into multiple sections [62], triple-helical NWs (THNs) can be fabricated. The fabrication procedure began with splitting a circle into six arches with 60° apart. Then, three platinum arches were deposited arranged every 120°, as shown in figure 9(a) as sites 1, 3, 5. For the following beam scan, the same structure was patterned except the scanning was anticlockwise rotated by 60°, forming the arches above the sites 2, 4, 6. By repeating the beam scanning with rotation for three times, the THNs with NW diameter of 110 nm, vertical pitch of 705 nm and external diameter of 375 nm were fabricated, as seen in figures 9(c), (d). This THNs demonstrate the excellent chiral optical features with up to 37% circular dichroism between 500 nm and 1000 nm and high S/N of 24 dB. Compared to other technologies, the FIBID technique has the advantages of high shape resolution (down to 100 nm) and smaller critical dimensions (down to tens of nanometers). While the drawbacks are the high cost due to the need of expensive equipment and high maintenance fees as well as the low yield.

Instead of using the expensive equipment, the helical structure, especially the metal helix can also be prepared in solution under ambient conditions at room temperature [49, 73, 74, 133]. The ultralong gold helices with length of several tens of micrometers, NW diameter of about 7 nm and length to diameter ratio up to >22300 were fabricated by Wang *et al* [74], as shown in figures 10(a)–(c). The helical Au NWs were prepared by incubating $HAuCl_4$, ascorbic acid, NaOH and 4-mercaptobenzoic acid (4-MBA) into ethanol/water mixture. Although the diameter of helices and pitch as defined in figure 10(f) was basically the same, they shown significant difference among different helices even though

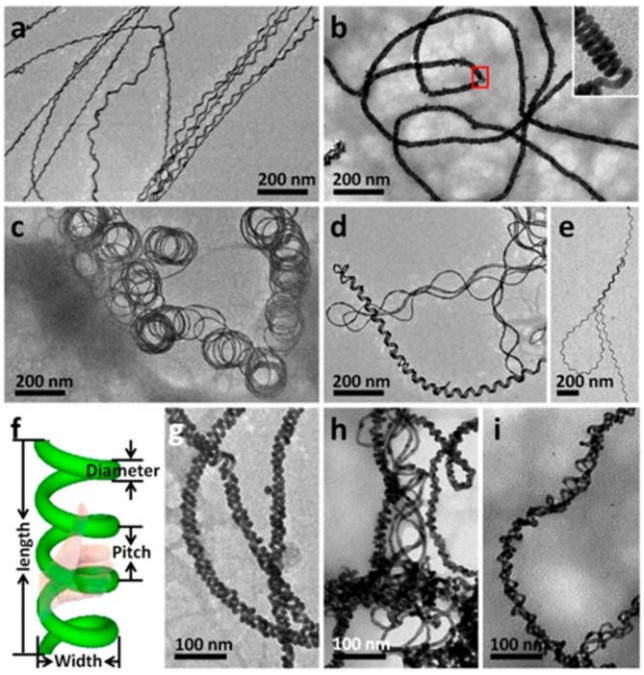


Figure 10. TEM images of different types of Au nanohelices. (a) Stretched helices with large pitch/width ratio. (b) Compact helices. (c) Helices with small pitch/width ratio. (d), (e) Folded double helices. (f) Model helix with definitions. (g), (h) Intertwined double helices (i) Triple-strand helices. Reprinted with permission from [74]. Copyright 2017, American Chemical Society.

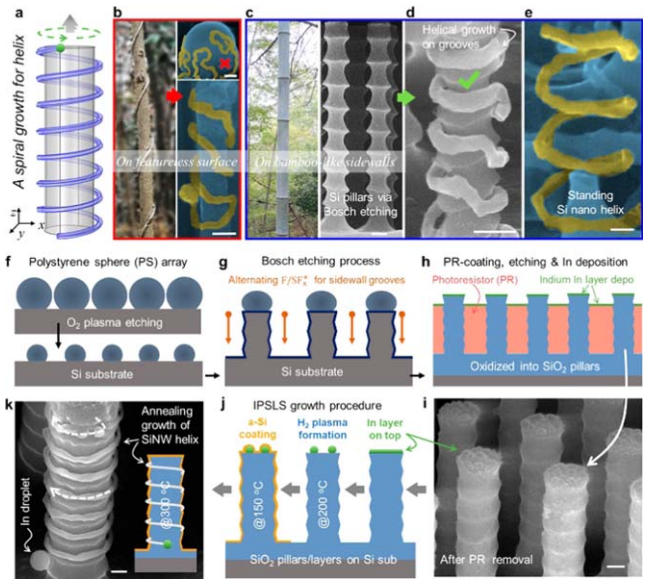


Figure 11. Spiral growth of NW on bamboolike cylinders. (a) Schematic illustration of a winding 3D growth of SiNWs cylinder sidewall to form a helical structure. (b)–(e) Photographs or SEM images of the growth of quasi-1D plant or SiNWs on featureless and bamboolike corrugated sidewall surfaces, respectively. (f)–(k) Fabrication procedure of SiNWs helix. Reprinted with permission from [134]. Copyright 2020, American Chemical Society.

they were in the same sample. For some helices, the width was small but the length was long as shown in figure 10(a). Some helices were compact with small pitch as shown in figure 10(b). Other helices tened to be looped circles for their width was much larger than pitch as shown in figure 10(c). Few helices were folded but parallel without interlocking as shown in figures 10(d), (e). Besides, 86.8% was single helices while the rest was double (figures 10(g), (h)) or multiple helices (figure 10(i)). The diameter of helices can range between 15 nm to 150 nm while the pitch distributed from 8 nm to 250 nm. The advantages of a solution method are the simple fabrication procedure and the high productivity. But its shortcoming is pretty obvious, as a high uniformity is hard to achieve over large area, as well as their diameter and pitch are difficult to be controlled or effectively adjusted.

Actually, when the top-down approach with precise controllability is combined with low-cost and high yield self-growth technique, helical structure can be conveniently prepared since producing a helix requires only a spiral growth of 1D NW on the curved sidewall surface of a cylinder, as indicating in figures 11(a), (b). Fortunately, the confined growth on the surface can be achieved via the IPSLS growth mechanism instead of the out-of-surface growth which usually happens in a traditional VLS process. Ma *et al* [134] demonstrated a growth of Si helices upon bamboolike cylinders with sidewall grooves, where the indium catalyst droplet travels around the full perimeter of a groove before switching to the neighbor vacant groove via a line-feeding transition, as seen in figures 11(c), (d). Specially, a monolayer of polystyrene spheres (PS) was used as templates after shrunk by O_2 plasma to form corrugated columns in the alternative Bosch etching process, as sen in figures 11(f), (g). It should be noted that both the periodicity and depth of the sidewall grooves can be easily adjusted during the etching. To expose the tip of column for catalyst deposition, the columns were first covered with thick photoresist (PR), followed by the thinning of PR layer by O_2 plasma etching (figure 11(h)). Finally, the growth was activated by the consuming a-Si film precoated on the surface of the column and to produce crystalline SiNW spiraling down the column, as indicated by figures 11(j), (k).

Meanwhile, the release of helices can be achieved by etching off the fully oxidized cylinders in HF solution, as shown in figure 11(e). Those free-standing helices were explored for many novel applications such as elastic spring supports, strechable devices and resonators. Figure 12(a) demonstrated a PS ball attached on top of helix by using a nanomanipulator in SEM system. After welding the ball *in situ* with deposited amorphpos carbon, the helix can be repetitively stretched to 140%, as indicated in figures 12(b), (c). Furthermore, the ability of free-standing helix as resonator was exhibited by approaching a tungsten probe applied alternating voltage of 5 V with different frequncy, as depicted in figure 12(d) while the SEM image of the as-chosen helix was shown in figure 12(e). The helix shown distinct resonant modes at different frequencies where back-forth and left-right manners were observed at lower frequencies while up-down mode happened at higher frequencies. The vibration amplitude against the frequency scan in figures 12(f)–(h) indicated three resonant peaks located at 0.42, 1.246 and 1.34 MHz, repectively. And typical SEM images during vibration were

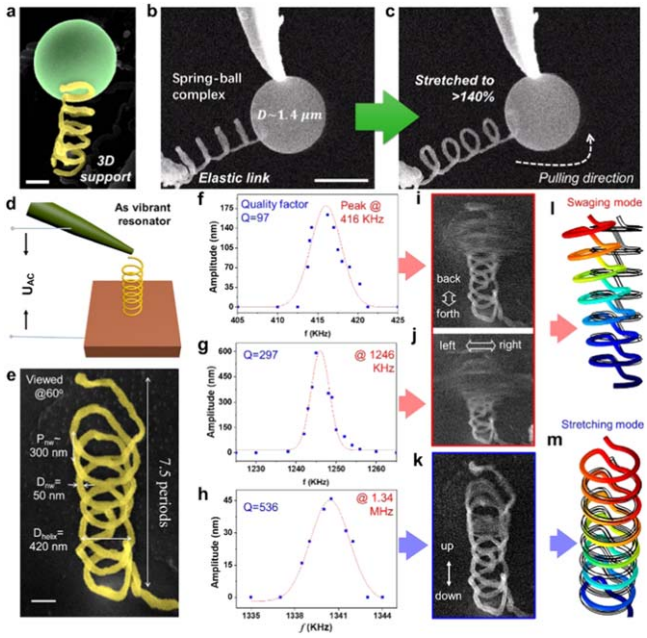


Figure 12. (a)–(c) The SEM images of the helix serving as 3D support for hybrid spring-ball complex and super elastic link before/under large stretching strain. (d) The experimental setup standing SiNH resonator testing with an SEM image shown in (e). (f)–(h) The vibration amplitude peaks for three different resonant modes with corresponding vibration SEM images presented in (i)–(k), respectively. According to finite element modeling and simulation analysis, the first two resonant frequencies are assigned to the swaging resonant modes (l) while the last one is assigned to an up−down stretching mode (m). The color rendering in the helices that varied from red to blue signifies the magnitude of displacement (from large to zero) in the resonant modes. Reprinted with permission from [134]. Copyright 2020, American Chemical Society.

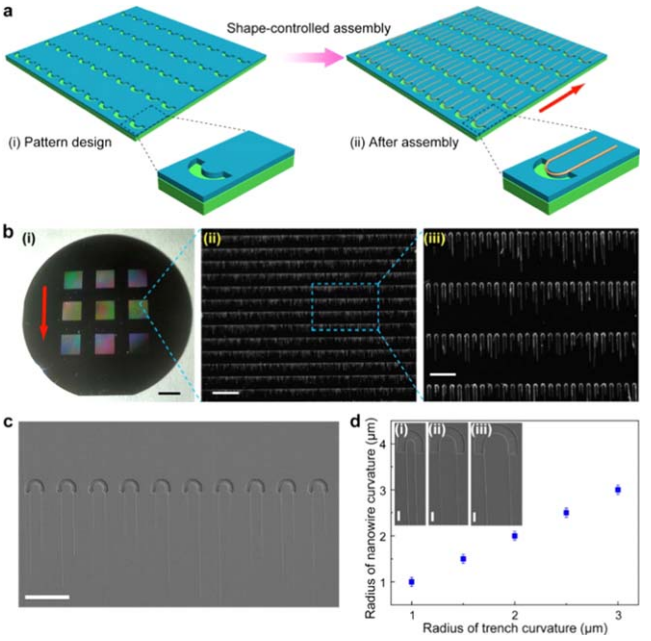


Figure 13. Shape-controlled NW assembly. (a) Schematic of deterministic assembly of U-shaped NW arrays. (b) Photograph and optical images of wafer-scale deterministically assembled U-SiNW arrays by trenches. The arrow in (i) shows the sliding direction of the NW growth substrate with respect to the target substrate. (c) Representative SEM image of U-shaped silicon nanowire array. (d) Plot of the radius of NW curvature versus the trench radius of curvature. Reprinted with permission from [137]. Copyright 2016, American Chemical Society.

demonstrated in figures 12(i)–(k), with corresponding finit element simulation results depicted in figures 12(l), (m).

Even a variety of methods have been proposed for the fabrication of helix, there are still several issues need to be addressed: (i) the fabrication of ordered arrays with precise location controllability is still need to be explored given that it is the basis for the realization of functional systems; (ii) extensive efforts need to be devoted to realizing reliable electrical connection for those 3D helices; (iii) the potential applications of the helix as resonators, strain sensors, chiral device or nanorobots have not to be fully boosted.

3.2. Kinked NW probe for bioelectronics

As a unique capability of 1D nanostructure, the tiny SiNWs can also be transformed, via geometry tailoring, into various pointy nanoprobes (NPs) to insert living cells and record intracellular signals with the minimal invasiveness [135, 136]. In particular, the semiconducting SiNPs, with passing channel current and proper dielectric layer coating, provide a power field effect sensing tool to detect and trace the local intracellular signals with rather high sensitivity, temporal/spatial precision and signal-to-noise ratio. To fabricate these SiNPs, several strategies including post-growth bending [137], kinked VLS growth [135], and *ab initio* IPSLS growth [138] fabrication have been developed. For instance, Zhao *et al* demonstrated the formation of U-shaped SiNPs by forcing the straight and long SiNWs to bend within a liquid oil environment [137]. The fabrication procedure involved three key steps, as shown in figure 13(a). First, an array of U-shaped trenches with designed curvature were patterned by standard EBL on the target substrate coated with viscosity mineral oil; Then, the parent substrate grown with long SiNWs was pressed to translate/slide over the pre-patterned surface to allow the long SiNWs to be trapped by the U-shaped trench and deform into the desired probe geometry, as seen in the optical microscopy and SEM images of the assembled NP arrays shown in figures 13(b), (c). In this way, SiNPs with radii of curvature from 1 to 3 μm can be obtained (figure 13(d)), with an overall yield of 86%–94%. Finally, the SiNPs were assembled and connected as bend-up arrays via an interfacial stress releasing technology, as explained in figure 14.

In comparison, the SiNPs can also be obtained via a kinking growth of SiNW during a VLS growth procedure. For example, Tian *et al* [135] demonstrated that during a VLS growth procedure, a sudden gas pressure modulation will trigger a kinking growth dynamics, leaving thus regular SiNPs. Note that, the kinking angle is determined by the crystallographic angles among different preferential growth orientations, as seen in figure 15, and thus is basically a constant of 120°, while the yield of forming such kinked SiNPs via gas pressure modulation is relatively low of ∼40%.

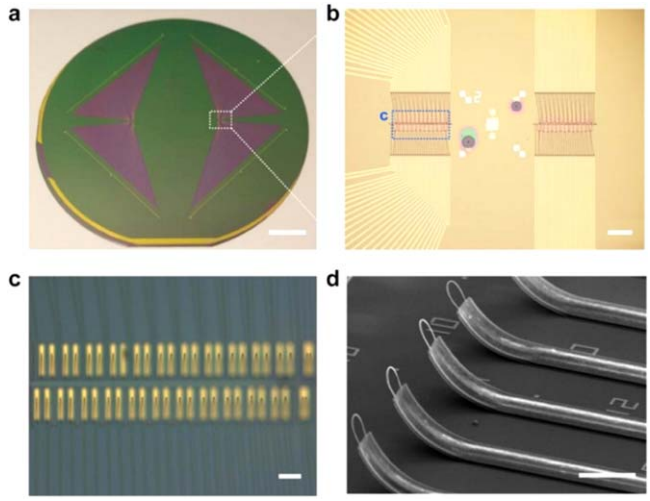


Figure 14. 3D U-shaped NW bioprobe arrays. (a) Photograph of a 3 in. wafer with deterministic 3D U-shaped NW probe arrays. (b), (c) Optical microscopy images of a representative region of 3D NW probe arrays. (d) Representative tilt-view SEM image of the tips of 3D bend-up probe array. Reprinted with permission from [137]. Copyright 2016, American Chemical Society.

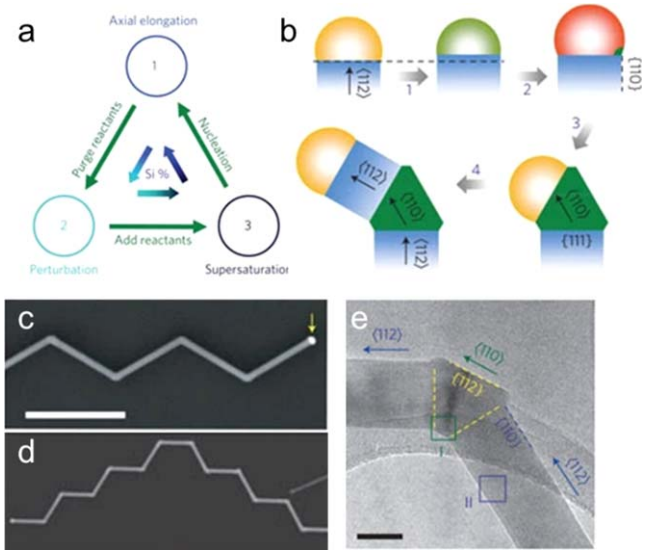


Figure 15. (a) Cycle for the introduction of a kinked NW by stepwise synthesis. (b) Arrows 1–4 denote purge, re-introduction of reactant, joint growth and subsequent arm growth, respectively. (c) SEM image of a multiply kinked two-dimensional SiNW with equal arm segment lengths. (d) SEM images of 150 nm diameter kinked SiNW grown with periodic 15 s purges. Schematic illustrating the key stages of kink formation. (e) TEM image of a single kink with crystallographic directions and facets indicated by arrows and dashed lines, respectively. Reprinted by permission from Springer Nature Customer Service Centre GmbH: Springer Nature, Nature Nanotechnology, [135], Copyright © 2009, Nature Publishing Group.

At the end, these vertically grown SiNPs need to be transferred to foreign substrate and connected selectively via EBL patterned metal electrodes, prior to being picked up and mounted upon movable platform.

In order to batch-manufacture programmable SiNPs with desired intersect angle and geometry, Liu *et al* [138] explored

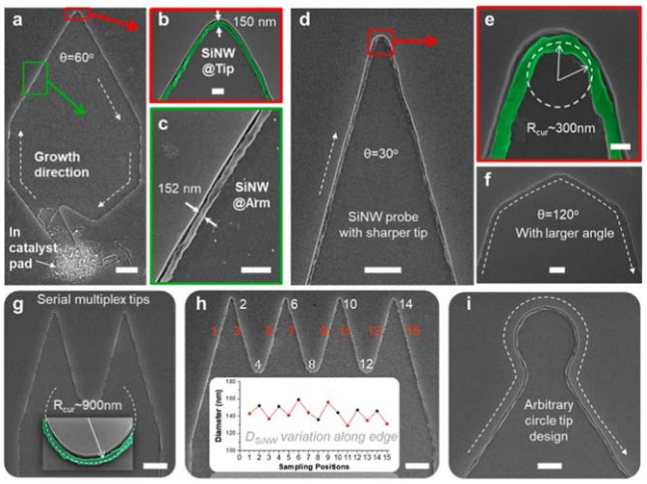


Figure 16. Growth shaping of SiNW nanoprobes via step-edge guiding strategy. (a) Guided growth of a SiNW probe with tip angle of 60° with enlarged SEM views of the bending tip and the straight arm shown in (b) and (c). (d) Sharper SiNW probe with tip angle of 30° and curvature radius of $R_{cur} \sim 300$ nm (see panel e); (f) wider probe with a tip angle of 120°. (g)–(i) Single-run growth shaping of multiplex (double in (g) and quadruple in (h)) and round in (i) probe tips. Reprinted with permission from [138]. Copyright 2021, American Chemical Society.

an edge-guided growth, that is via an IPSLS approach, to fabricate orderly array of SiNPs with designable probe shape control. Without the needs of post-growth enforced bending of SiNWs [137] or kinking growth modulation [135] as discussed above, the SiNWs can be directed by the guiding edges to grow into various tip shapes. More importantly, as witnessed in figures 16(a)–(f), the SiNP turning angles can be readily controlled to be of $\theta = 30°$, 60°, 120°, not just a constant kinking switching angle of 120°. Without the use of high precision EBL, a sharp tip with curvature radius down to 300 nm can be reliably obtained, as seen in figure 16(e), which is an important basis to ensure a minimal invasiveness of the SiNPs when they are inserted into the living cell to extract intracellular signals. In addition, more advanced parallel SiNP array were also fabricated via the single run growth of ultralong SiNWs, which represent indeed a far more complicated and potentially more functional probe structure that is difficult to fabricate via kinked VLS growth or post-growth bending, as can be seen in figures 16(g)–(i).

After being connected with Pt/Au metal electrode pads, the the as-grown SiNPs can be reliably transferred in batch from the parent substrate and mount upon movable platforms, via a procedure as depicted in figures 17(a)–(c). The free-standing NPs, as seen in figures 17(e), (f), can also sustain large enough loading force in pulling or pressing directions to penetrate/pierce the membranes of living mesenchymal steam cell (figures 17(j)–(k)). After coating SiNP with 30 nm Al_2O_3 dieletric layer, the field-effect sensing ability of the SiNPs was successfully verified in liquid droplets with different PH values, as witnessed in figure 17(i). These successful batch-fabrication and sensing demonstration of the SiNPs indicate a practical and scalable new approach to develop

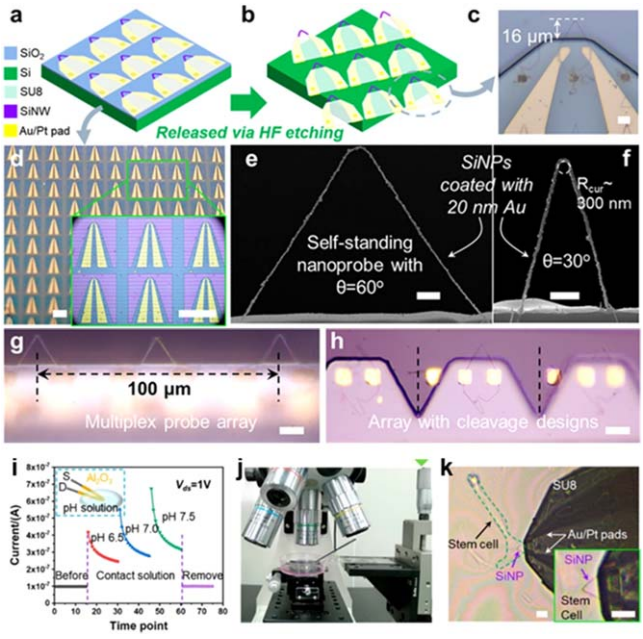


Figure 17. Scalable assembly of free-standing NPs. (a), (b) Electric connection, SU8 coating, and transferring of the orderly NP array with an optical image of the array presented in (c) and a close examination in (d). (e), (f) SEM images of the free-standing NPs with tip angles of 60° and 30°, respectively. (g)–(h) Photo images of the transferred NP array. (i) The sensor properties of the fabricated FET probe in pH solution. (j), (k) The free-standing probe was mounted on an XYZ micromanipulator and targeted to the elected stem cell. Reprinted with permission from [138]. Copyright 2021, American Chemical Society.

more advanced and sophisticated bio-probing, manipulation and sensing functionalities.

4. Conclusion and perspectives

In this Review, the recent progresses of 3D growth and integration of electronics and NEMS devices have been revisited, with a focus on the 3D nanostructures that are composed of or engineered out of 1D NWs. It has been clear that assembling 1D NWs into standing or laterally stacked FET channels can help to substantially reduce the footprint area. In parallel, more advanced helical NW structures provide ideal and unique building blocks, many of them are difficult to be fabricated via conventional lithography approach, to explore novel electronic, optoelectronic and mechanical applications. Finally, many new functionalities can be derived from the 3D geometry engineering of simple NW channels, such as the tailored nano-probes that can provide very sensitive field effect detection to cellular signals with unprecedented high spatial resolution, as well as diverse nanoscale manipulation functionalities. In addition to the conventional top-down lithography and etching approach, the addictive formation of various 3D nanostructures, via electron beam assisted or laser beam assisted depositions, provides a very promising strategy to fabricate complicated 3D architecture, while the only challenge remained is how to scale up this deterministic writing formation technology for large scale electronic device integration. A relatively new IPSLS growth mechanism could provide an interesting alternative, as the slim Si NWs can be produced on 3D sidewall surfaces with precise location and geometry controls. This thus makes it possible to design and batch-manufacture a wide range of 3D NW structures, including parallely stacked multilayer NW channels and standing helixes, as well as designable NW probes. All these new progresses combined could enable, in the near future, a more reliable and efficient 3D fabrication and scalable integration of various NW-based electronics, sensors and NEMS applications.

It can also be evnisioned that 3D architecture and electronics will prevail and flourish in the near future, as a key technology that can push forwards the Moore's law to scale further. In the mean time, Si or other semiconducting NWs, as the most advantageous channel units, will also dominate the marketplace at the N5 or N3 technology nodes, taking a vertical standing or laterally stacked configuration. The major benefits can be derived out of these structural revolutions will include, but not limited to, largely increased integration density, much better electrostatic control and greatly reduced power consumption. In addition, precise 3D stacked integration will also make it possible to conceive and fabricate a monolithic integration of more advanced near or in memory logics, enabling revolutionary neuromorphy functionalities that are difficult to implement in conventional Von Nomann architecture.

Of course, more functional 3D NW structures, such as single or double standing helices, nanoprobes and nanomanipulators, will continue to emerge, providing unprecedented platforms or testbeds to explore ultrasensitive bio detection, nanoscale manipulation and unprecedented NEMS applications. In addition to the conventional top-down etching approaches, many of these advanced technologies are supposed to rely on the unique capability of catalytic growth to produce pre-designable NW structures with tunable size, position and line-shape in 3D space, which are rather difficult, if not impossible, to be fabricated via top-down lithography and etching processes. Of course, to estabilish as a mature and reliable integration technology, there are still plenty of key aspects for the catalyst growth of NW to be further improved and verified, such as the precise position, lattice quality, doping and composition controls. Addressing all of these challenges requires thus a comprehensive and profound understanding of the key growth mechanism, dynamics and control parameters of NW channel formation and engineering processes, which need to be developped via a series of systematic and well-coordinated investigations. Nevertheless, a brighter future is ahead for the 3D fabrication and integration of NW channels for a broad range of advanced nano electronics and sensor applications

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Data availability statement

No new data were created or analysed in this study.

ORCID iDs

Linwei Yu https://orcid.org/0000-0002-0801-5210

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