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High-Performance Edge-Line Contact Memristors with In-Plane Solid–Liquid–Solid Grown Silicon Nanowires for Probabilistic Neuromorphic Computing

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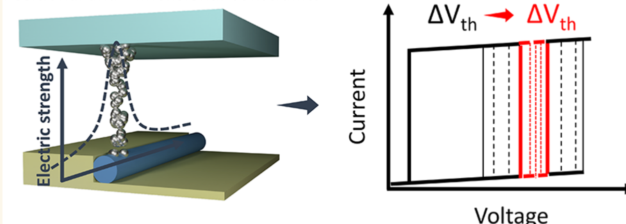
ABSTRACT: **Memristors have garnered increasing attention in neuromorphic computing hardware due to their resistive switching characteristics. However, achieving uniformity across devices and further miniaturization for large-scale arrays remain critical challenges. In this study, we demonstrate the scalable production of highly uniform, quasi-one-dimensional diffusive memristors based on heavily doped n-type silicon nanowires (SiNWs) with diameters as small as ~50 nm, fabricated via in-plane solid–liquid–solid (IPSLS) growth technology. The edge-line contact structural design improves the control of nucleation sites and the size of conductive filaments (CFs) in Ag/SiO_2/n-SiNW memristors. These devices exhibit excellent self-compliance threshold switching characteristics, including a low operating voltage (~0.8 V) with a standard deviation of 0.073 V, low leakage current (1 pA), high switching ratio (>10^7), ultrafast switching speed (~8 ns), and extremely low switching energy (47.2 fJ per operation). Additionally, we developed neurons with tunable sigmoidal probabilistic activation functions, demonstrating high uniformity across different devices. These neurons achieved an accuracy of 96.2% in binary tumor classification tasks, underscoring the potential of IPSLS-fabricated SiNWs for advanced neuromorphic computing hardware. This work highlights the effectiveness of SiNW-based memristors in addressing challenges in neuromorphic hardware design and their potential for large-scale integration.**



KEYWORDS: *silicon nanowires, in-plane solid–liquid–solid, memristor, edge-line contact, sigmoidal*

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In the era of large-scale models, the increasing demand for efficient information processing has imposed higher requirements on computing hardware, specifically for lower power consumption and faster speeds. Neuromorphic hardware systems, such as memristors, which mimic biological neural functions, are regarded as promising candidates for efficient big data processing due to their low-power consumption and inherent parallelism.[1−3] However, one major obstacle to their widespread adoption is the uncontrolled formation and rupture of conductive filaments (CFs), particularly from active ions like Ag and Cu, in the switching medium. This unpredictability leads to significant performance fluctuations and undermines the reliability of memristor devices.[4−7] As a result, this challenge has hindered the practical implementation of memristors in neuromorphic computing. To address this issue, several ion migration control strategies have been proposed for traditional thin-film memristors. These approaches include specialized electrode designs,[5,8−10] defect engineering,[11−14] interfacial barrier layers,[15,16] and constraining CF growth. While these methods have shown some success, they often suffer from limitations related to yield, reproducibility, cost-effectiveness, preservation of intrinsic material properties, and scalability for mass production. Furthermore, their effectiveness in controlling filament growth without compromising other device characteristics remains limited.

These approaches demonstrate the feasibility of improving memristor performance by confining the growth and rupture of CF at the nanoscale. Nanowires (NWs), with their inherent nanoscale dimensions, are particularly well-suited for this

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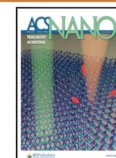

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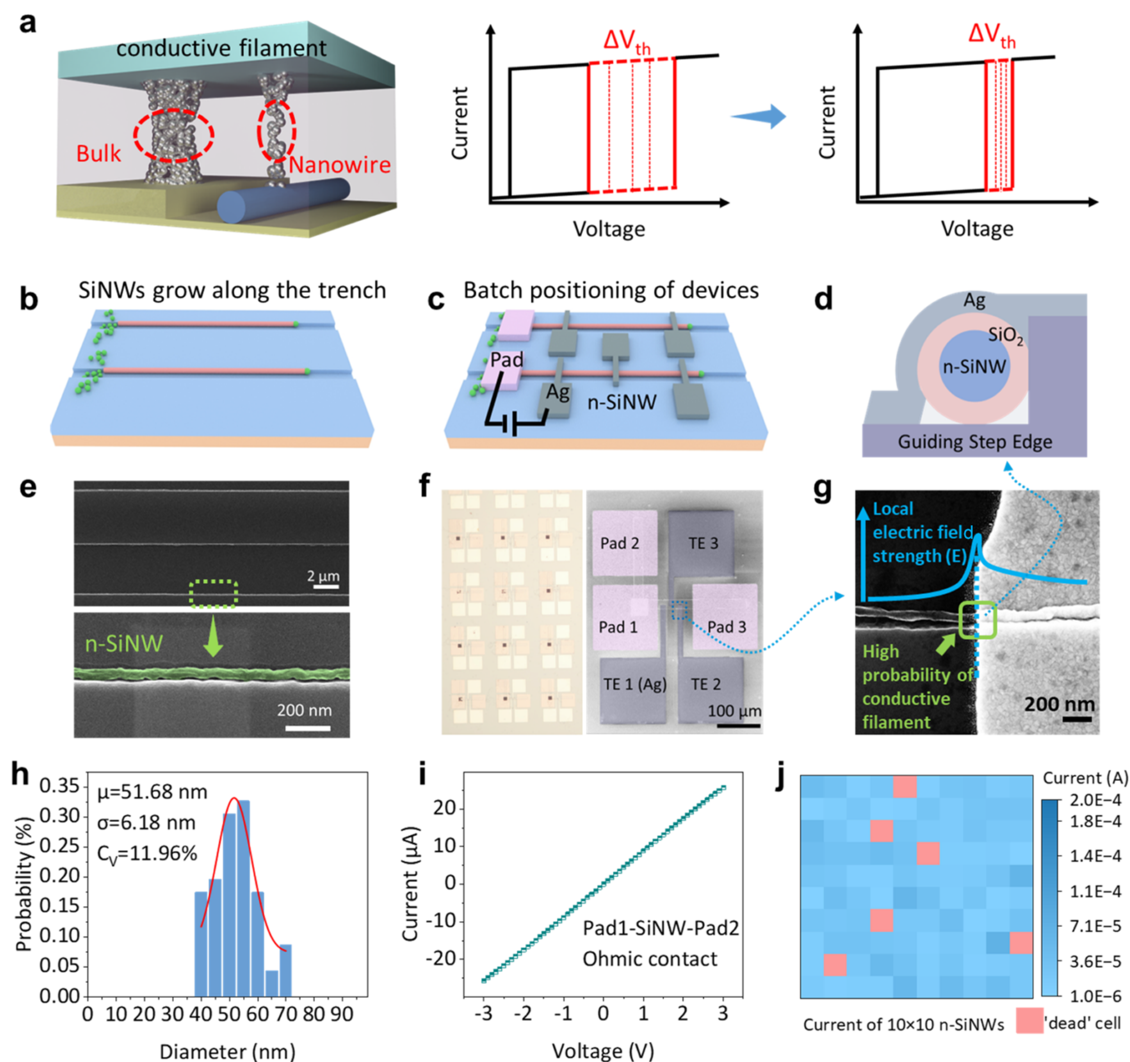

Figure 1. One-dimensional (1D) edge-line contact $Ag/SiO_2/n$-SiNW memristors fabricated in batches using the IPSLS technique. (a) Schematic illustrating the effect of NW dimension on the confinement of conductive filament (CF) growth, reducing threshold voltage fluctuations through CF control. (b) Schematic of SiNW growth positioned in batches using IPSLS technology, with SiNWs precisely aligned along the trenches. (c) Schematic of a 1D line-contact memristor based on n-SiNWs, enabling easy batch fabrication through trench alignment. (d) Cross-sectional schematic of the $Ag/SiO_2/n$-SiNW memristor, where n-SiNW serves as the electrode, the surface SiO_2 layer acts as the functional layer, and the top electrode is Ag. (e) Scanning electron microscopy (SEM) image of n-SiNWs grown along the trenches. (f) Optical microscope images of the fabricated device array (left) and SEM images of the $Ag/SiO_2/n$-SiNW memristor, featuring multiple Ag top electrodes (right). Metal pads (Ni) directly contact the n-SiNW, with the surface SiO_2 removed. (g) SEM image of the edge of the $Ag/SiO_2/n$-SiNW device, where the combination of high electric field intensity at the electrode edge and the 1D dimensions of the SiNW creates a localized quasi-zero-dimensional CF formation region. (h) Diameter distribution of n-SiNWs. (i) Ohmic contact between the n-SiNW and the pad, eliminating the interference of contact barriers with device performance. (j) Conductive current of a 10 × 10 n-SiNW cell array, where "dead cells" indicate the absence of n-SiNWs.

purpose. The nanoscale structural characteristics of NW-based memristors ensure that switching events are highly spatially localized, effectively constraining CF growth.[17−22] This precise control over CF dynamics contributes to reducing threshold voltage fluctuations in the devices, as illustrated in Figure 1a. So far, to fabricate ultrathin NW channels, there are two primary fabrication strategies: high-precision lithography and catalyst-assisted growth/formation. While high-precision lithography enables precise patterning and integration, its high cost limits scalability.[23,24] In contrast, catalyst-assisted growth/formation, such as the well-established vapor−liquid−solid (VLS) or metal-assisted chemical etching mechanism, offers a simple and cost-effective approach for producing ultrathin NWs. However, NWs are typically obtained as vertical bundles that need to be transferred and rearranged on planar substrates for memristor or other electronic device fabrication.[17,25,26] This "transfer-and-place" approach represents a formidable technological challenge for achieving reliable large-scale integration. Though numerous postgrowth assembly techniques, such as nanoscale combing,[25] surface-controlled contact printing of NWs,[27−29] magnetic field alignment,[30,31] electric field alignment,[32,33] and fluidic alignment,[34] have been explored to enhance the spatial control of the transferred NWs, achieving a deterministic positional control and precise integration of individual SiNWs on planar substrates remains highly challenging. In addition, high-precision electron beam lithography (EBL) is typically required to align and pattern electrodes upon individual NWs,[22,35,36] which is too expensive

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or inefficient for scalable and high-precision integration NW-based memristor applications.

In comparison, the in-plane solid−liquid−solid (IPSLS) SiNWs growth technique presents an effective solution by enabling the selective growth of SiNWs at predefined locations, guided by simple step edges.[37,38] This method ensures precise spatial control, seamlessly integrates with subsequent electrode fabrication, as illustrated in Figure 1b,1c, and effectively eliminates the reliance on high-precision lithography. Comparison of different technologies used to assemble catalytic NWs is shown in Table S1. By completely eliminating postgrowth transfer and assembly steps, IPSLS technique not only streamlines the manufacturing process but also facilitates large-scale, batch production, significantly reducing costs while demonstrating the capability for high integration density[39,40] and morphological control,[41−43] Furthermore, its ability to support advanced architectures, such as three-dimensional (3D) stacking, positions it as an ideal candidate for memristor logic functionality integration.[44,45]

In this work, we employed IPSLS mechanism to fabricate heavily doped n-type SiNWs (n-SiNWs) with a diameter as small as ∼50 nm, achieving a low resistivity of 1.89×10^{-3} Ω·cm. These IPSLS n-SiNWs were first used as electrodes in edge-line contact diffusion memristors, with a SiO_2 insulating layer and a silver (Ag) top electrode. The quasi-one-dimensional design, combined with edge-induced electric field enhancement, localized CF growth while maintaining control over CF position and size, resulting in improved device uniformity. The resulting devices exhibited excellent self-compliance threshold switching characteristics, including a low operating voltage of 0.8 V (standard deviation of 0.073 V), a switching ratio exceeding 10^7, a low leakage current of 1 pA, an ultrafast switching speed of ∼8 ns, and extremely low switching energy consumption of 47.2 fJ per operation. Finally, we developed passive artificial neurons based on these n-SiNW memristors, which exhibited tunable sigmoidal probability activation functions. The neurons demonstrated good uniformity and achieved an accuracy of up to 96.2% in binary tumor recognition tasks.

RESULTS AND DISCUSSION

Fabrication and Electrical Characteristics of n-SiNW Memristors. Utilizing the IPSLS method, SiNWs can be precisely positioned and grown in batches along the etched single-side edge, as illustrated in the schematic in Figure 1b and the scanning electron microscope (SEM) image of SiNWs in Figure 1e. This approach enables the direct synthesis of n-SiNWs at their designated device locations, streamlining the efficient large-scale fabrication of one-dimensional line-contact memristors, as illustrated in Figure 1c. The complete device fabrication process is detailed in Figure S1, with step-by-step procedures provided in the Methods section (Guiding Edge and Catalyst Formation; Growth of n-SiNW Arrays by IPSLS Strategy; Ag/SiO_2/n-SiNW Memristors Fabrication), and all these fabrication procedures are well-established and widely adopted in standard and industrial-scale manufacturing. The cross-sectional schematic of the Ag/SiO_2/n-SiNW memristor is depicted in Figure 1d. In this structure, the SiNW serves as the bottom electrode, Ag as the top electrode, and the SiO_2 layer (with a thickness of ∼4 nm, as shown in the cross-sectional image of the SiNW in Figure S2a) on the SiNW acts as the insulating dielectric layer, within which the Ag CF forms. Figure 1f highlights the fabricated n-SiNW memristor array (left) and a SEM image of an individual unit (right), where the pad metal directly contacts the n-SiNW to enable testing (with the SiO_2 layer removed). The top electrode (Ag) has a width of 10 μm, forming a quasi-one-dimensional line contact with the n-SiNW, and its multielectrode input configuration mimics a biological morphology. The SEM image of the critical region of the n-SiNW memristor in each unit is shown in Figure 1g, with the device region outlined by the blue dashed line corresponding to the cross-sectional schematic in Figure 1d. Notably, at the electrode edges, abrupt structural transitions lead to nonplanar surfaces, resulting in a significant increase in local electric field intensity—commonly referred to as the electrode edge effect.[46,47] The migration of Ag ions within the dielectric layer is positively correlated with the electric field strength.[5] The enhanced local electric field is expected to increase the probability of CF formation at the edges of the Ag electrode (a detailed discussion on the edge effect is provided in Figure 3e,f), thereby creating a localized quasi-zero-dimensional switching region, as illustrated in Figure 1g. Compared to the inherent uncertainties in CF growth dynamics in film devices, the edge-line structural design of the n-SiNW memristor holds potential for achieving highly uniform and reproducible switching characteristics.

The IPSLS technique facilitates the efficient large-scale growth of SiNWs extending beyond hundreds of micrometers, as evidenced by the planar SEM image of batch-fabricated SiNWs in Figure S2b. Meanwhile, the diameter fluctuations of n-SiNWs are remarkably low (the planar SEM image of a single SiNW in Figure S2c), and statistical analysis in Figure 1h indicates an average diameter of 52 nm, ensuring exceptional uniformity and reliable device performance. For the n-SiNW-based memristors designed in this work, achieving Ohmic contact between the n-SiNW and the metal pad used for electrical connection is essential, as it eliminates interference from contact barriers and other factors, thereby facilitating the accurate characterization of the intrinsic properties of the Ag/SiO_2/n-SiNW memristor. Figure 1i demonstrates the excellent Ohmic contact between n-SiNWs and Ni, with a calculated resistivity of $\rho = 1.89 \times 10^3$ Ω·cm. Similarly, good Ohmic contacts are achieved with metals like Pt/Au or Pt/Al, as shown in Figure S3. The resistance of n-SiNWs increases with temperature, exhibiting a temperature coefficient of resistance of 0.07%/K, indicative of metallic behavior and confirming that the n-SiNWs are degenerate doped as shown in Figure S4. This exceptional conductivity positions n-SiNWs as a promising candidate for use as electrodes. The conductive state of n-SiNWs was assessed in an adjacent 10 × 10 cell array (measuring the current at 1 V between Pad 1 and Pad 2 in Figure 1f), achieving a production yield of up to 94%, as shown in Figure 1j. The characterization and statistical analysis of n-SiNW yield are also consistent, which is shown in Supporting Movie S1. This high yield is critical for scaling up the production of n-SiNW-based memristors. Moreover, the IPSLS approach combines high economic efficiency with robust output, further solidifying its practicality for large-scale manufacturing.

To evaluate the performance improvements brought by the edge-line contact structured design, we compared the basic electrical characteristics of Ag/SiO_2/n-Si film memristors with Ag/SiO_2/n-SiNW memristors. The Si film electrode devices exhibited significant performance fluctuations over 100 $I-V$ scanning cycles (with a compliance current of 1 μA to avoid nonvolatile switching), as shown in Figure 2a. The statistical

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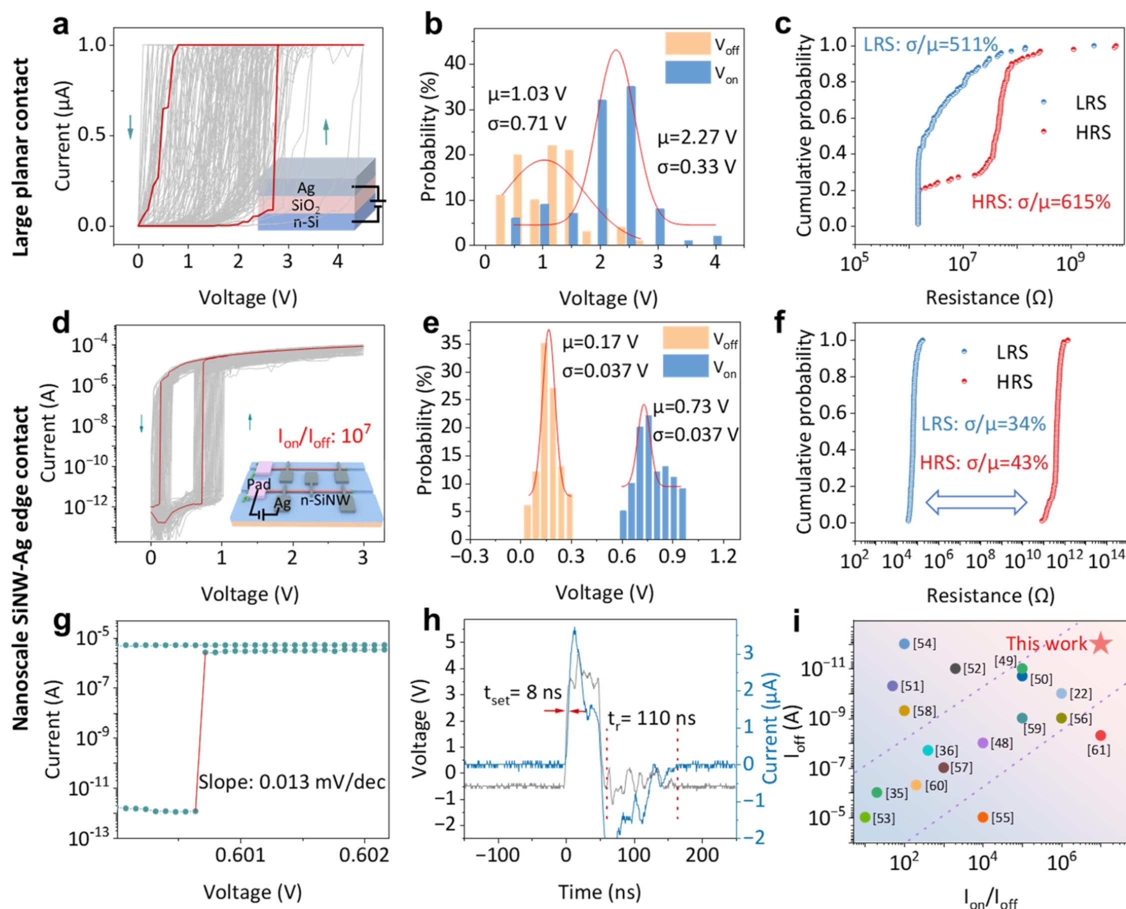

Figure 2. Performance comparison between Ag/SiO_2/n-Si film memristors and Ag/SiO_2/n-SiNW memristors. For n-Si thin-film memristors: (a) Resistive switching I−V characteristics, (b) Distribution of V_{on} and V_{off}, and (c) Cumulative probability of HRS/LRS. For n-SiNW memristors: (d) Resistive switching I−V characteristics, (e) Distribution of V_{on} and V_{off}, and (f) cumulative probability of HRS/LRS, showing significant improvement in intradevice uniformity. (g) High-resolution scan demonstrating ultrafast resistive switching with a subthreshold swing (SS) of 0.013 mV/dec (h) ultrafast switching speed of 8 ns. (i) Comparison of switching ratio and leakage current of n-SiNW memristors with other typical single NW memristors.[22,35,36,48−61]

distributions of turn-on voltage (V_{on} ranges from 0.5 to 4 V with a step interval of 0.5 V) and turn-off voltage (V_{off} ranges from 0.3 to 2.7 V with a step interval of 0.3 V) (Figure 2b), as well as the cumulative probability distribution of high resistance state (HRS) and low resistance state (LRS) (Figure 2c), showed considerable dispersion. In contrast, the Ag/SiO_2/n-SiNW memristor demonstrated significantly improved performance. As shown in Figure 2d, the device exhibited stable threshold switching characteristics (with a scanning step size of 0.02 V, and no current limitation), achieving a switching ratio as high as 10^7, a low threshold voltage of ∼0.8 V, and a leakage current as low as 1 pA. Compared to the Si film electrode device, the standard deviations (σ) of V_{on} (ranges from 0.6 to 0.95 V with a step interval of 0.05 V) and V_{off} (ranges from 0.05 to 0.3 V with a step interval of 0.05 V) for the n-SiNW electrode ones, obtained from Gaussian fitting of their statistical distributions, were reduced from 0.33 and 0.71 to 0.037 V (Figure 2e). Additionally, the variation coefficients (σ/μ) for the cumulative probability of HRS and LRS, were reduced from 615% and 511% to 43% and 34%, respectively, as shown in Figure 2f. The overall variation range of the SiNW device was significantly improved by an order of magnitude. For device integration, uniformity among different devices is essential, and the threshold voltage statistics of the n-SiNW devices are shown in Figure S5. The spatial distribution of threshold voltages for 10 × 10 different devices is shown in Figure S6, with minimal variation between devices, yielding a σ of 0.069 V, indicating excellent uniformity. The device yield closely matched the growth yield of n-SiNWs, reaching 93%.

Figure 2g highlights the ultralow turn-on slope of 0.013 mV/dec under high-resolution IV scanning for the n-SiNW device, approaching the lowest reported subthreshold swing (SS).[5] Further testing revealed an ultrafast switching speed of 8 ns under a 4 V pulse stimulus, with a single switching event consuming only 47.2 fJ. Additionally, the self-compliance behavior of the device eliminates the need for an external protective resistor during operation, effectively preventing nonvolatile transitions (Figure S7). A performance comparison with a typical single NW memristor in Figure 2i indicates that the n-SiNW device achieves a higher switching ratio and lower leakage current, which translates to a larger selection ratio and lower static power consumption.[22,35,36,48−61] Furthermore, the IPSLS mechanism employed for the fabrication of single NW memristors provides a cost-effective approach for scalable production. A detailed comparison can be found in Table S2.

Mechanism of Edge-Line Contact n-SiNW Memristors. To elucidate the role of the edge-line contact structure in enhancing the performance of SiNW devices, we first investigated the impact of electrode dimensions on CF growth. Specifically, we analyzed the conductive states of a planar Si

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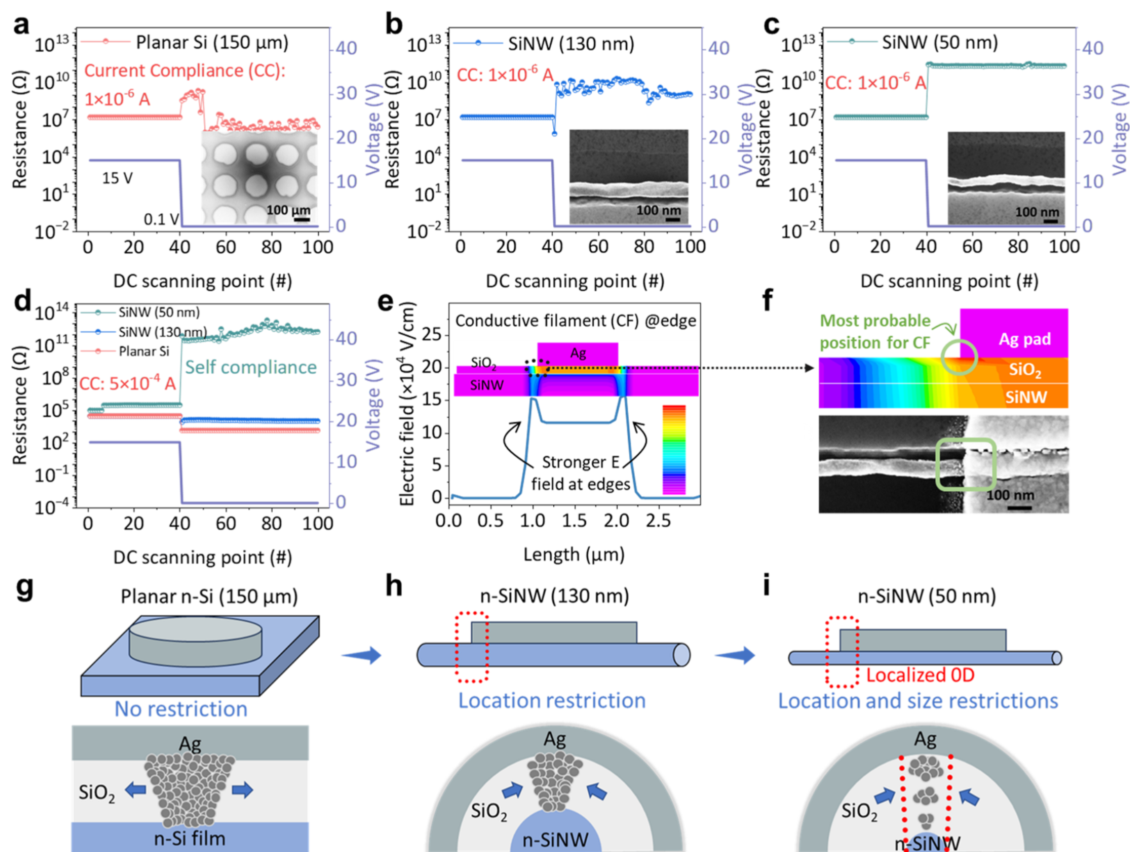

Figure 3. Switching mechanisms in Ag/SiO_2/n-SiNW memristors. Device resistance after applying 15 V high-voltage stimulation (compliance current 1 μA) (insets show SEM images reflecting device size): (a) n-Si thin-film memristor, (b) n-SiNW memristor with a diameter of 130 nm, (c) n-SiNW memristor with a diameter of 50 nm. (d) Resistance changes in the three types of devices under stimulation after increasing the compliance current to 500 μA. (e) Simulated electric field intensity distribution in the Ag/SiO_2/n-SiNW memristor. (f) Localized high electric field caused by edge effects clarifies the position of CF formation. Schematic representation of Ag CF growth under high bias in three devices: (g) Unrestricted n-Si thin-film memristor forming thick CF, (h) Partially restricted CF formation in 130 nm diameter n-SiNW, (i) More restricted CF formation in 50 nm diameter n-SiNW.

film device (150 μm in planar diameter), a SiNW device with a diameter of 130 nm, and another SiNW device with a diameter of 50 nm under external stimulation. With a compliance current of 1 μA (ensuring all devices receive the same stimulus), each device was subjected to a prolonged high voltage of 15 V, followed by resistance testing at a read voltage of 0.1 V. After stimulation, the Si film device remained in the LRS (<10^7 Ω, Figure 3a), indicating the presence of Ag CF in the SiO_2 dielectric layer. The SiNW device with a diameter of 130 nm returned to HRS (<10^{10} Ω, Figure 3b) after stimulation, while the SiNW device with a diameter of 50 nm exhibited an even higher HRS (>10^{11} Ω, Figure 3c). Although CFs in the SiO_2 dielectric layer were disrupted in both SiNW devices, the thicker SiNW's SiO_2 dielectric layer likely contained more Ag grains, leading to a lower off-state resistance. To further verify this, the compliance current was increased to 500 μA. As shown in Figure 3d, after stimulation, the Si thin-film device displayed a lower LRS than the SiNW device with a diameter of 130 nm, suggesting that the CFs in the thin-film device were thicker due to the lack of size constraints. The SiNW device with a diameter of 50 nm exhibited saturation under the 15 V high voltage (with the inherent resistance of the SiNW acting as a self-compliance mechanism), remaining in HRS (>10^{11} Ω) after stimulation. The thickness of the CFs is positively correlated with the size of the electrodes. Due to atomic surface diffusion driven by system energy minimization, thinner metallic CFs are more prone to spontaneous rupture, subsequently existing in the form of nanoclusters.[62−64] The smaller dimensions of the SiNW more effectively limit CF formation, allowing the device to rapidly revert to HRS once the bias voltage is removed. This behavior is further demonstrated in the cyclic switching of SiNW devices under scanning (with a 3 V bias voltage and a 0.05 V read voltage). During this process, the HRS of the SiNW device with a diameter of 130 nm fluctuated significantly (Figure S8a), indicating greater randomness in the size of Ag clusters left behind after the formation and breakup of thicker CFs. These Ag clusters within the SiO_2 dielectric layer contributed to the variability in the device's HRS resistance. In contrast, the SiNW device with a diameter of 50 nm exhibited consistent HRS throughout each switching cycle (Figure S8b), as the thinner CFs break more thoroughly, which also explains the device's ultralow leakage current.

In addition to the confinement effect attributed to the SiNW diameter, we further evaluated the potential growth locations of the CFs. Electrode edge effects typically refer to the phenomena occurring in field-effect transistors (FETs), where the sharp structural features at the electrode edges induce a localized and stronger electric field distribution along the edge line.[46,47] In SiNW-based memristors fabricated here, these edge effects have some beneficial impacts. As shown in Figure 3e, the simulation of the electric field distribution across the

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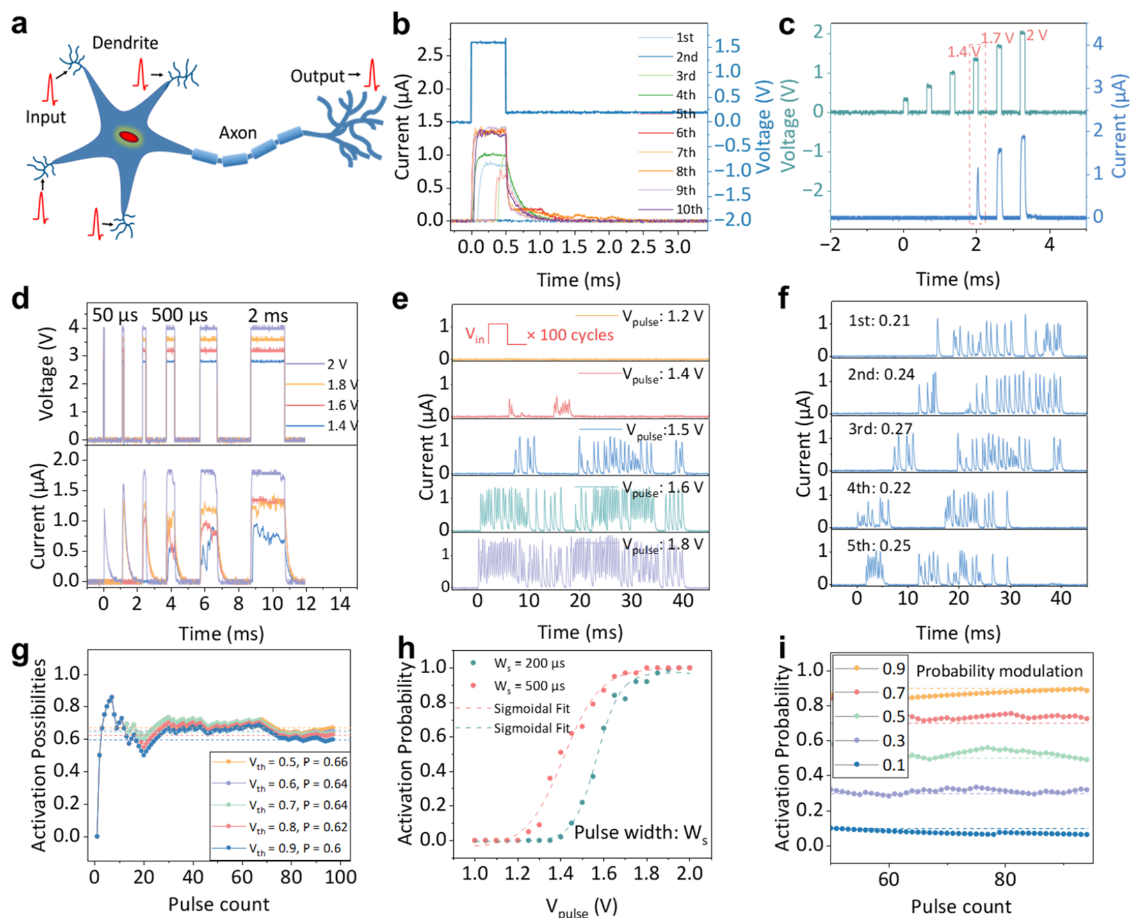

Figure 4. Artificial neurons with sigmoidal probabilistic activation functions implemented using Ag/SiO_2/n-SiNW memristors. (a) Schematic of a biological neuron, which transmit information via neural spikes (b) randomness in spike timing, where the exact spike emission time may vary under the same stimulation conditions. (c) Threshold-driven spiking behavior. (d) Spike response as a function of both stimulus intensity and duration. (e) Frequency modulation of the spiking response under continuous pulse stimulation. (f) Uniformity of the spike response under identical stimulation. (g) Convergence of neuronal spike activation probability with the number of pulses. (h) Activation probability of neurons at different pulse widths W_s (500, 200 μs) under the condition of pulse spacing W_i of 500 μs as a function of pulse amplitude V_{pulse}, and the sigmoidal function fit. (i) Activation probability modulation implemented by the fitted function to achieve convergence of the actual activation probability of a neuron to the expected probability.

SiNW when a voltage is applied to the Ag electrode reveals that the field strength near the electrode edges is higher than in the central region. Due to electric field concentration caused by curvature, Ag ions are more likely to migrate in these high-field regions. As illustrated in Figure 3f, the SiNWs and the electrode edges form localized quasi-0D switching regions, where there is a higher probability of CF formation. Additionally, the high curvature of the SiNWs themselves further enhances the local electric field strength, contributing to the fast-switching speed of the device, reaching as quick as 8 ns (Figure 2h). The switching speed of Ag-based memristors primarily depends on the migration speed of Ag ions, which is controlled by the applied electric field.[5]

Figure 3g,i schematically depict the CF growth in three different types of devices under strong bias. In thin-film devices (Figure 3g), CF growth is unrestricted in both space and size, allowing CF to nucleate anywhere and excessively grow into thick filaments, which may be beneficial for memory applications but can reduce device reliability. In SiNW device with a diameter of 130 nm (Figure 3h), the CF growth space is constrained from two-dimensional to quasi-one-dimensional. However, for nanoscale CF, this size restriction is insufficient, still leading to resistance fluctuations in the device. In contrast, for SiNW devices with a diameter of 50 nm, the CF growth is not only spatially confined (quasi-0D, as shown in Figure 3i), but the diameter of the SiNW only allows for the formation of thin CF. This, combined with the intrinsic resistance of the SiNW, endows the device with self-compliance, resulting in excellent uniformity. As a result, SiNW devices with smaller diameters exhibit continuous and stable threshold switching behavior under pulsed operation, with endurance exceeding 10^6 cycles, as shown in Figure S9.

Implementation of Sigmoidal Artificial Neurons Based on n-SiNW Memristors for Tumor Diagnosis. Biological neurons transmit information through neural spikes (Figure 4a), characterized by key features such as spike timing randomness, threshold-driven behavior, and frequency response, which collectively support the functional efficiency of complex neural systems.[65,66] Memristors with threshold switching characteristics, which eliminate the need for additional reset operations, demonstrate advantages in mimicking neuronal spiking behavior.[65,67−69] Here, we constructed artificial neurons using n-SiNW threshold-switching memristors without the assistance of additional circuit

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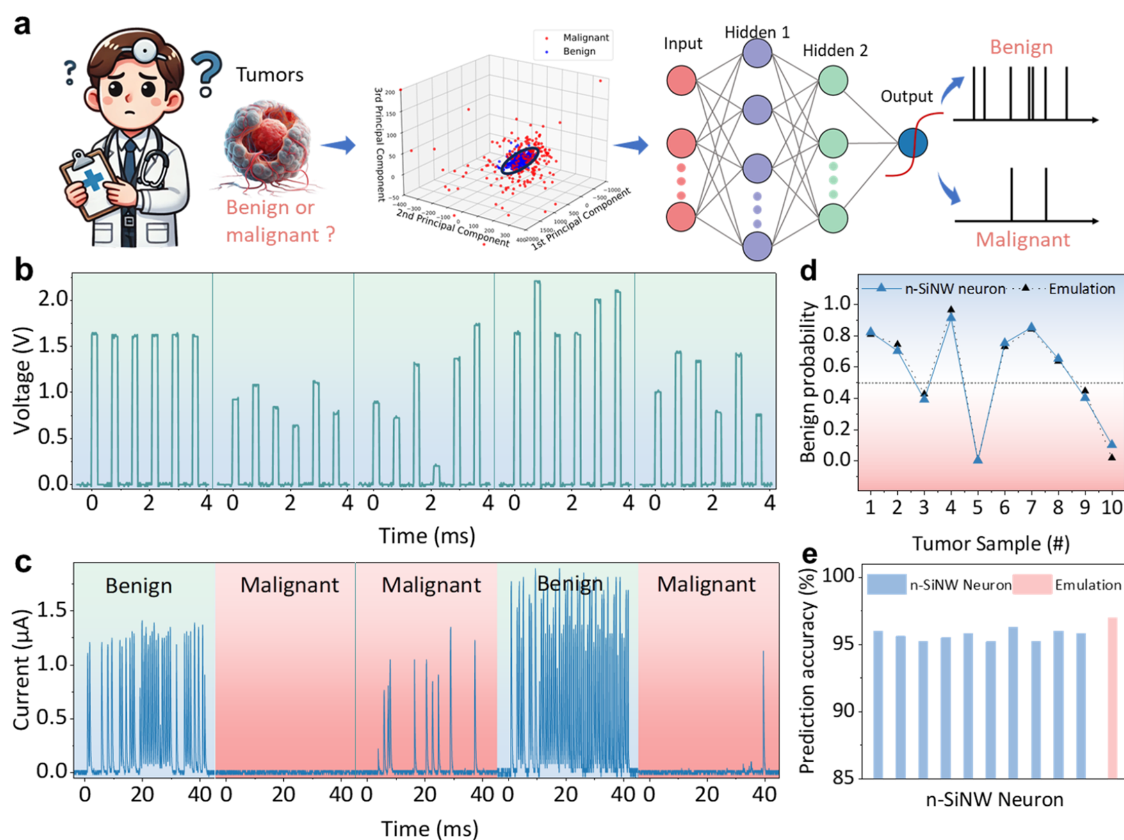

Figure 5. Binary tumor diagnosis based on n-SiNW neurons. (a) Schematic of tumor diagnosis using n-SiNW neurons with sigmoidal functions, including pretraining visualization of tumor features and a diagram of the SNN network (input layer, two hidden layers, and a sigmoidal output layer). (b) Features of five randomly selected tumor samples from hidden layer 2 after training, presented in the form of pulses. (c) Spike responses of n-SiNW neurons corresponding to the five tumor samples; high spike probability corresponds to benign tumors (blue background), while low spike probability corresponds to malignant tumors (red background). (d) Comparison of benign tumor probability predictions between simulations and n-SiNW neurons. (e) Prediction accuracy of different n-SiNW neurons.

components. Randomness enhances the flexibility and adaptability of the nervous system, enabling it to process complex environmental information. Under identical stimulation conditions, the exact spike timing can vary, a phenomenon known as "spike timing jitter". Figure 4b shows the device's random time response under a 1.6 V pulse stimulus. In biological neurons, the uncertainty in spike timing decreases under strong stimuli, and n-SiNW neurons exhibit the same trait (Figure S10). The threshold refers to the specific voltage that the membrane potential must reach to trigger a neuronal spike. The presence of this threshold allows neurons to filter out weak or irrelevant signals, thereby ensuring efficient information transmission. Figure 4c illustrates the device's threshold-driven response, where a spike is only generated when the pulse amplitude reaches 1.4 V under the same stimulation duration. Under prolonged stimulation, the membrane potential may gradually accumulate toward the threshold, increasing the probability of spike generation. A higher pulse amplitude accelerates this accumulation process, thereby reducing the time required to elicit a spike response, as shown in Figure 4d. Specifically, under a 2 V pulse stimulus, a 50 μs pulse is sufficient to induce a spike response, whereas under a 1.4 V pulse stimulus, a significantly longer duration of 500 μs is required to generate a spike.

Frequency modulation by stimulus intensity is crucial in the nervous system, as it allows neurons to convey different information intensities through varying firing frequencies. Figure 4e demonstrates the device's frequency response under continuous pulse stimuli (period T = 400 μs, pulse width W_s = 200 μs), where the spike response frequency increases with higher pulse amplitudes. A complete view of spike responses at different amplitudes is provided in Figure S11. Furthermore, at specific stimulus amplitudes, the spike response probability remains relatively stable, as shown in Figure 4f. In contrast, in diffusive memristors without structural optimization, identical stimuli often result in highly variable probabilistic spike behavior.[70,71] While this randomness is beneficial for true random number generation, it compromises the critical neuronal function of frequency-modulated response. Among representative approaches, artificial neurons are constructed by combining input resistors, capacitors, and diffusive memristors to delay spike generation (giving CF more relaxation time, ensuring complete CF rupture) and achieve frequency response (Figure S12).[65,67−69] Benefiting from the structured design of n-SiNW memristors, CF formation and rupture occur more rapidly, ensuring uniform spike frequency response, which is crucial for the practical construction of neural networks. The n-SiNW memristor can achieve key neuronal functions with just a single device, demonstrating great potential for hardware-based spiking neural networks.

To evaluate the applicability of n-SiNW artificial neurons in probabilistic computing, we quantitatively assessed the spike activation probability. Activation probability is defined as the

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likelihood of a neuron emitting a spike in response to the current stimulation pulse (i.e., the ratio of the number of spikes to the number of pulses). Figure S13 shows the neuron's spiking response under continuous 1.5 V pulse stimulation (period T = 1 ms, pulse width W_s = 500 μs). As the pulse stimulation continues, the spike activation probability gradually converges to a stable value, demonstrating a behavior similar to the adaptation of biological neurons to stimuli (Figure 4g). Convergence of the spike activation probability was observed under pulse stimulations ranging from 1.1 to 2 V (Figure S14), with the probability increasing as the pulse amplitude increased. The overall activation probability closely fits a sigmoidal curve (Figure 4h). Additionally, Figure 4h illustrates the effect of pulse width W_s on activation probability, showing that reducing the single-pulse stimulation duration (while maintaining a constant pulse interval W_i = 200 μs) shifts the sigmoidal curve to the right. This demonstrates the ability to regulate the neuronal probability sigmoid function through electrical parameters. In contrast, the pulse interval W_i has a much smaller effect on activation probability, as shown in Figure S15a. As discussed in Figure 3, the structural confinement of CF in n-SiNW memristors leads to easier CF rupture after the formation of thin CFs. With pulse intervals W_i (200 and 500 μs) larger than the CF rupture relaxation time under the same intensity of pulse width W_s (200 μs), the activation probability remains unaffected. Owing to the exceptional uniformity of n-SiNW memristors, the probabilistic sigmoidal functions of different devices are nearly identical (Figure S15b), which may help reduce computational errors in neural networks caused by variations in node parameters.

The sigmoidal function is widely used across various fields, particularly in scenarios involving probabilistic outputs, nonlinear mapping, and binary classification tasks.[69,72,73] The n-SiNW neuron exhibits a probability response that closely matches the sigmoidal function. The sigmoidal function is expressed by the following equation:

$$y = \frac{a}{1 + e^{-b(x-c)}}$$

where x is the pulse amplitude, and a, b, and c are fitting parameters. The sigmoidal functions under different W_s and W_i conditions are listed in Table S3, and the ones for different devices are shown in Table S4. For the condition with W_s = 200 μs and W_i = 500 μs, the fitting parameters obtained from the probability response are a = 0.98, b = 18.22, and c = 1.57. Based on this function, we inversely verified the spike activation probability control. The expected voltages required to achieve activation probabilities from 0.1 to 0.9 were calculated as 1.45, 1.5, 1.525, 1.55, 1.57, 1.595, 1.62, 1.65, and 1.7 V, respectively. The neuron activation probability under specific voltage pulses is shown in Figure 4i, where the response probability converged closely to the expected values (complete probability verification can be found in Figure S16). The normalized mean square error (NMSE) between the expected and actual probabilities significantly decreases with the increasing number of pulses (Figure S17). This probability control capability has been applied to Bayesian networks,[74,75] such as probabilistic Bayesian inference in gene regulatory networks.[72]

Figure 5 demonstrates the potential of n-SiNW neurons equipped with sigmoidal functions for binary classification tasks. Taking tumor diagnosis as an example (Figure 5a), real-life clinical data are often difficult to strictly categorize as benign or malignant. Principal component analysis visualization of tumor features shows that benign and malignant tumors partially overlap (highlighted in black), leading to diagnostic challenges. The spike neural network (SNN) based on probabilistic neurons performed well in addressing this uncertainty quantification issue.[69] Here, we constructed a probabilistic SNN using 300 sets of tumor data for training, with the remaining 269 sets used as the test set. The hidden layer 2 converts the trained data into six-dimensional features, and the sigmoidal neurons execute the binary classification task, where the output probability of benign tumors corresponds to the spike probability of the neurons. We utilized the sigmoidal probabilistic response of the n-SiNW neurons at the hardware level to perform prediction tasks.

Figure 5b shows the pulse input for five randomly selected tumor samples, with the data from hidden layer 2 mapped to the working range of the n-SiNW neurons. Each cycle consists of six pulses, and for improved prediction accuracy, each tumor sample received 10 cycles, resulting in a total of 60 pulses. The tumor prediction results are shown in Figure 5c: samples 1 and 4 (blue background) displayed significant neuron spike responses, indicating a high probability that these samples are benign. In contrast, samples 2, 3, and 5 had no or weak spike responses, and were thus classified as malignant. These predictions matched the actual outcomes perfectly. We compared tumor prediction results between simulations and n-SiNW neurons, and the prediction probabilities from n-SiNW neurons closely aligned with the theoretical expectations of the simulations, as shown in Figure 5d. In traditional hardware, implementing the sigmoidal function requires multiple transistors,[76,77] whereas the n-SiNW neuron achieves the same functionality with just a single device, significantly reducing hardware area overhead. Figure 5e further considers the effect of device variability on prediction accuracy, showing that all 10 different n-SiNW neurons achieved over 95% accuracy, with a maximum of 96.2%, approaching the 97.4% accuracy achieved by the software-based SNN. The high consistency of probabilistic responses across different neurons presents promising potential for their application in large-scale neural networks.

CONCLUSIONS

This study demonstrates the fabrication of highly uniform, quasi-one-dimensional memristors using n-SiNWs grown via IPSLS technique. The edge-line contact design enabled precise control over conductive filament formation, achieving excellent self-compliance threshold switching characteristics, including low operating voltage, high switching ratio, ultrafast speed, and low energy consumption. These memristors were further utilized to develop artificial neurons with tunable sigmoidal activation functions, achieving 96.2% accuracy in binary tumor classification tasks. The IPSLS method offers a scalable, cost-effective solution to challenges in neuromorphic hardware, contributing to the development of energy-efficient, large-scale systems.

METHODS

Guiding Edge and Catalyst Formation. Silicon wafers with a 500 nm SiO_2 surface were first cleaned with acetone, alcohol and deionized water. Straight guiding edges were prepared on the SiO_2 surface using standard photolithography and Inductively Couple Plasma etching procedures with the etching gas C_4F_8. The etching depth of the guiding edge lines was approximately 100 nm. Indium

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(In) stripes with a thickness of 8 nm were then patterned and deposited by photolithography, thermal evaporation, and standard stripping procedures.

Growth of n-SiNW Arrays by IPSLS Strategy. The samples were loaded into a PECVD system and then treated with hydrogen plasma at 250 °C for 15 min to remove the native Indium oxide layer, with a hydrogen flow rate of 35 SCCM, a pressure of 130 Pa, and a RF power of 10 W. The precursor layer of phosphorus-doped amorphous silicon (a-Si) thin films was deposited on the surface of the samples under the conditions of a gas flow rate of 6 SCCM for SiH_4, a gas flow rate of 1.5 SCCM for a mix of 5% PH_3 + 95% H_2, a pressure of 40 Pa, and a RF power of 0 W. A phosphorus-doped a-Si thin film precursor layer was then deposited on the sample surface at 100 °C with a pressure of 40 Pa and an RF power of 0 W. In the next step, the substrate temperature was increased to 350 °C and held in vacuum for 60 min. Molten In droplets move along the guiding edges and absorb the a-Si layer, producing crystalline n-SiNW behind it. Finally, the residual a-Si layer is selectively etched away using CF_4 gas.

Ag/SiO_2/n-SiNW Memristors Fabrication. The samples were placed in a hot annealing furnace with oxygen passed through and oxidized for 5 min at 450 °C. The SiO_2 dielectric layer formed on the surface of n-SiNW. The n-SiNW was used as the bottom electrode, and the photolithography defined the test Pad region, where metal was deposited after removing the SiO_2 by hydrofluoric acid and the lift-off procedure was performed. The metal Pad formed an ohmic contact with the n-SiNW for the test connection. Then photolithography defines the top electrode region, vaporizes Ag and prepares the top electrode using lift-off procedure to prepare a memristor with a structure of Ag/SiO_2/n-SiNW.

Electrical Measurements. Fabricated Ag/SiO_2/n-SiNW memristors were measured under atmospheric conditions. DC current−voltage characteristics were measured using a Keithley 2636B source meter. Impulse response was measured using a waveform generator (Keysight, 33600A) and oscilloscope (Keysight, DSOX3052A).

Emulation. *Edge Effect.* We utilized the Silvaco-TCAD simulator to model the physical behavior of the n-SiNW memristor. The electric field distribution was extracted from the simulation-generated structure files.

SNN. The tumor data is sourced from the Wisconsin Breast Cancer Database. The SNN architecture is implemented using Python. This multilayer Spiking Neural Network (SNN) model processes input features through hidden neurons, calculating membrane potentials (threshold potentials) and employing a sigmoid function to determine spike generation. The firing probabilities of the output neurons represent class predictions, and synaptic weights are updated based on errors during the training process. Further details can be found in Supporting Information Note S1.

ASSOCIATED CONTENT

Data Availability Statement

The data in this work is available from the authors upon reasonable request.

Supporting Information

The Supporting Information is available free of charge at https://pubs.acs.org/doi/10.1021/acsnano.4c16583.

Schematic illustration of device fabrication (Figure S1); characterization and electrical properties of n-SiNWs (Figures S2−S4); statistical analysis of n-SiNW memristor uniformity (Figures S5 and S6), self-compliance behavior (Figures S7 and S8), and endurance (Figure S9); neuronal spike responses of SiNW memristors (Figures S10−S17); comparison of nanowire alignment strategies (Table S1); comparison of single-nanowire memristors (Table S2); sigmoidal fitting parameters of SiNW neuronal devices (Tables S3 and S4); mathematical formulation of multilayer SNNs (Note 1) (PDF)

Demonstration of high-guided growth yield of SiNWs (Movie S1) (MP4)

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Author Contributions

L.Y. carried out the experiments, analyzed the data, and wrote the manuscript. Y.Z. participated in the neural network simulations. Z.H. contributed to the electric field simulations. Z.L., J.W., and L.Y. oversaw all phases of the research and revised the manuscript. All authors participated in the writing and revision of the manuscript.

Notes

The authors declare no competing financial interest.

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