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Heteroepitaxial Writing of Silicon-on-Sapphire Nanowires

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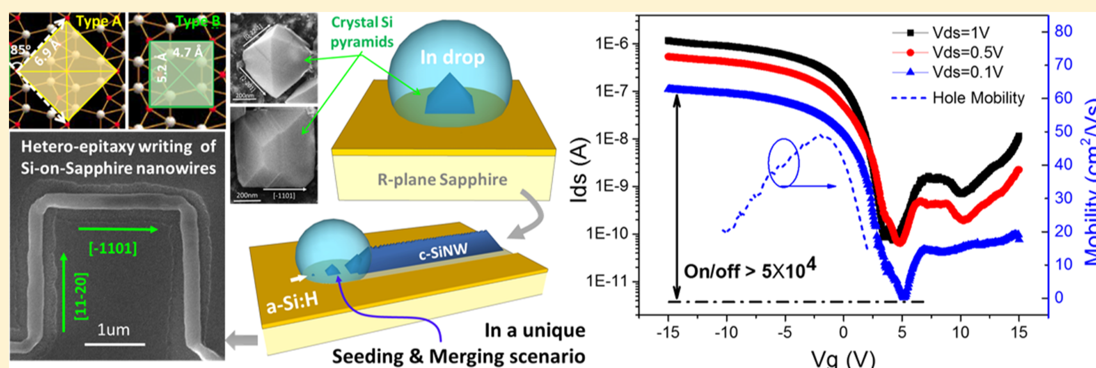

ABSTRACT: The heteroepitaxial growth of crystal silicon thin films on sapphire, usually referred to as SoS, has been a key technology for high-speed mixed-signal integrated circuits and processors. Here, we report a novel nanoscale SoS heteroepitaxial growth that resembles the in-plane writing of self-aligned silicon nanowires (SiNWs) on R-plane sapphire. During a low-temperature growth at <350 °C, compared to that required for conventional SoS fabrication at >900 °C, the bottom heterointerface cultivates crystalline Si pyramid seeds within the catalyst droplet, while the vertical SiNW/catalyst interface subsequently threads the seeds into continuous nanowires, producing self-oriented in-plane SiNWs that follow a set of crystallographic directions of the sapphire substrate. Despite the low-temperature fabrication process, the field effect transistors built on the SoS-SiNWs demonstrate a high on/off ratio of $>5 \times 10^4$ and a peak hole mobility of >50 cm^2/V·s. These results indicate the novel potential of deploying in-plane SoS nanowire channels in places that require high-performance nanoelectronics and optoelectronics with a drastically reduced thermal budget and a simplified manufacturing procedure.

KEYWORDS: *In-plane Si nanowires, silicon on sapphire, heteroepitaxy, self-alignment*

The heteroepitaxial growth of thin film crystals over foreign substrates has been the key enabling technology for high-performance space and mobile electronics.[1,2] Because of a similar atomic arrangement of the surface oxygen sites on R-plane $(1\bar{1}02)$ sapphire (SP) to those of the Si atoms on the Si(100) plane, it is possible to achieve heteroepitaxial growth of a crystalline silicon (Si) thin layer over the insulating Al_2O_3 substrate, which has been referred to as the silicon-on-sapphire (SoS) structure.[1,3] As a special type of silicon-on-insulator (SOI) technology, the SoS configuration can shed off a large portion of parasitic capacitance to achieve a faster transistor operation with an even lower power consumption and a higher integration density[1,3−5] because all the reverse-biased isolation zones required in bulk c-Si CMOS can be removed. In parallel, SoS nanowire waveguides, carved out of planar SoS thin films, are widely used for mid-infrared photonics and sensor applications, where a wider transparent window beyond 3.5 μm is preferred.[2,6−9]

However, conventional SoS fabrication via chemical vapor deposition (CVD) requires a relatively high temperature >900 °C.[2] During the final cooling step, a high density of defects, on the order of $>10^9$ line-defects/cm^2, are generated in the epitaxially grown c-Si layer[1,2] because the thermal expansion coefficient of sapphire of $\sim$7.3−8.1 $\times 10^{-6}$/°C is two times larger than that of c-Si (3.6×10^{-6}/°C).[10] Therefore, a low-temperature heteroepitaxial growth process is desirable. On the other hand, the lattice spacing along the $(1\bar{1}02)$ and $(11\bar{2}0)$ orientations in the R-plane sapphire substrate are 4.75 and 5.20 Å, respectively, which are 12.5% and 4.2% smaller than the lattice spacing of 5.43 Å on the Si(100) plane; this makes it difficult to achieve a high quality heteroepitaxial thin film over a large extent. In particular, in most SoS-based field effect

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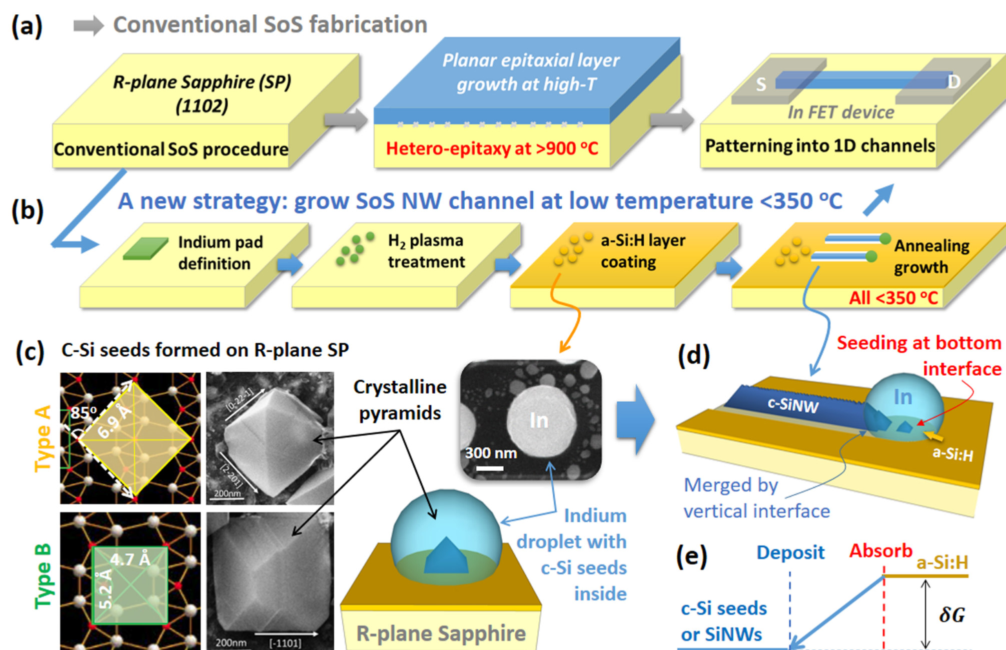

Figure 1. Heteroepitaxial growth of in-plane SoS nanowires (NWs). (a) Schematic illustration of the conventional heteroepitaxial growth process and the patterning of a planar silicon-on-sapphire (SoS) thin film structure; (b) schematic illustration of a more straightforward in-plane SoS growth of Si nanowire channels in a single-run and through low-temperature fabrication on a sapphire substrate; (c) the lattice alignment and SEM images of the formation of crystal Si pyramid seeds on an R-plane sapphire substrate within In droplets with two distinct orientations of Type A and B; (d) the in-plane growth of SiNWs led by a moving droplet that absorbs a-Si/H in front and produces c-SiNW behind, where the preferential formation of new nuclei occurs at the bottom heteroepitaxial interface with a diagram showing the difference in Gibbs energy between a-Si/H and c-Si in (e), which is the driving force for the progression of the in-plane growth.

transistors (FET) or waveguide applications,[1−3,6−9] the quasi-1D channel structures carved out of the planar SoS epitaxial thin layer via lithography and etching (as depicted in Figure 1a) serve as the functional units. A radically different thought process or strategy involves the growth of self-oriented in-plane SiNWs directly into the required places, which would ideally be conducted in a single-run and through low-temperature manufacturing, as illustrated schematically by the lower panel series in Figure 1b. Therefore, the nanoscale locomotion of liquid metal droplets, for example, indium (In) with a low melting point of 156.6 °C, can help to mediate the in-plane growth of SiNWs directly on the R-plane substrates. This is advantageous for device applications, as it precludes the need for high temperature in planar SoS heteroepitaxial growth as well as the need for subsequent lithography and etching steps. Recently, the discovery of the metal-droplet-mediated hetero-epitaxial growth of self-aligned GaN or ZnO nanowires upon sapphire substrates[11,12] in a vapor−liquid−solid (VLS) mode[13,14] has highlighted the potential of nanoscale self-assembly in manufacturing crucial building blocks for nano-electronics.[12] However, the heteroepitaxial growth of SoS nanowires, via a fundamentally different in-plane growth mechanism,[15−18] has not been explored or demonstrated to date, despite its important potential for future SoS-based electronic and optoelectronic device applications.

In this Letter, we propose and demonstrate for the first time a heteroepitaxial growth of SoS SiNWs with the aid of nanoscale surface-rolling indium (In) catalyst droplets that proceeds by following the crystallographic guidance of the underlying R-plane sapphire substrate. This can be viewed as a running version of liquid-phase droplet epitaxial growth,[19−22] which occurs via a unique seeding-and-merging scenario within a catalyst droplet oversaturated with Si atoms, as schematically depicted in Figure 1c,d. Therefore, the epitaxial growth of SoS nanowires can be initiated at a relatively low temperature of 350 °C. Interestingly, we found that the heteroepitaxial interface has a deterministic influence not only on the alignment of SiNWs but also on their morphology and line-shape. In addition, we propose a new collective-and-competitive interface nucleation model to address and explain the heteroepitaxial growth dynamics and the observed criteria for SoS growth. In contrast to previous homoepitaxial growth of in-plane SiNWs on semiconducting Si(100) substrates,[16] the heteroepitaxial growth of SoS nanochannels enables the direct fabrication of high-performance FET devices, as demonstrated later, and thus it lays the foundation for future nano-SoS device applications.

The heteroepitaxial growth of in-plane SiNWs was carried out on R-plane sapphire substrates, which were first cleaned by ultrasonication in deionized water. First, as schematically illustrated in Figure 1b, a 10 μm wide array of In pads was patterned through evaporation and lift-off procedures, prior to its loading into a plasma-enhanced chemical vapor deposition (PECVD) system. Then, a hydrogen (H_2) plasma treatment was applied at 300 °C to reduce the oxide shell of the In layer and transform the In layers into discrete droplets. In the next step, the substrate temperature was decreased to 180 °C, and a thin layer of hydrogenated amorphous silicon (a-Si:H) of approximately 40−60 nm was deposited from pure silane plasma. A close scanning electron microscopy (SEM) view of the discrete In droplets is presented in the top-right inset of Figure 1c. Finally, without breaking the vacuum the samples were annealed at 350 °C in a H_2 ambient for 1 h to activate the in-plane growth of SiNWs. At the end, the remnant a-Si:H layer around the in-plane SiNWs can be selectively removed by H_2 plasma at 100 °C.[15,16,23,24]

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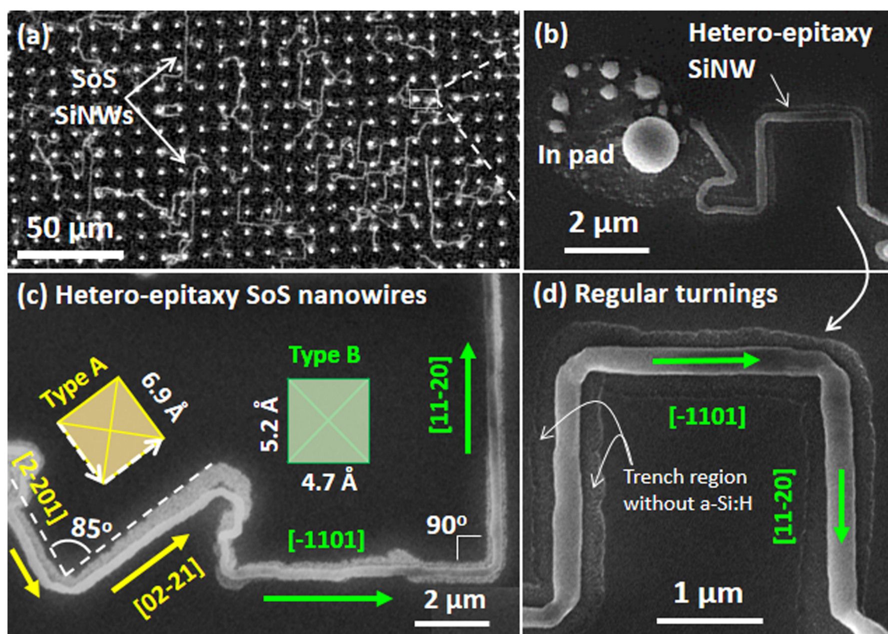

Figure 2. Heteroepitaxial growth of in-plane SoS nanowires. (a−d) The SEM images of the heteroepitaxial SiNWs grown on a R-plane sapphire substrate. Schematic illustrations of the two possible alignments of the Si seed pyramids, in Type A or B orientations, are plotted in (c).

SEM images of the in-plane heteroepitaxial SoS SiNWs are shown in Figure 2, where the epitaxial SoS nanowires are identified as the long and straight white lines lying among an array of indium pads in Figure 2a. The in-plane SiNWs first grew out of the indium pads and then followed the growth orientations to form regular straight SiNW segments, as indicated in Figure 2b,c. When the remnant a-Si:H is preserved, a wider trench region can be observed around the SiNWs, as shown and marked in Figure 2d, which is left by the passing catalyst droplet and thus serves as an accurate record of the moving path and width of the catalyst droplets.

As a matter of fact, the driving force of this in-plane growth is the higher Gibbs energy of the Si atoms observed in an amorphous state compared to that in crystalline Si, as illustrated in Figure 1e, which is $\delta G = G_{aSi} - G_{cSi} = 0.12{-}0.15$ eV.[25,26] During the annealing growth step, the a-Si:H layer coated upon the In droplets will first be absorbed by the droplet to establish a supersaturated state of Si atoms (see Figure 1b), which then leads to the nucleation and formation of crystalline Si seeds[27,28] within the In droplet that rest on the R-plane sapphire surface. For example, the SEM images of the typical pyramid seeds found on the R-plane sapphire substrate are presented in Figure 1c. As the R-plane substrate has a similar atomic arrangement to that of Si(100), the c-Si seeds formed with a coherent epitaxial interface to the underlying sapphire lattice thus develop into regular pyramid shapes bounded by Si(111) planes, as is usually found in the homoepitaxy of Si on Si(100) substrates.[16] However, on the R-plane sapphire (SP) substrate, we identify two types of pyramid seeds, according to their different baseline alignments, as indicated in Figure 1c: these are the Type A or Type B seeding arrangements with pyramid baselines aligned with the SP[$2\bar{2}01$] and SP[$0\bar{2}2\bar{1}$] directions or with the SP[$11\bar{2}0$] and SP[$\bar{1}101$], respectively.

It is important to note that the epitaxial Si atoms will be linked to the R-plane sapphire substrate via bridging oxygen-atom sites.[1] As depicted in Figure 2c, the Type A seeding arrangement can be viewed as a 45° rotation from the Type B arrangement, while the former configuration has a larger oxygen-site spacing of 6.9 Å in the SP[$2\bar{2}01$] and SP[$02\bar{2}\bar{1}$] orientations, compared to that of 5.4 Å on Si(100), and the latter has a smaller spacing of 5.2 and 4.7 Å along the SP[$11\bar{2}0$] and SP[$\bar{1}101$] directions. Interestingly, the growth directions of the SoS in-plane SiNWs also follow these exact baseline alignments, as observed in Figure 2c. A close scrutiny of the Type A epitaxy SoS nanowires, marked by the yellow lines/arrows in Figure 2c, shows a slightly inclined turning angle of ∼85°, which is in contrast to the typical 90° turning angles observed for the Type B nanowires, marked by the green lines/arrows. This is not surprising if we examine the surface lattice vectors of the oxygen sites on the R-plane sapphire substrate, which actually represents a rhombus with a small 5° deviation from an exact square, as highlighted by the dashed lines in Figure 2c. Therefore, during an in-plane SoS growth along the Type A directions, the turning angle between the SoS segments is not exactly 90° but instead it is approximately 85°, which is consistent with the rhombus lattice vectors of the oxygen sites on the R-plane sapphire substrate. This also indicates that the lattice orientation of the underlying R-plane sapphire substrate has a unique and deterministic role in the growth direction of the in-plane SoS nanowires, even when the growth orientation is not fully consistent with the lattice symmetry of the c-SiNW matrix.

As illustrated in Figure 1d, a peculiar aspect of in-plane heteroepitaxial growth of SiNWs is that there are two competing and yet collaborating nucleation/deposition interfaces that coexist in the nanocatalyst droplet during the in-plane growth, that is, the bottom interface between the catalyst and the bottom sapphire substrate and the vertical interface between the catalyst and the rear SiNW end. This is extremely different from the conventional metal-droplet-mediated growth of nanowires (via the VLS mode), where only one nucleation and deposition interface exists. During the in-plane hetero-epitaxial growth, the formation of discrete new c-Si pyramid seeds occurs preferentially on the bottom heteroepitaxial interface (indicated by the red arrow in Figure 1d), while the lateral advancement of the vertical In/SiNW interface

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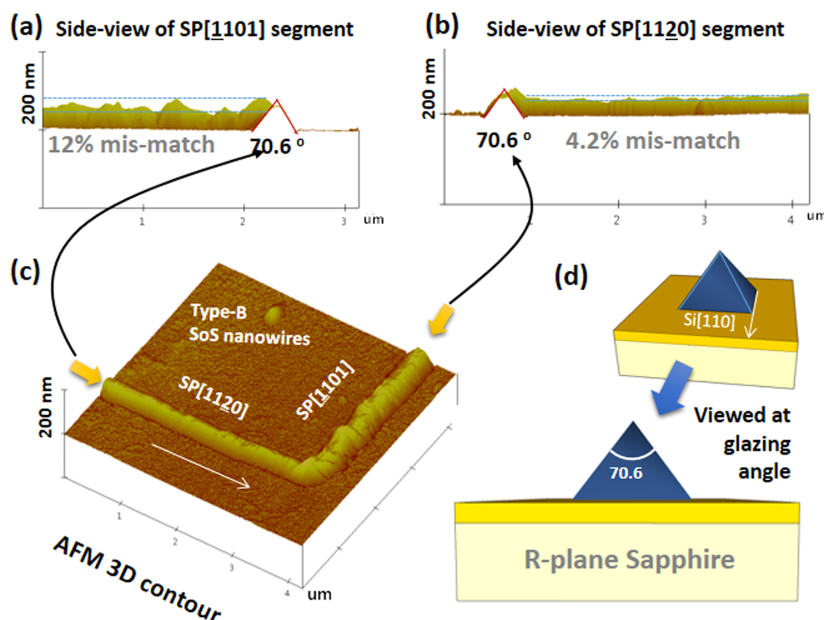

Figure 3. AFM analysis of the in-plane SoS SiNWs. (a,b) The glazing side-views, along the SP[1$\bar{1}$01] and SP[11$\bar{2}$0] orientations, respectively, of a segment of the SoS SiNW with 3D reconstruction images presented in (c). The cross-section angles of 70.6° observed in both (a) and (b) are identical to what is expected from a regular c-Si pyramid seed viewed at a glazing angle, as depicted in (d).

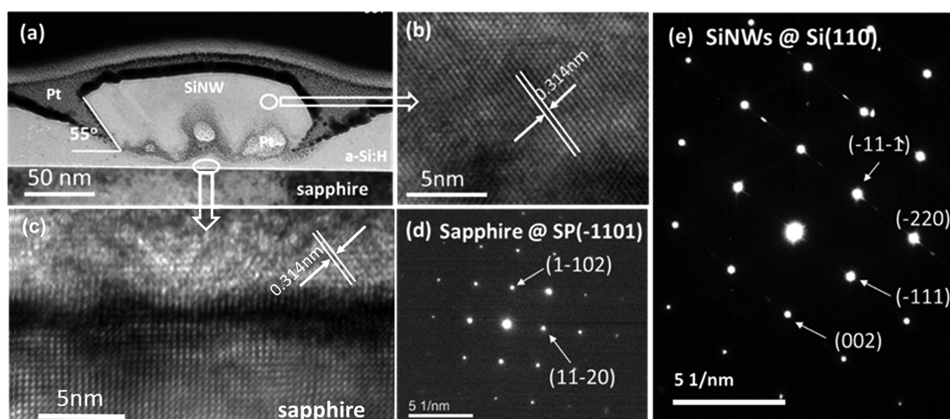

Figure 4. High-resolution electron transmission microscopy (HR-TEM) analysis of the in-plane SoS SiNWs. (a) Cross-section of an in-plane SoS nanowire, where the sample is protected by a thin layer of platinum coating to prevent damage during FIB milling; (b,c) the lattice images taken in the SiNW zone and at the heteroepitaxial interface, respectively, while the diffraction patterns of the SiNW and the sapphire substrate are shown in (e,d).

(represented by the blue arrow in Figure 1d) sweeps and merges the seeds into a continuous nanowire. As all the pyramid seeds have a coherent alignment relative to the sapphire substrate, the merging of them by a moving catalyst droplet in a "seeding-and-merging" scenario thus sets a preferential growth direction for the in-plane SiNWs, which leads to a self-alignment of the in-plane SiNWs on the R-plane sapphire substrate.

Meanwhile, it is worthy to note that the Type-A-oriented growth only occurs during the initial stage and is less stable or persistent than the Type-B-oriented growth, as observed, for instance, in Figure 2c. This can be attributed to a larger lattice mismatch in the Type-A epitaxial growth and the intrinsic misalignment between the inclined rhombus lattice and the square Si(100) arrangement; however, the detailed mechanism for this remains unclear.

In addition, this unique seeding-and-merging growth scenario can also be inferred from the atomic force microscopic (AFM) characterizations of a segment of the Type-B SoS nanowire that first develops along SP[$\bar{1}$101] and then turns into the SP[11$\bar{2}$0] orientations. As shown in Figure 3a–c, the 3D contour profiles reveal a rather rugged top surface of the SoS SiNW, particularly for the segment along the SP[$\bar{1}$101] direction, where the lattice mismatch of 12.5% is larger than that of only 4.2% along the SP[11$\bar{2}$0] direction. Remarkably, the spiky outline closely resembles a chain of merging pyramids, and the cross-section profiles of the SoS nanowires are also triangle-shaped (Figure 3a,b) with a top intersect angle of ~70.6°, which is precisely the projected side angle of regular Si pyramids, as highlighted in Figure 3d. This observation confirms that the SoS in-plane SiNWs have been assembled from discrete c-Si pyramid seeds in a seeding-and-merging scenario; moreover, under certain circumstances, their initial triangle cross-section geometry is preserved after the lateral merging growth. However, this geometric feature is not always apparent, as the sweeping lateral growth of the vertical In/

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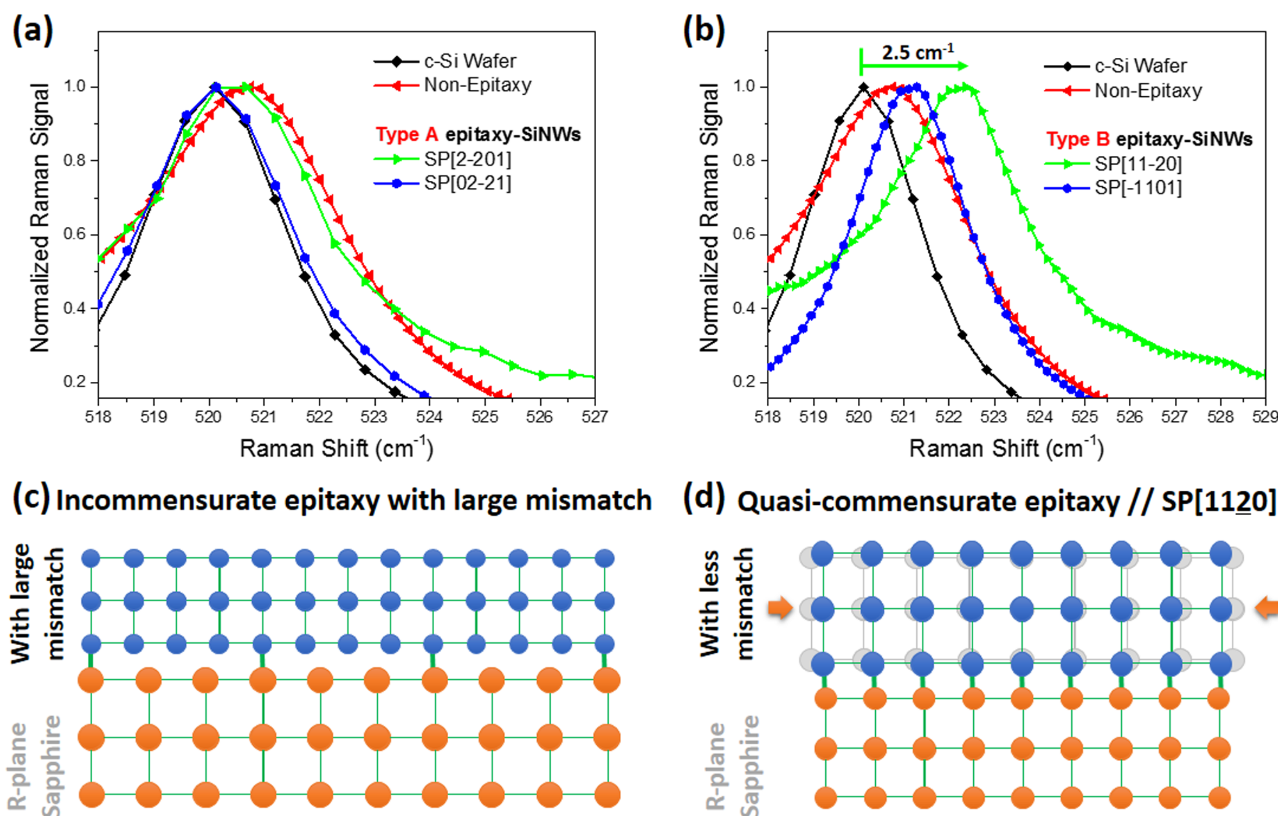

Figure 5. Raman spectroscopy of the SoS nanowires in different growth directions. (a,b) The Raman scattering spectra of the in-plane SoS SiNWs in Type A and Type B orientations, respectively, as well as the reference samples of the c-Si wafer and free SiNWs; (c,d) the incommensurate and quasi-commensurate atomic bonding configurations at the heteroepitaxial interface, when the lattice mismatch is large or less (as in the case of SoS nanowires along the SP[$11\bar{2}0$] orientation), respectively.

SiNW interface can smoothen the rugged details, as observed in the relatively larger SoS nanowires in Figure 2d.

The lattice quality of the heteroepitaxial SoS nanowires was first examined by cross-section high-resolution transmission electron microscopy (HR-TEM) characterization. To protect the nanowires from ion bombardment during focus-ion-beam (FIB) sample preparation, the nanowires were first covered by a platinum capping layer, sliced into thin cross-section specimens with the aid of FIB cutting and then transferred onto a copper grid for HR-TEM analysis. As shown in Figure 4, the growth direction of this SoS nanowire is along the SP[$\bar{1}101$] orientation in the sapphire system or the Si[110] orientation in the c-Si matrix, as determined by the diffraction patterns in Figure 4d and 4e. Note that the baseline directions of the pyramid seeds are all along Si ⟨110⟩ in the c-Si lattice matrix, regardless of their alignment with respect to the underlying sapphire orientations. Furthermore, the cross-section of the SiNW in Figure 4a reveals a smooth and round top edge line but clear facets are still observed on both sides. At the hetero Si/sapphire interface, we observe a coherent heteroepitaxial interface between the R-plane sapphire substrate and a thin c-Si layer. Unfortunately, the region between this epitaxial c-Si layer and the SiNW core region above has been seriously damaged and broken during the FIB milling and thus it is filled with a large amount of Pt. Nevertheless, by comparing the HR-TEM lattice image taken at the heteroepitaxial interface to that in the above-mentioned SiNW zone, as observed in Figure 4c,b, respectively, we found that their lattice spacing and orientations are indeed coherent, which confirms an epitaxial relation between the SoS nanowire the R-plane sapphire substrate. In addition, as shown in Supporting Information S-2, the cross-section analysis of a control sample, grown at a higher annealing temperature of 425 °C, also reveals a similar coherent lattice alignment between the in-plane SiNW and the underlying sapphire substrate. However, a seemingly higher density of twin or stacking fault lines has been identified in the cross section. The mechanism behind this remains unclear, and it has to be better understood in our future investigations.

Another important issue that can be investigated is the remnant strain introduced in the SoS nanowires during such a heteroepitaxial growth, as the lattice constant mismatch between c-Si and sapphire is clearly very large. To verify this point, Raman scattering spectroscopy provides a straightforward and nondestructive method to determine the lattice strain of SoS nanowires. Raman characterization was carried out at room temperature with a probing laser beam operating at a wavelength of 514 nm; the beam can be focused on targeted segments of the in-plane SiNW with a spot size of ∼3−4 μm, which is approximately the size of the disk labels marked in Supporting Information (SI) S-1a. The laser power has been carefully controlled to a minimal level; therefore, one can ensure that the effect of local heating is eliminated while maintaining a sufficient signal intensity for recording the spectra.

From Figure 5a,b, despite a large lattice mismatch along these epitaxial directions, the Raman spectra of the Type-A SoS nanowires grown along the SP[$2\bar{2}01$] and SP[$02\bar{2}\bar{1}$] orientations reveal only a slight blue shift of below 0.7 cm^{-1} with respect to the main TO mode scattering peaks of c-Si at 520 cm^{-1}, which is even smaller than that of free nanowires. In

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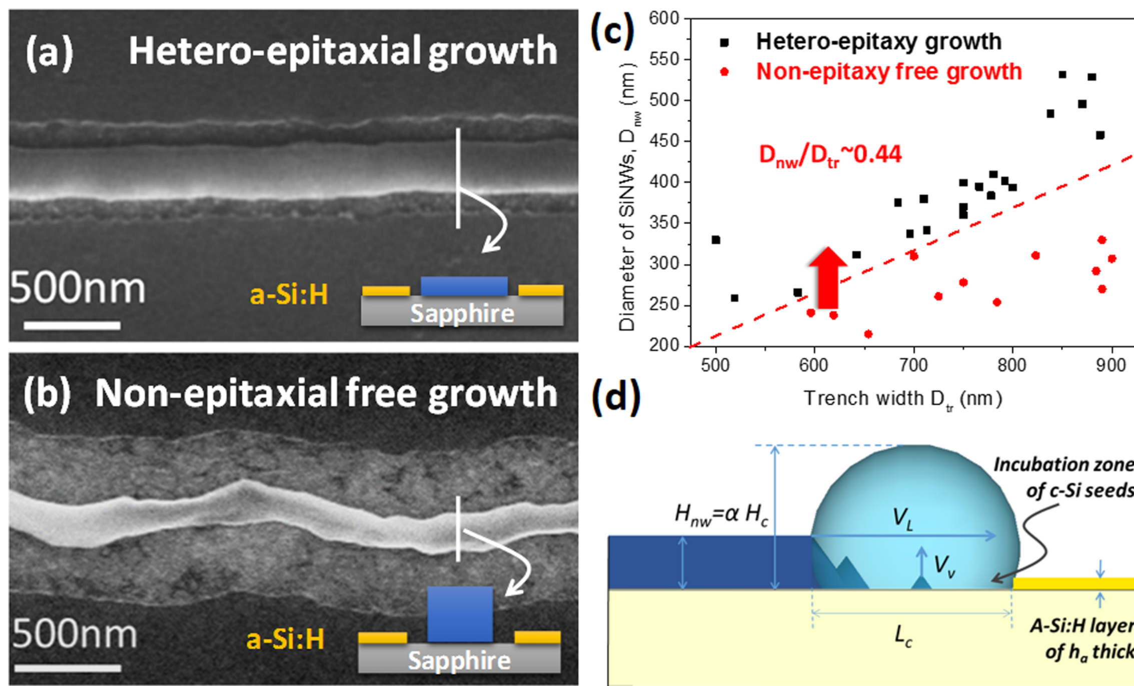

Figure 6. Morphological impacts of the heteroepitaxial growth on the in-plane SiNWs and geometric criteria for epitaxial growth. (a,b) The typical SEM images of the heteroepitaxial or nonepitaxial free in-plane growth of SoS SiNWs, respectively. (c) a statistics of the diameter of the SoS SiNWs D_{nw} against the trench width D_{tr} (which is proportional to the size of the catalyst droplet W_c), with a linear demarcation between the epitaxial and nonepitaxial SiNWs; this observation can be explained using a competitive interfacial nucleation model of the vertical and lateral development, as illustrated in (d).

comparison, a larger blue-shift of the Raman peak has been recorded for the Type-B SoS SiNWs, particularly for the epitaxial direction along SP[11$\bar{2}$0] that leads to a large $\Delta\omega$ = 2.3 ± 0.2 cm^{-1}. The exact places on the SoS nanowire segments, where the probe laser beams were focused on for Raman spectra characterization, are clearly marked in the SEM image in SI S-1a and displayed alongside their corresponding Raman peak curves in SI S-1b. Surprisingly, the largest blue shift has been found in the Type-B SiNW segments along the SP[11$\bar{2}$0] direction, which however has the least lattice mismatch of 4.2% with respect to the underlying substrate lattice. According to the formula in the reference[29]

$$\Delta\omega = -b\epsilon_{xx}^{\langle 110\rangle} = -337\epsilon_{xx}^{\langle 110\rangle} \quad (1)$$

this corresponds to a uniaxial strain of $\epsilon_{xx}^{\langle 110\rangle} < 0.6\%$ in the SiNW growth orientation of Si ⟨110⟩, which is 30% less than the typical strain (also determined by Raman spectroscopy) observed in planar SoS thin film growth.[30] In comparison, for all the Type-A SiNWs and the Type-B SiNWs along the SP[$\bar{1}$101] orientation (with a much larger lattice mismatch of 12.5%), the in-plane growth could only establish an incommensurate epitaxy in contact with the underneath R-plane sapphire substrate, as depicted schematically in Figure 5c, which thus allows a rapid relaxation of the large lattice mismatch. On the other hand, for the Type-B SoS SiNW in the SP[11$\bar{2}$0] orientation, a much smaller lattice mismatch makes it possible to establish a quasi-commensurate epitaxial growth, as illustrated in Figure 5d. In this mode, a significant amount of compressive strain can be introduced and stored in the as-produced SoS SiNWs. It is important to note that in general the strain level of the in-plane SiNWs, especially those of the incommensurate epitaxial growth, is much lower than that of the planar thin film SoS structure.[30] These findings indicate a promising strategy for manufacturing self-aligned and strain-relaxed SoS nanowire channels for device applications.

Among the epitaxial SoS SiNWs, we also observe non-epitaxial SiNWs that grow freely without a fixed orientation, as observed, for example, in the SEM image in Figure 6b, which features an irregular and twisted morphology compared to the straight and smooth epitaxial morphology in Figure 6a. This highlights the beneficial contribution of epitaxial growth in shaping the straight and uniform SiNWs. To gain insight into the epitaxial growth criteria of the in-plane SiNWs, the diameters of the in-plane SiNWs (D_{nw}) and the widths of their trench regions (D_{tr}) are extracted and plotted in Figure 6c. We found that there seems to be a clear demarcation between the groups of epitaxial and nonepitaxial grown SiNWs, by a line with an approximately constant ratio of $\alpha \equiv \frac{D_{nw}}{D_{tr}} = 0.44$.

To understand this phenomenon, one has to invoke the mass conservation condition during the in-plane growth of SiNWs, that is, the amount of a-Si:H taken by the In catalyst droplet should be, in principle, equal to that produced in terms of SiNW, which can be formulated as follows

$$D_{nw}H_{nw} = D_{tr}h_a \quad (2)$$

where h_a is the thickness of the a-Si/H layer, which is ~40 nm in this study, and H_{nw} is the height of the SiNW, which is proportional to the height of the catalyst droplet by $H_{nw} = \alpha H_c$. The same proportionality ratio is expected for the width of the catalyst $W_c = D_{tr}$ and the diameter of the SiNW W_{nw}, as $W_{nw} = \alpha W_c$ or $\alpha = D_{nw}/D_{tr}$. According to eq 2, we have the following

$$H_c = \frac{h_a}{\alpha^2}, \text{ and } H_{nw} = \frac{h_a}{\alpha} \quad (3)$$

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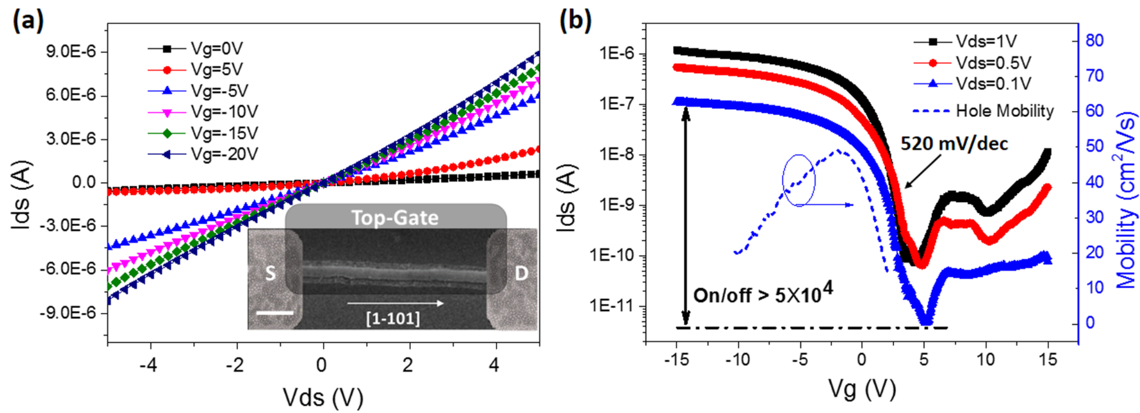

Figure 7. FET device performance based on the SoS nanowire channels. (a,b) The $I_{ds}-V_{ds}$ transport and $I_{ds}-V_g$ transfer properties of a single SoS in-plane SiNW FET device, respectively, in a top-gate configuration, as schematically illustrated in the inset of (a). The scale bar in the inset of (a) is 2 μm.

In a seeding-and-merging scenario, as illustrated in Figure 6d, once the absorption line passes over and exposes a fresh region of the sapphire substrate, the formation of new c-Si pyramid seeds will require an extra period with an incubation time of τ_{in}. After that, the c-Si seeds will grow up with a vertical speed of v_v and will reach the height of the SiNW after $\tau_v = H_{nw}/v_v$. In parallel, the rear vertical SiNW interface also advances at a speed of v_l, and thus it will pass this newly formed c-Si island after $\tau_l = L_c/v_l$, where L_c is the length of the catalyst droplet, as marked in Figure 6d. Ideally, one will expect $\tau_v + \tau_{in} = \tau_l$ for a balanced in-plane growth. In reality, the incubation time for forming a new seed should be allowed, $\tau_{in} > 0$, which thus puts the following constraint

$$\tau_v < \tau_l \rightarrow \frac{H_{nw}}{v_v} < \frac{L_c}{v_l} \tag{4}$$

For the sake of simplicity but without losing the generality, the total catalyst volume of $V_c = W_cH_cL_c$ can be considered as a constant. Substituting this and eq 4 into eq 3, we have the following

$$\alpha^3 > \frac{v_l}{v_v}\frac{W_c h_a^2}{V_c} \rightarrow \alpha = \frac{D_{nw}}{D_{tr}} > \left(\frac{v_l}{v_v}\frac{W_c h_a^2}{V_c}\right)^{1/3} \sim \left(\frac{h_a}{D_c}\right)^{2/3} \tag{5}$$

which is precisely the physical meaning of the linear demarcation boundary observed in Figure 6c. In other words, the rear SiNW deposition interface should not advance too fast with respect to the vertical growth rate of the c-Si pyramids, to allow a sufficient time to incubate all the new seeds directly on the bottom heterogeneous epitaxial interface instead of on the vertical SiNW interface. If the latter case occurs, the lateral growth will revert to a normal free growth mode with little influence from the bottom heterointerface. Meanwhile, according to eq 5, this threshold ratio can be controlled by tuning the relative a-Si:H layer thickness to the initial size of the catalyst droplet $D_c \equiv V_c^{1/3}$, and this will be very useful in promoting heteroepitaxial SoS nanowire growth in a wider parametric window.

It is extremely important to note that self-aligned in-plane SiNWs are advantageous for electric connection and device prototyping in the mainstream planar architecture, for example, the lateral epitaxial growth of ZnO or GaN nanowires via the VLS mode along facet-grooves structured on miscut sapphire substrates has recently been demonstrated.[11,12] To determine the electrical properties of the in-plane SoS SiNWs, we fabricated field effect transistor (FET) prototypes based on individual SoS nanowire channels. Prior to device fabrication, the samples were first cleaned in 15% diluted HCL acid solution for 10 min to remove the remnant indium catalyst droplets from the surface; then, individual SoS nanowires were connected by standard lithography and electron sputtering evaporation of stacking Al (150 nm)/Pt (50 nm) source-drain electrode contacts. In the next step, 60 nm Al_2O_3 was coated as a gate dielectric by the atomic layer deposition (ALD) technique, followed by the patterning and evaporation of an Al/Pt gate electrode to achieve a top-gated SoS FET configuration. As indicated in the inset of Figure 7a, this specific SiNW channel is along the SP[$1\bar{1}01$] direction with a mean diameter and channel length of 150 nm and 10 μm, respectively. Though no doping has been intentionally introduced during the growth, the transfer characteristic in Figure 7b clearly implies a p-type channel behavior in the heteroepitaxial SoS nanowire. This is due to the incorporation of In atoms that serve as p-type donors in c-Si.[23,31] Remarkably, a high on/off ratio of >5 × 10^4 has been achieved, with a subthreshold swing of 520 mV/dec The field effect hole mobility is also extracted, according to a simplified formula of $\mu_p = \frac{dI_{ds}/dV_g}{C_i V_{ds}(W/L)}$, where $C_i = \epsilon_0\epsilon_r/t_{Al203}$ and ϵ_0 and ϵ_r are the dielectric and relative dielectric constants of the Al_2O_3 layer, respectively, and the mobility is plotted in Figure 7b, with a peak mobility of 50 cm^2/V·s achieved at $V_g = -2$ V. Note that only the Type-B SoS nanowires were chosen for the device testing, as the Type-A SoS nanowires are less stable in epitaxial growth, and it is usually difficult to achieve a sufficient channel length for device manufacturing. In a group of 6 SoS nanowire FET devices, 3 in the SP[$1\bar{1}01$] and 3 in the SP[$11\bar{2}0$] orientations, the extracted peak mobility varies in a range from 30 to 50 cm^2/V·s, but this variation occurs without a clear dependence on the epitaxial orientations. This could either be due to the low and efficient dissipation of strain in the SoS nanowires or because this trend is too weak to be exhibited against other technical background fluctuations during the device fabrication. In addition, these preliminary test results are certainly limited by a poor surface passivation of the SiNW channels. In the latter case, a more systematic and precisely controlled investigation will be required in our future studies. Nevertheless, because all these have been achieved at a rather

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low temperature, below <350 °C, these initial prototype device performance results still highlight the potential of the in-plane heteroepitaxial SoS SiNWs to serve as functional building blocks for future SoS nanoelectronics.

In summary, we have demonstrated a unique nanoscale heteroepitaxy phenomenon of the in-plane writing growth of silicon-on-sapphire (SoS) Si nanowires on R-plane sapphire substrates via a novel nanoscale liquid droplet locomotion that enables both a self-alignment deployment and a tunable morphology control. Our investigation reveals a unique seeding-and-merging epitaxial growth scenario aided by two collaborating bottom and lateral interfaces. A dynamic competing model has been proposed to identify the key control parameter of the heteroepitaxial SoS nanowire growth. Moreover, at a relatively low temperature of <400 °C growth, we demonstrated SoS nanowire FET devices with a high on/off ratio >5 × 10^4 and a hole mobility >50 $cm^2/V{\cdot}s$. All these results indicate a new design principle and manufacturing strategy for future SoS electronics and optoelectronics.

■ ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge on the ACS Publications website at DOI: 10.1021/acs.nanolett.6b02004.

Raman spectra of in-plane heteroepitaxial Si nanowires in different orientation segments; HR-TEM cross-section analysis of the in-plane heteroepitaxial SoS nanowires grown at different annealing temperature (PDF)

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Notes

The authors declare no competing financial interest.

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■ REFERENCES

(1) Culurciello, E. *Silicon-on-Sapphire Circuits and Systems: Sensor and Biosensor Interfaces*; McGraw-Hill Professional: New York, 2009.
(2) Houssaye, A. P. R. d. l.; Russell, S. D.; Shimabukuro, R. L. *Proc. SPIE* **2004**, 145.
(3) Kelly, D.; Brindle, C.; Kemerling, C.; Stuber, M. In *The state-of-the-art of silicon-on-sapphire CMOS RF switches*; Compound Semiconductor Integrated Circuit Symposium, 2005. CSIC '05; IEEE: Bellingham, WA, 2005.
(4) Peregrine Semiconductor, UltraCMOS SOS. http://www.psemi.com/technologies/ultracmos-technology-platform (accessed Nov 14, 2016).
(5) Kelly, D.; Brindle, C.; Kemerling, C.; Stuber, M. In *The state-of-the-art of silicon-on-sapphire CMOS RF switches*, Compound Semiconductor Integrated Circuit Symposium, 2005. CSIC '05. IEEE, 2005.
(6) Zou, Y.; Chakravarty, S.; Chen, R. T. *Appl. Phys. Lett.* **2015**, *107* (8), 081109.
(7) Singh, N.; Hudson, D. D.; Yu, Y.; Grillet, C.; Jackson, S. D.; Casas-Bedoya, A.; Read, A.; Atanackovic, P.; Duvall, S. G.; Palomba, S.; Luther-Davies, B.; Madden, S.; Moss, D. J.; Eggleton, B. J. *Optica* **2015**, *2* (9), 797−802.
(8) Singh, N.; Hudson, D. D.; Eggleton, B. J. *Opt. Express* **2015**, *23* (13), 17345−17354.
(9) Baehr-Jones, T.; Spott, A.; Ilic, R.; Spott, A.; Penkov, B.; Asher, W.; Hochberg, M. *Opt. Express* **2010**, *18* (12), 12127−35.
(10) Yim, W. M.; Paff, R. J. *J. Appl. Phys.* **1974**, *45* (3), 1456−1457.
(11) Tsivion, D.; Schvartzman, M.; Popovitz-Biro, R.; von Huth, P.; Joselevich, E. *Science* **2011**, *333* (6045), 1003−1007.
(12) Schvartzman, M.; Tsivion, D.; Mahalu, D.; Raslin, O.; Joselevich, E. *Proc. Natl. Acad. Sci. U. S. A.* **2013**, *110* (38), 15195.
(13) Wagner, R. S.; Ellis, W. C. *Appl. Phys. Lett.* **1964**, *4* (5), 89.
(14) Dhalluin, F.; Baron, T.; Ferret, P.; Salem, B.; Gentile, P.; Harmand, J. C. *Appl. Phys. Lett.* **2010**, *96* (13), 133109−3.
(15) Yu, L.; Alet, P.-J.; Picardi, G.; Roca i Cabarrocas, P. *Phys. Rev. Lett.* **2009**, *102* (12), 125501.
(16) Yu, L.; Xu, M.; Xu, J.; Xue, Z.; Fan, Z.; Picardi, G.; Fortuna, F.; Wang, J.; xu, j.; Shi, Y.; Chen, K.; Roca i Cabarrocas, P. *Nano Lett.* **2014**, *14*, 6469−6474.
(17) Xue, Z.; Xu, M.; Li, X.; Wang, J.; Jiang, X.; Wei, X.; Yu, L.; Chen, Q.; Wang, J.; Xu, J. *Adv. Funct. Mater.* **2016**, *26*, 5352.
(18) Xue, Z.; Xu, M.; Zhao, Y.; Wang, J.; Jiang, X.; Yu, L.; Wang, J.; Xu, J.; Shi, Y.; Chen, K.; Roca i Cabarrocas, P. *Nat. Commun.* **2016**, *7*, 12836.
(19) Somaschini, C.; Bietti, S.; Trampert, A.; Jahn, U.; Hauswald, C.; Riechert, H.; Sanguinetti, S.; Geelhaar, L. *Nano Lett.* **2013**, *13* (8), 3607−3613.
(20) Wu, J.; Shao, D.; Dorogan, V. G.; Li, A. Z.; Li, S.; DeCuir, E. A.; Manasreh, M. O.; Wang, Z. M.; Mazur, Y. I.; Salamo, G. J. *Nano Lett.* **2010**, *10* (4), 1512−1516.
(21) Liu, Y.; Deal, M. D.; Plummer, J. D. *Appl. Phys. Lett.* **2004**, *84* (14), 2563−2565.
(22) Tersoff, J.; Jesson, D. E.; Tang, W. X. *Science* **2009**, *324* (5924), 236−8.
(23) Yu, L.; Chen, W.; O'Donnell, B.; Patriarche, G.; Bouchoule, S.; Pareige, P.; Rogel, R.; Salaun, A. C.; Pichon, L.; Roca i Cabarrocas, P. *Appl. Phys. Lett.* **2011**, *99* (20), 203104−3.
(24) Xu, M.; Xue, Z.; Yu, L.; Qian, S.; Wang, J.; Xu, J.; Shi, Y.; Chen, K. J.; Roca i Cabarrocas, P. *Nanoscale* **2015**, *7*, 5197−5202.
(25) Štich, I.; Car, R.; Parrinello, M. *Phys. Rev. B: Condens. Matter Mater. Phys.* **1991**, *44* (20), 11092.
(26) Roorda, S.; Doorn, S.; Sinke, W. C.; Scholte, P. M. L. O.; van Loenen, E. *Phys. Rev. Lett.* **1989**, *62* (16), 1880.
(27) Yu, L.; Roca i Cabarrocas, P. *Phys. Rev. B: Condens. Matter Mater. Phys.* **2010**, *81* (8), 085323.
(28) Yu, L.; Roca i Cabarrocas, P. *Phys. Rev. B: Condens. Matter Mater. Phys.* **2009**, *80* (8), 085313−5.
(29) Peng, C.-Y.; Huang, C.-F.; Fu, Y.-C.; Yang, Y.-H.; Lai, C.-Y.; Chang, S.-T.; Liu, C. W. *J. Appl. Phys.* **2009**, *105* (8), 083537.
(30) Englert, T.; Abstreiter, G.; Pontcharra, J. *Solid-State Electron.* **1980**, *23* (1), 31−33.
(31) Chen, W.; Yu, L.; Misra, S.; Fan, Z.; Pareige, P.; Patriarche, G.; Bouchoule, S.; Cabarrocas, P. R. i. *Nat. Commun.* **2014**, *5*, 4134.

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