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Direct Growth and Integration of Silicon Nanowire Transistors on Polymer Substrates

Xiaopan Song,[#] Junyu Fan,[#] Bin Sun, Yang Gu, Sheng Wang,* Junyang An, Duanwangde Liu, Junzhuan Wang, and Linwei Yu*

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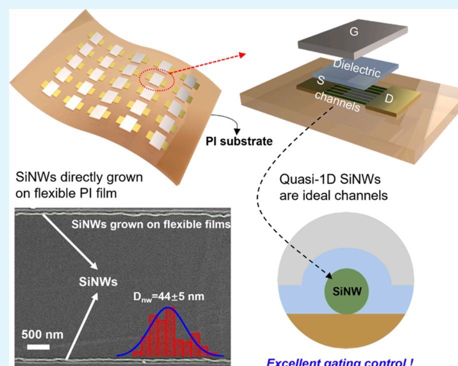
ABSTRACT: The direct low-temperature synthesis of crystalline silicon nanowires (c-SiNWs) on flexible polymer substrates remains a critical yet unrealized milestone for scalable flexible thin-film transistors (TFTs), hindered by the interfacial mechanical mismatch between rigid silicon and deformable polymers and the ultralow thermal budgets imposed by the flexible substrates. Though nanoscale SiNW channels can be patterned/grown and transferred onto polymer substrates, high-precision postgrowth transferring and alignment of these tiny SiNW channels remain technically difficult or too cost-intensive for the implementation of large-area electronics. Here, we demonstrate a direct growth of orderly c-SiNW channels upon a flexible polyimide (PI) film for the first time, through an in-plane solid−liquid−solid (IPSLS) mechanism at 200 °C, achieving uniform diameters of 44 ± 5 nm. The prototype flexible SiNW TFT can endure a bending radius of 6.5 mm for 10,000 cycles, while achieving a high I_{on}/I_{off} current ratio of ∼5 × 10^5, working stably in an ambient environment over 10 months without any passivation protection. These results represent the first experimental evidence that c-Si electronics can also be grown and integrated upon low-cost flexible substrate, opening a straightforward routine to harness the mature and stable c-Si device performance for future flexible electronics, optoelectronics.



KEYWORDS: silicon nanowires, direct growth, positioning integration, flexible electronics, thin-film transistor

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1. INTRODUCTION

Large-area flexible electronics are indispensable for contemporary portable and wearable technologies, offering exceptional flexibility and integration that significantly advance human−computer interaction and continuous health monitoring.[1−5] The crystalline silicon channel, leveraging its superior electrical performance, exceptional mechanical flexibility, and compatibility with well-established fabrication techniques, is widely adopted in large-area flexible electronics.[6−9] Specifically, quasi-one-dimensional (quasi-1D) crystalline silicon nanowires (c-SiNWs) have emerged as attractive candidates for next-generation flexible electronics, stemming from their unique combination of properties including a high surface-to-volume ratio, high crystallinity, high-density integration, and outstanding electrostatic modulation capability in fin-gate configurations, all of which collectively contribute to the realization of a series of excellent SiNW-based sensors and transistors.[10−16]

Given the growing demand for such advanced electronic components, various fabrication methods have been explored to meet the stringent requirements of diameters and flexibility. One established "top-down" method involves the physical fabrication of ultrathin c-SiNWs through high-resolution electron beam lithography (EBL) on silicon-on-insulator (SOI) substrates, as illustrated in Figure 1a.[17] However, this approach faces limitations due to its dependence on costly equipment/materials and the intrinsic resolution limits of lithographic processes. To address these challenges, alternative "bottom-up" chemical growth methods have been investigated. Notably, the vapor−liquid−solid (VLS) technique has been extensively used for producing high-crystallinity vertical SiNWs.[18−28] However, for the fabrication of planar electronic devices, vertically grown randomly oriented SiNWs at high temperatures (>700 °C) via the VLS mode typically require complex postgrowth transfer and alignment steps. Moreover, our previous work introduced an innovative in-plane solid−liquid−solid (IPSLS) growth mechanism,[29−34] which facilitates controlled and uniform SiNW growth on hard substrates at temperatures below 350 °C.[35]

Despite significant advancements, there have been no reports of direct integration of c-SiNWs on flexible substrates

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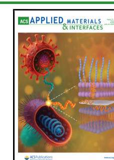

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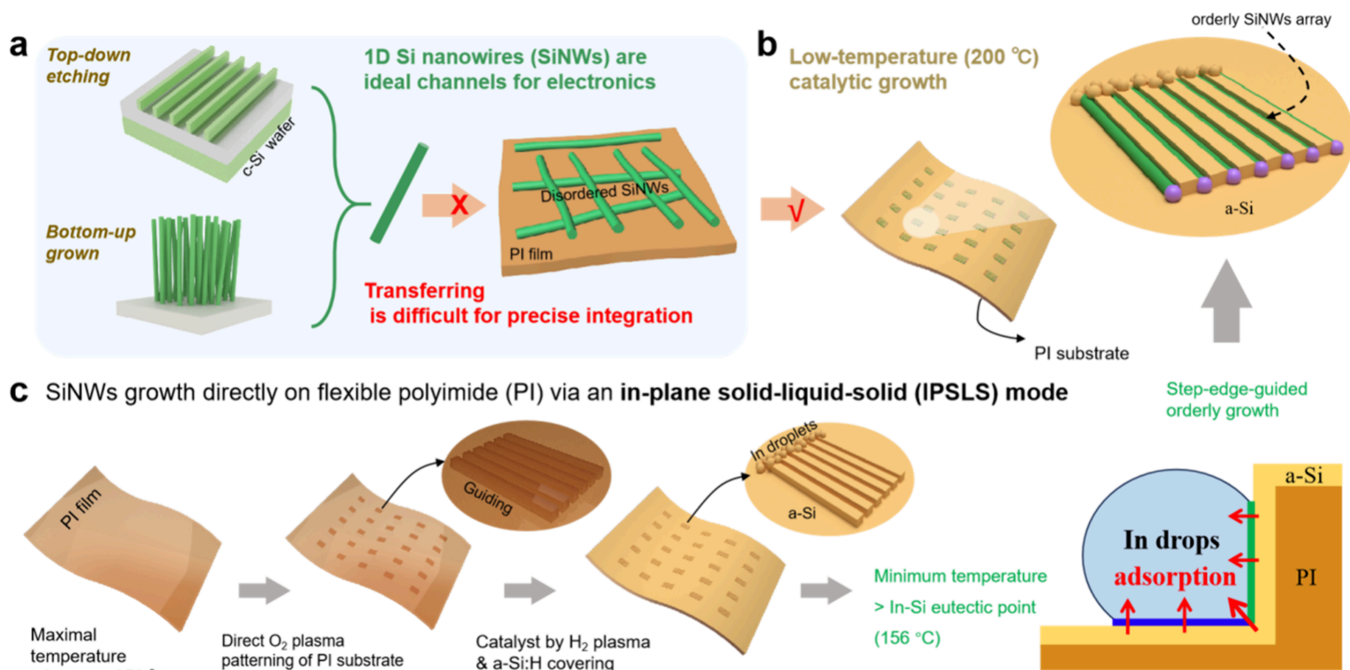

Figure 1. (a) Quasi-1D SiNWs fabricated via "top-down" etching and "bottom-up" grown methods serve as ideal channel materials, but their precise integration is hindered by transfer steps. (b) Low-temperature direct growth of an orderly SiNW array on polymer films offers a viable solution. (c) Key steps for directly growing orderly SiNWs on a flexible PI substrate via the IPSLS growth mode at only 200 °C.

to date, primarily due to the combined constraints of inherent mechanical incompatibility between crystalline silicon materials and flexible substrates,[36] and the ultralow thermal budgets required to prevent polymer degradation. Although many dry transfer techniques, such as contact printing and transfer printing, have enabled clean and scalable integration of ordered nanowires over large areas,[37−39] the postgrowth transfer process remains an essential step in these approaches. This requirement inevitably introduces additional complexity into the fabrication flow and often limits the positioning and alignment accuracy during integration. On the other hand, as illustrated in Figure 1b, direct positioning and growth enable more accurate placement of nanowires through a simpler fabrication process, facilitating higher-resolution patterning and superior alignment accuracy, which are both essential for advanced device architectures. However, realizing this paradigm requires overcoming a critical trade-off between achieving high-quality c-SiNWs and maintaining substrate temperatures below 250 °C, as polyimide (PI) substrates experience irreversible structural deformation when exceeding this thermal threshold. This approach is theoretically grounded in the thermodynamic requirement of exceeding the indium−silicon (In−Si) eutectic point (156 °C), which represents a critical thermal boundary condition required for initiating catalytic droplet activation and maintaining sustained nanowire crystallization dynamics. More critically, achieving in situ control over nanowire placement and morphology on flexible substrates is paramount for advancing high-performance flexible electronics. Such a capability significantly accelerates the development of advanced flexible devices by enabling precise control over device architecture and performance optimization. These unmet needs underscore the necessity for disruptive methodologies enabling direct growth of c-SiNW channels on flexible substrates, such as PI foil.

In this work, we demonstrate the direct positioning and growth of an orderly SiNW array on a flexible PI film for the first time, at a remarkably low temperature of 200 °C, with an average diameter of approximately 44 nm, achieved via the in-plane solid−liquid−solid (IPSLS) growth mechanism. The fabricated prototype flexible SiNW thin-film transistors (TFTs) demonstrate an I_{on}/I_{off} ratio as high as $\sim 5 \times 10^5$, and repetitive testing for more than 10,000 cycles (with 6.5 mm bending radius), verified with a numerical model. An integrable approach has been developed and experimentally validated, fundamentally addressing the challenge of directly integrating crystalline silicon materials onto flexible substrates, thereby establishing a silicon-compatible roadmap for the high-throughput fabrication of multifunctional flexible electronics at the industrial scale.

2. RESULTS AND DISCUSSION

Figure 1c shows the key steps for directly growing orderly SiNWs on a flexible PI substrate via an IPSLS growth mode at 200 °C. First, guiding steps were carved on the PI substrate using standard photolithography and inductively coupled plasma (ICP) etching. Afterward, indium (In) stripes were patterned and evaporated at the termini of the guiding edges. Subsequently, the sample was transferred into a plasma-enhanced chemical vapor deposition (PECVD) system for hydrogen (H_2) plasma treatment to reduce the native oxide layer on the In film. When the In film is activated into In droplets, an amorphous silicon (a-Si) layer was then deposited. Then, the In droplets absorbed the surrounding a-Si, generating aligned SiNWs along the predefined guiding edges at 200 °C. The diameter of the SiNWs is primarily determined by the size of the In catalyst droplets.[29,30,40] This size can be controlled by adjusting the initial In film thickness and H_2 plasma treatment conditions. Thicker In films or higher treatment temperatures enhance surface diffusion and droplet

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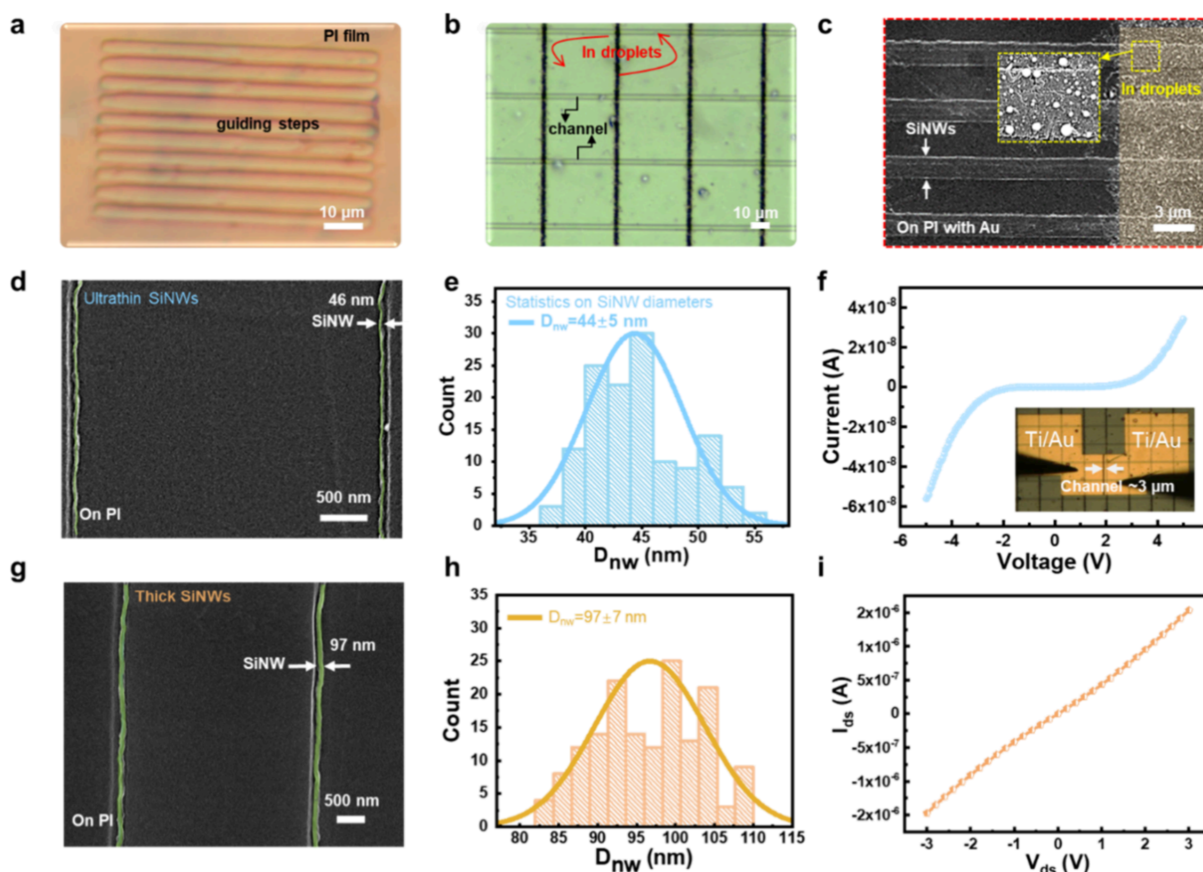

Figure 2. (a) Typical optical microscope image of plasma-patterned guiding steps on a PI film. (b) Optical microscope image of grown SiNW channels and In droplets. (c) SEM image of SiNWs and In droplets, with an inset showing a magnified view of In droplets. (d−f) Enlarged SEM examinations, diameter statistics, and output characteristics of thin SiNWs in contact with Ti/Au electrodes, respectively. An optical image of the device structure is provided in the inset of (f). (g−i) Corresponding enlarged SEM examinations, diameter statistics, and output characteristics of thick SiNWs with Ti/Au contacts.

coalescence, leading to larger catalyst particles and thus thicker SiNWs. Note that ultrathin SiNWs with even stricter uniformity have already been fabricated by using surface nanogrooves, sidewall grooves, or edge-trimming technology in our previous works.[41−43] The growth velocity in this work is estimated to be >30 nm/s, by dividing the length of SiNWs over the growth duration. After growth, unreacted a-Si was selectively etched using CF_4. Finally, the source and drain electrodes, SiN_x dielectric, and gate electrode were sequentially deposited to fabricate the SiNW TFT. Additional experimental details are provided in Section 4.

The growth of SiNWs on PI substrates via the IPSLS growth mode occurs through a thermally activated process at ∼200 °C. In this process, a liquid In catalyst droplet absorbs and transforms the surrounding solid a-Si precursor. As the concentration of Si atoms within the catalyst increases, it eventually reaches a state of supersaturation. The maximum supersaturation that can be established (at ∼200 °C) in the In catalyst is estimated to be[29]

$$S = C_{Si}/C_{eq}^{c} = e^{\Delta\mu/kT} \leq e^{\Delta E_{ac}/kT} \approx 19.2 - 39.6 \quad (1)$$

where C_{Si} and C_{eq}^{c} are the concentrations of the dissolved Si atom in an In catalyst droplet and the equilibrium Si concentration at the SiNW/In interface, respectively. This supersaturation is driven by the Gibbs energy difference between the amorphous and the crystalline Si phases.[30] The higher Gibbs potential energy in the a-Si matrix (E_a) as compared to that In crystalline SiNWs (E_c) is[44,45]

$$\Delta E_{ac} = E_a - E_c \approx 0.12 - 0.15\text{eV} \quad (2)$$

This supersaturation facilitates the stable formation of silicon nucleation seeds within the In droplet, which then grow at the interface between the catalyst, a-Si, and flexible PI substrate. The largest silicon seeds cause the catalyst droplet to tilt, propelling it forward and allowing it to absorb more a-Si from ahead. Subsequently, the nucleation seeds continue to expand and generate c-SiNWs.

However, because the catalyst droplets have only one absorption face at the bottom in contact with the a-Si layer, this causes the droplets to tilt within a 2D plane, making it difficult to maintain a straight growth trajectory. Therefore, guiding steps on the flexible PI substrate are predefined through photolithography and etching processes, followed by the deposition of an a-Si layer. The catalyst droplets near the step edges will absorb the deposited a-Si layer on the step sidewalls and firmly adhere to them,[34] as indicated by the green line in Figure 1c. This enables the precise guided growth of straight SiNWs. Notably, during the IPSLS growth mode, SiNWs exhibit a self-avoiding characteristic,[30] indicating that randomly grown SiNWs do not interfere with the directionally grown SiNWs at the step edges.

Figure 2a presents an optical microscope image of O_2 plasma-patterned guiding steps on a PI foil. In droplets

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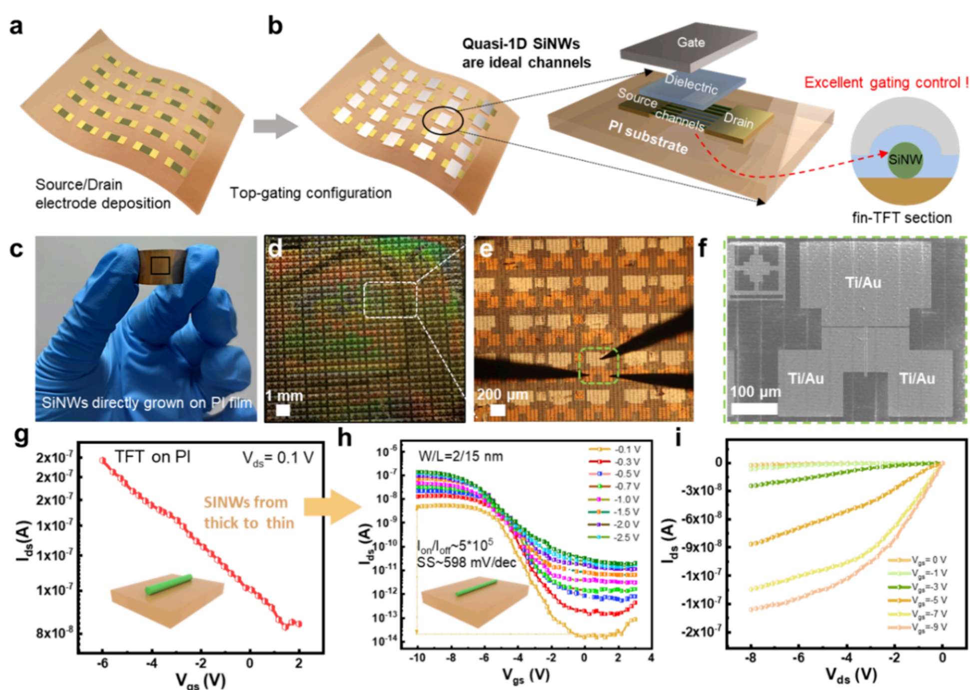

Figure 3. (a) Schematic illustration of the fabrication for SiNWs with Ti/Au contacts. (b) Device schematic of fin-structured quasi-1D SiNW TFT array, including a magnified view of the architecture and a cross-sectional profile of the channel region. (c) Optical image of the flexible SiNW TFT array. (d) Close-up of the SiNW TFT array, with the white dashed box marking the region magnified in (e). (f) SEM image of an individual SiNW TFT device. The transfer characteristics of thick and thin SiNW TFTs are shown in (g) and (h), respectively, while the output characteristics of the thin SiNW TFT are presented in (i).

migrated along the step edges, leading to the growth of c-SiNWs as shown in Figure 2b, highlighting their precise orientation and relatively uniform diameter. Figure 2c shows an enlarged SEM view of the SiNWs (artificially colored green for enhanced visibility). A thin layer of gold nanoparticles (∼2 nm thick) was sputter-coated onto the sample to improve conductivity during imaging. The inset reveals the microscopic morphology of the catalytic In droplet residing at the growth front, illustrating its role in directing the anisotropic growth of the nanowires. By precisely modulating the growth parameters, both thin and thick SiNWs were successfully grown. Figure S1 presents SEM images showing that 98% of the SiNWs grown across each transistor channel (20 wires per device) exhibit straight and well-aligned morphology. Figure 2d displays a representative SEM image of the thin SiNWs, while the statistical analysis in Figure 2e confirms their narrow diameter distribution, averaging 44 ± 5 nm. To evaluate their electrical properties, titanium/gold (Ti/Au) electrodes were directly deposited at both ends of the thin SiNWs, forming a channel length ((L_{ch}) of ∼3 μm (Figure 2f). The observed bilateral Schottky barriers enable effective gate-controlled switching in Schottky barrier tunneling field-effect transistors (SBT FETs), as these barriers function similarly to p−n junctions in conventional metal-oxide-semiconductor field-effect transistors (MOSFETs), allowing efficient modulation of the source−drain current by gate electrodes. For comparison, analogous experiments were conducted on thick SiNWs as illustrated in Figure 2g−i, which demonstrated similarly excellent diameter controllability, averaging 97 ± 7 nm. However, unlike their thin counterparts, the thick SiNWs exhibited Ohmic behavior when interfaced with Ti/Au contacts. This metallic-like conduction mechanism renders them ineffective for gate modulation, highlighting the critical role of nanowire diameter in tailoring electronic transport properties for specific device functionalities.

These observations reveal that, as the diameter increases from ∼40 to around 100 nm, the electrical properties of SiNWs undergo substantial alterations, attributed to dielectric confinement, quantum confinement effects, doping concentration, and other factors.[46,47] The ionization of impurities in fine SiNWs is suppressed due to these confinements, resulting in an increase in the ionization energy as the size decreases. When the diameter of the SiNWs approaches the Bohr radius of the impurity, the ionization energy of the impurity increases due to the quantum-limited transport of charge carriers, but this is not as apparent in the 40 nm experimental size. Therefore, the main factor affecting the ionization energy may be dielectric confinement. Due to the dielectric mismatch between the SiNWs and its surroundings, the Coulomb potential of the impurity is not fully screened in the SiNWs. This dielectric confinement phenomenon is particularly noticeable in small sizes, leading to further enhancement of the ionization energy. The impurity is less likely to be ionized, reducing the doping efficiency and resulting in a reduced effective doping concentration. Lower effective doping makes the metal−semiconductor contact exhibit the characteristics of a Schottky contact and increases the resistivity. At the same time, thin SiNWs may be more easily affected by interface state defects, leading to a decrease in their mobility. As the diameter of the SiNWs increases to ∼97 nm, the influence of dielectric confinement and quantum confinement weakens, the suppression of impurity ionization decreases, and the effective doping concentration is raised. Additionally, in our previous work, the SiNWs with larger diameters typically had an equivalent concentration of approximately 10^{19} cm^{-3},[48] while the thin SiNWs had an equivalent concentration of 10^{17} cm^{-3}.[49]

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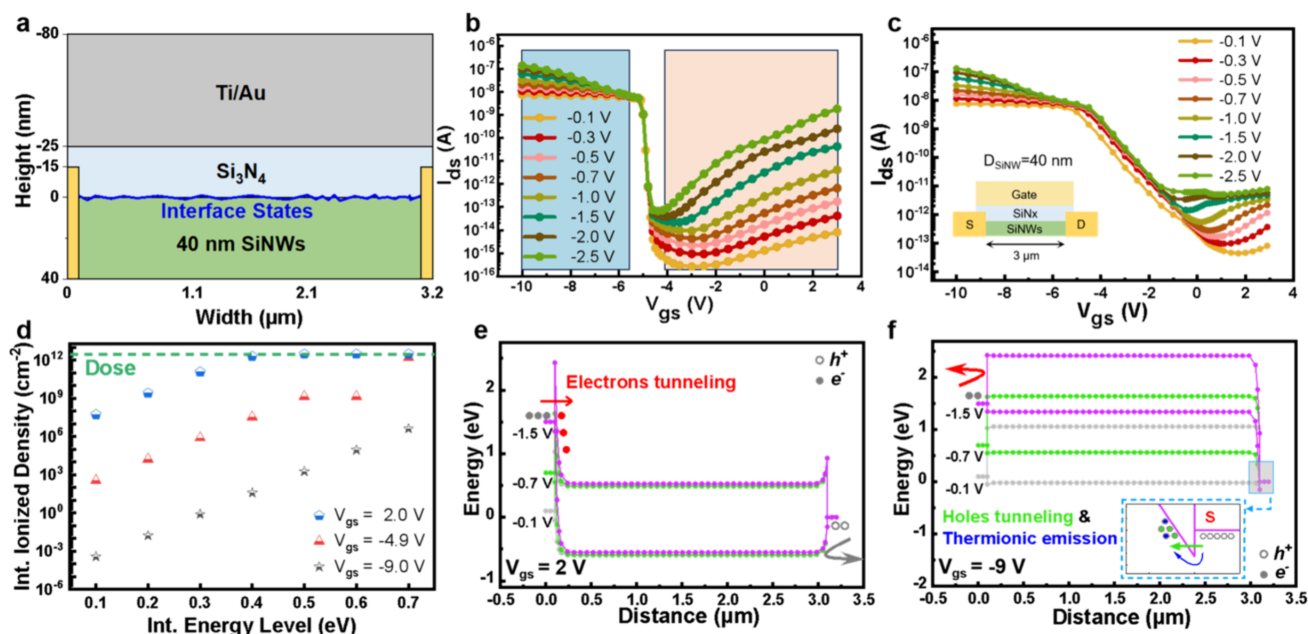

Figure 4. A simulation model of SiNW TFTs was established in (a), with dimensions marked. (b) Transfer characteristics of a typical SBT FET. (c) Transfer characteristics of a modified SBT FET. (d) Simulated dependence of the ionized acceptor density at the interface state defect levels varies with V_{gs} for the modified SBT FET model. The band diagrams in the cutoff region (V_{gs} = 2 V) and the saturation region (V_{gs} = −9 V) are presented in (e) and (f), respectively, showing their variation with V_{ds} along with a schematic illustration of the carrier transport mechanism.

Crucially, this diameter-dependent variation in doping concentration, which is governed by quantum confinement effects, serves as the determining factor in controlling the interfacial transition between the Schottky and Ohmic contact configurations.

Afterward, the source/drain (S/D) electrodes, SiN_x dielectric, and gate electrode were sequentially deposited to fabricate the SiNW TFT, as schematically illustrated in Figure 3a,b. The cross-sectional view of the fin-TFT channel highlights its enhanced gate controllability. Figure 3c,d shows images of the SiNW TFT array directly grown on a PI substrate, demonstrating good flexibility and scalability in integration. Additional optical microscopy images (top view) in Figure 3e display an array of device units on the flexible PI substrate. Figure 3f presents an enlarged SEM view of a TFT device configuration, where both the source/drain and gate electrodes are made of Ti/Au. The thick SiNW TFT in Figure 3g exhibits uncontrolled transfer characteristics with poor off-state behavior, indicating an inefficient gate modulation. In contrast, the thin SiNW TFT (Figure 3h) achieves a significantly enhanced switching performance, demonstrating an I_{on}/I_{off} ratio of ∼5×10^5 under V_{ds} = −0.1 V bias. However, our prototype device is significantly limited by the presence of interface trap charges. These trap states degrade the electrostatic gate control and result in a higher subthreshold swing (SS ∼ 598 mV/dec) and difficulty in extracting the actual carrier mobility (due to the Schottky barrier contacts at S/D electrodes). The corresponding output characteristics in Figure 3i further validate its modulation ability, showing p-type characteristics, which are attributed to the incorporation of In atoms into c-SiNWs during planar growth.[48]

For the mechanical stability, the device retained approximately 72% of its initial performance after 10,000 bending cycles at a bending radius of 6.5 mm, as shown in Figure S2. In addition, the temperature stability was tested from 25 to 50 °C, which covers the typical physiological temperature range. The device maintained >71% of its original performance, as presented in Figure S3. Furthermore, we tested the performance of the device after it was placed for 10 months, demonstrating extremely strong stability, even without passivation protection (Figure S4). These results confirm the excellent structural integrity, mechanical robustness, and thermal stability of the fabricated transistors, supporting their potential for use in flexible and wearable electronics.

To thoroughly study the characteristics of the fabricated SiNW TFTs, a simulation model based on the Silvaco model was established. Figure 4a shows the detailed structure and size parameters of the model established, on which a traditional SBT FET simulation[50] and a modified simulation were conducted. The comprehensive simulation parameters are provided in detail in the Supporting Information (Table S1). The corresponding transfer characteristics are shown in Figure 4b and Figure 4c, respectively. Notably, the modified model's simulation results closely resemble the experimental data presented in Figure 3h. For analytical clarity, the transfer characteristics are categorized into three regions, as labeled in Figure 4b: the saturation region (blue area), the cutoff region (yellow area), and the subthreshold region (middle area). A typical transfer characteristic simulation of an SBT FET is shown in Figure 4b for the purpose of assisting in understanding the conduction mechanism of the fabricated SiNW TFTs. Obviously, as a p-type device, a negative bias should be applied to the SiNW TFTs. Therefore, the majority of carrier holes flow from the source to the drain. Unlike traditional MOS devices, in the cutoff region, as depicted in Figure S5a, holes are blocked by a wide and high barrier and do not participate in conduction, while minority carriers' electrons tunnel through the narrow triangular barrier at the drain to participate in conduction. The increase in the negative V_{ds} bias applied to the electron barriers adds an additional tunneling current on top of the previously flat cutoff leakage current. In the saturation region, the current is primarily

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composed of the thermionic emission current of holes across the source barrier and the hole tunneling current through the narrow triangular barrier induced by the bias voltage, without the involvement of electrons, as shown in Figure S5b.[50] As the drain bias increases, the narrow triangular hole barrier at the source is squeezed, which improves the tunneling current.

Then, the simulated transfer curve with interface state defects taken into account is shown in Figure 4c, where a good simulation trend is obtained. Based on the transfer curve (Figures 3h) and hysteresis test (Figure S6) of the SiNW TFT, we infer that the interface state of the device is dominated by a negative acceptor. The extracted acceptor ionization charge densities at different bias voltages are shown in Figure 4d. As the gate voltage is increased in the positive direction, the quasi Fermi level in the channel is gradually raised relatively, and the ionization rate of the interface state acceptor continuously increases until it is fully ionized, which means that in the cutoff region, there is a large amount of interface state negative acceptor impurities that interfere with the gate's control ability. This effectively isolates the external electric field from influencing charge transport,[51] demonstrating a distinct energy band in the cutoff regions of Figure 4e and Figure S5a. In the saturation region, the ionized interface defect density is very low and its influence on the characteristics of the saturation region is relatively small. Therefore, the band structure and conduction mechanisms in Figure 4f and Figure S5b are essentially the same.

As mentioned earlier, interface defects introduce a nearly 3 V clockwise hysteresis (Figure S6a) in the SiNW TFT during voltage sweeps,[52,53] which can be accurately simulated by considering the interface state charge in the model shown in Figure S6b, as it arises from the interface state characteristics of SiN_x.[54−56] Increasing the gate voltage during scans ionizes neutral acceptors, introducing negative charges at the interface, which explains the hysteresis in the reverse scan. This indicates that acceptor defects significantly impact device performance through the interface states.

Compared to the flexible TFTs reported in the literature, as summarized in Table S2, the SiNW TFT can survive a bending radius of 6.5 mm for 10,000 cycles, while achieving a high I_{on}/I_{off} current ratio of ∼5 × 10^5. More importantly, these SiNW channels can be precisely and directly grown on polymer substrates, preparing them for the manufacturing and integration of scalable devices on soft elastomeric substrates. This approach establishes a robust platform for incorporating c-Si electronics into flexible electronic applications.

3. CONCLUSIONS

In this work, we demonstrate the reliable integration of precisely positioned, orderly SiNW arrays with a uniform thin diameter of 44 ± 5 nm, directly grown on predesigned locations via IPSLS growth mode for the first time at a low temperature of only 200 °C. The SiNW TFT exhibits a high I_{on}/I_{off} ratio of approximately 5 × 10^5 and can survive a bending radius of 6.5 mm for 10,000 cycles, indicating their potential for practical applications. Numerical simulations further revealed that optimizing interface states will enhance device performance and mitigate hysteresis effects. These advancements suggest that the SiNW TFTs can be directly integrated onto flexible substrates with broadened capabilities, bridging high-performance crystalline semiconductors with mechanically compliant systems and propelling the progress of next-generation flexible display and wearable electronic applications.

4. EXPERIMENTAL SECTION

Growth of SiNWs on a Flexible PI Substrate. First, the PI film (∼100 μm) was subjected to ultrasonic cleaning using acetone, ethanol, and deionized water, each for 10 min, and then the substrates were dried with N_2 gas. Second, guiding steps were patterned via photolithography, followed by ICP etching with oxygen plasma to carve guiding edges approximately 100 nm deep into the PI. The In stripe (10 nm) is subsequently deposited at the termini of guiding edges, accomplished through a series of steps: photolithography, thermal evaporation, and lift-off. Third, samples were loaded into the PECVD system and subjected to H_2 plasma treatment at 180 °C for 5 min to eliminate the native oxide layer from the surface of the indium particles, with the gas flow rate set to 15 sccm, chamber pressure to 140 Pa, RF voltage to 14 V, and RF power to 10 W. Subsequently, a 10 nm-thick a-Si film was deposited at 150 °C for 3 min, with the gas flow rate set to 15 sccm, chamber pressure to 20 Pa, RF voltage to 13 V, and RF power to 2 W. Next, the growth was activated under high vacuum at 200 °C for 30 min. During this period, the indium film was activated into indium droplets, which migrated along the predefined step edges via dual a-Si adsorption interfaces, generating SiNWs in their wake. Finally, unreacted a-Si was selectively etched by CF_4 gas in the reactive ion etching (RIE) system for 4 min, with the gas flow rate set to 30 sccm, chamber pressure set to 3 Pa, and RF power set to 5 W.

Fabrication of Flexible SiNW TFTs. Source and drain electrode regions were then patterned using photolithography techniques, and a 4.0% HF solution for 5 s was used to eliminate the oxide layer from the surface of the SiNWs. Subsequently, Ti/Au (5/55 nm) (S/D) electrodes were deposited via electron beam evaporation (EBE), followed by a lift-off process to deposit the metal only in designated areas. Then, a 25 nm SiN_x layer was deposited as a gate dielectric in the PECVD system at 200 °C, followed by the evaporation of Ti/Au (5/55 nm) as the gate electrode by EBE and open via holes upon the source and drain electrodes by SF_6 plasma etching in the flexible PI substrate.

Simulation Setup. The electrical stimulation of the flexible SiNW TFT device was conducted using the Silvaco Technology Computer-Aided Design (TCAD) simulator, with the dimensions and electrical parameters detailed in Figure 4a and Table S1. The included simulation physical model explains the partial contributions of thermal emission and tunneling current by the Trap-Assisted Tunneling model and the Universal Schottky Tunneling model, as well as the SRH, Fermi, CVT models.

■ ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge at https://pubs.acs.org/doi/10.1021/acsami.5c11278.

(Figure S1) SEM image of grown SiNWs; (Figure S2) cyclic stability test; (Figure S3) temperature stability test; (Figure S4) long-term stability test; (Figure S5) band diagrams of a typical SBT FET model in the cutoff region (V_{gs} = 2 V) and the saturation region (V_{gs} = −9 V); (Figure S6) hysteresis characteristic and its simulation; (Table S1) Silvaco simulation parameters; and SBT FET simulation (PDF)

■ AUTHOR INFORMATION

Corresponding Authors

Sheng Wang − *School of Future Science and Engineering, Soochow University, Suzhou 215222, P. R. China;* orcid.org/0009-0009-5385-1283; Email: shengwang@suda.edu.cn

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Linwei Yu − *School of Electronics Science and Engineering, Nanjing University, Nanjing 210023, P. R. China;* orcid.org/0000-0002-0801-5210; Email: yulinwei@nju.edu.cn

Authors

Xiaopan Song − *School of Electronics Science and Engineering, Nanjing University, Nanjing 210023, P. R. China*

Junyu Fan − *School of Future Science and Engineering, Soochow University, Suzhou 215222, P. R. China*

Bin Sun − *School of Future Science and Engineering, Soochow University, Suzhou 215222, P. R. China*

Yang Gu − *School of Future Science and Engineering, Soochow University, Suzhou 215222, P. R. China*

Junyang An − *School of Electronics Science and Engineering, Nanjing University, Nanjing 210023, P. R. China;* orcid.org/0009-0008-2522-5165

Duanwangde Liu − *School of Electronics Science and Engineering, Nanjing University, Nanjing 210023, P. R. China*

Junzhuan Wang − *School of Electronics Science and Engineering, Nanjing University, Nanjing 210023, P. R. China*

Complete contact information is available at: https://pubs.acs.org/10.1021/acsami.5c11278

Author Contributions

[#]X.S. and J.F. contributed equally to this study.

Notes

The authors declare no competing financial interest.

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