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Lithography-free, site-controlled germanium quantum dots in silicon nanowires for single-hole transistors operating up to 50 K

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Precise control over quantum dot (QD) position and size is critical for quantum electronics but typically requires complex nanofabrication. Here, we report a step-confined heteroprecursor supply (sc-HPS) strategy for growth of crystalline germanium (c-Ge) QDs at predefined step edges within planar ultrathin silicon nanowire (SiNW) channels, eliminating the need for high-resolution lithography. Unlike conventional in-plane solid-liquid-solid growth using a uniform amorphous silicon precursor, sc-HPS uses a spatially confined amorphous germanium (a-Ge) layer defined by oblique patterning of a SiO_2/a-Ge stack. This restricts Ge supply to a narrow strip along the step edge, enabling nucleation and tunable QD diameters of ~25 to 150 nm, sandwiched between two epitaxially connected SiNWs. The SiNW/Ge-QD/SiNW heterostructure forms a Si/Ge interface that provides three-dimensional hole confinement. Single-hole transistors fabricated from these structures exhibit clear Coulomb oscillations and well-defined Coulomb diamonds up to 50 K, demonstrating single-hole charging behavior. This scalable and lithography-free approach enables previously unexplored opportunities in hole-based quantum devices and nanoelectronic architectures.

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INTRODUCTION

The realization of well-defined, precisely positioned quantum dots (QDs) exhibiting single-electron or single-hole blockade is central to quantum device engineering, as such structures enable controlled access to discrete charge states and serve as fundamental building blocks for spin-based qubits in quantum computing and single-charge detection in quantum sensing (as illustrated in Fig. 1A) (*1*–*5*). Among various material platforms, holes in germanium (Ge) are particularly promising candidate for spin-based quantum technologies (*6*). They offer strong spin-orbit coupling, enabling all-electrical control of spin states and simplified device architectures (*7*), along with high hole mobility (*8*–*10*), long spin coherence times (*11*), absence of low-energy valley degeneracies (*12*), and full compatibility with complementary metal-oxide semiconductor (CMOS) processes (*13*). In canonical Ge single-hole transistors (SHTs) (*14*–*16*), a QD is formed by confining carriers within a nanoscale region where charge addition energy becomes quantized. Observing the Coulomb blockade, a hallmark of such quantization, requires the charging energy (E_C) to exceed the thermal energy (K_BT). This condition typically limits the QD size to a few tens of nanometers (*17*) and necessitates the use of ultrahigh-precision nanofabrication techniques (*18*–*21*), thereby posing a major challenge for scalable quantum integration.

To date, Ge-QDs are primarily realized through two approaches: band-engineered confinement in heterostructures, such as silicon/germanium (Si/Ge) quantum wells (*22*–*30*) or strain-induced Ge hut wires (*31*–*38*), and size-confinement strategies in quasi–one-dimensional (1D) channels, such as the Si/Ge core-shell nanowires (NWs) grown via vapor-liquid-solid (VLS) mechanism (*39*–*43*) (Fig. 1B). More recently, V-groove–confined selective epitaxy has enabled reproducible on-chip integration of GeNW QDs with tailored positioning (*44*). In addition, additional ultrafine gating electrodes are required to impose further electrostatic confinement potential to shape/define the QDs within the quasi-2D or 1D systems. In contrast, axial heterostructures with Ge-QDs embedded in SiNW channel (*45*, *46*) hold a unique potential to combine the strengths of heterointerfacial and lateral size confinement to produce well-defined "natural" QDs, as depicted schematically in Fig. 1C. The type II band offset at the Si/Ge interfaces can help to confine the holes within the Ge segment, while the surrounding SiNW serving as high-quality epitaxial electrodes with triangle tunnel barriers. Despite of this advantageous quasi-1D heterostructure, no SHTs or single-electron transistors (SETs) have ever been demonstrated for the VLS-grown axial Si/Ge/Si heterostructures. A major reason for this is the lack of precise control over the location and orientation of VLS-grown NWs, which severely hinders reliable electrical connections and scalable device fabrication.

Recently, we have demonstrated that such hetero–Si/Ge/Si structure, with Ge island or QDs embedded in planar SiNWs can also be obtained (*47*, *48*), via an in-plane solid-liquid-solid (IPSLS) mechanism with the use of stacked amorphous Si (a-Si)/amorphous Ge (a-Ge) precursor layers (*49*–*51*). Although the IPSLS SiNWs can be guided to grow into orderly array, the positions of the Ge-QD formations within these SiNWs are still randomly distributed, thus posing a formidable challenge for achieving scalable fabrication of Ge-QD–based SHT devices.

In this work, we report a step-confined heteroprecursor supply (sc-HPS) strategy based on the IPSLS mechanism to achieve fully deterministic control over the positions and sizes of embedded Ge-QD islands. This was accomplished by obliquely cutting a predeposited SiO_2/a-Ge stack to expose Ge precursors exclusively at narrow a-Ge strips on the cutting step sidewalls, which are perpendicular to the growth direction of the SiNWs. Consequently, well-defined Ge-QD islands nucleate precisely at the cutting step edges, forming site-controlled axial SiNW/Ge-QD/SiNW heterostructures. These structures feature sharp Si/Ge interfaces with rapid compositional

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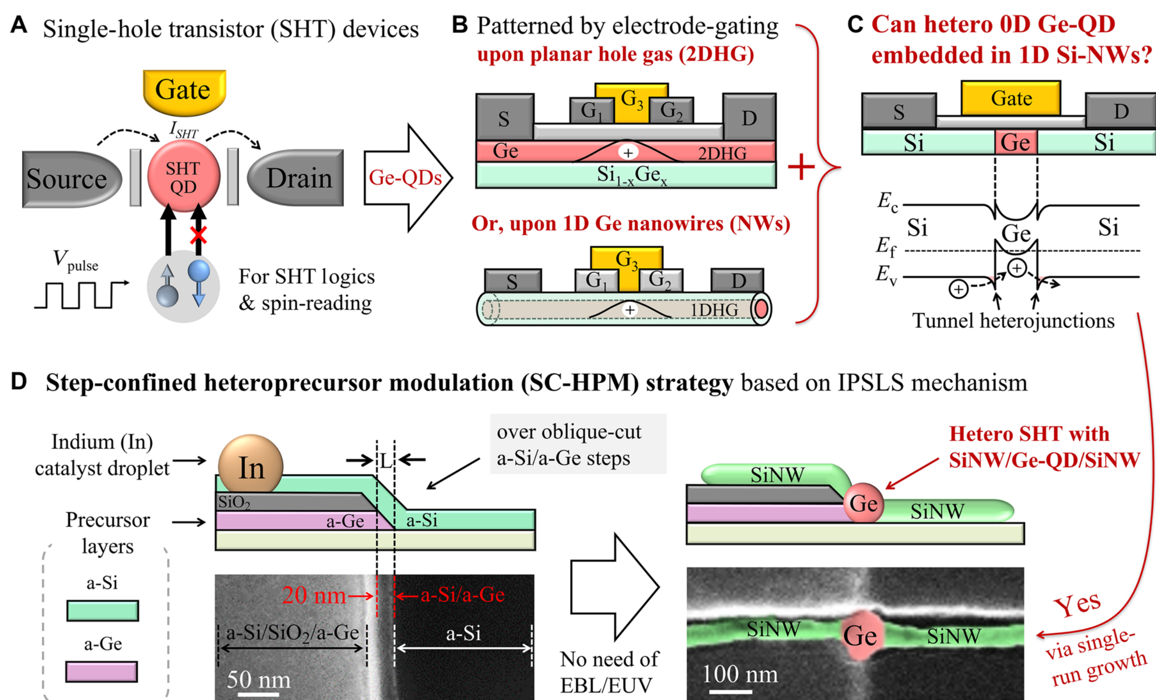

Fig. 1. Concepts and implementation routes for Ge-QD SHTs. (**A**) Logic operations and spin readout based on SHT devices. (**B**) Electrostatically confined Ge-QDs: in a Si/Ge heterostructure, multi-gates define QDs in a planar two-dimensional hole gas (2DHG) (top) and a NW one-dimensional hole gas (1DHG) (bottom). (**C**) Naturally confined 0D Ge-QD: The Si/Ge/Si band offset places the Ge valence-band edge above that of Si, creating two tunnel junctions at the interfaces and enabling a 0D QD without electrostatic confinement (band diagram). (**D**) The sc-HPS strategy based on the IPSLS mechanism. Oblique-cut steps define a sub–20 nm confined a-Si/a-Ge region, eliminating the need for high-resolution lithography [bottom: scanning electron microscopy (SEM) image]. Within this confined region, IPSLS growth yields a single Ge island embedded between SiNWs, forming a well-defined SiNW/Ge island/SiNW heterostructure (bottom: SEM image).

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transitions and strong interfacial band offsets that naturally confine individual holes within the Ge-QDs. The combined effects of strong heterointerfacial and size confinement enabled the direct fabrication of SHTs using these lithography-free Ge-QDs. The devices exhibited clear Coulomb oscillations and well-resolved Coulomb diamonds up to 50 K, demonstrating a CMOS-compatible, scalable approach for realizing single-charge logic devices, ultrasensitive sensors, and Si-based spin qubits.

RESULTS

Fabrication of site-controlled Ge-QDs via sc-HPS

Figure 2 (A to F) illustrates schematically the fabrication procedure of the Ge-QD islands, embedded in SiNW channels, by using the sc-HPS strategy. Specifically, this involves first the patterning of guiding steps on a Si wafer precoated with a SiO_2 layer through photolithography and subsequent etching to a depth of about 100 nm by using inductively coupled plasma (ICP) of C_4F_8 (Fig. 2A). Next, a SiO_2/a-Ge bilayer was deposited over the whole surface by plasma-enhanced chemical vapor deposition system (PECVD), followed by the patterning and deposition of indium (In) catalyst strips at the ends of the guiding steps (Fig. 2B). Thereafter, the SiO_2/a-Ge bilayer was cut/etched down to the substrate, at the locations prescribed for the later formation of Ge-QDs, with direction perpendicular to the guiding steps (Fig. 2C), by using a mixture of C_4F_8 and O_2 etching gases in ICP system. During this etching, the flow rate of O_2 was adjusted to control the slope of the resulting oblique step sidewall, and thus the width of the exposed a-Ge layer at the cutting edge. Subsequently, an H_2 plasma treatment was carried out in PECVD at 230°C to remove the oxide layer on the surface of In strips, and allow them to melt and merge into discrete catalyst droplets. Last, the substrate was cooled to frozen the In droplets at 100°C and covered by an a-Si layer of 10 nm thick. This leads to the formation of a narrow strip of a-Si/a-Ge bilayer exclusively at the exposed oblique cutting edges, as indicated in Fig. 2E, while in the other regions, a-Si layer is the only supply for the IPSLS growth. The spatially confined nature of this precursor supply configuration is first intuitively revealed in the SEM image of Fig. 1D, where the buried a-Ge layer is effectively isolated from the top a-Si layer by a continuous SiO_2 capping layer. This design ensures that, during subsequent heating, the In catalyst droplets can only access and absorb Ge at the exposed oblique cutting edges, while remaining completely unable to reach the a-Ge layer elsewhere.

To further verify this critical structural feature, we provide cross-sectional high-angle annular dark-field scanning transmission electron microscopy (HAADF-STEM) imaging of a focused ion beam (FIB)–prepared sample and energy-dispersive x-ray spectroscopy (EDS) analysis in fig. S1, which more clearly reveal the microscopic details of the precursor architecture; Ge elemental signals are strictly localized to the left side of the oblique edge, and the region above is fully encapsulated by a continuous SiO_2 layer. Moreover, the data confirm that the a-Si/a-Ge bilayer coexists exclusively along the oblique cutting plane. These high-resolution results not only directly validate the successful implementation of the "spatially confined

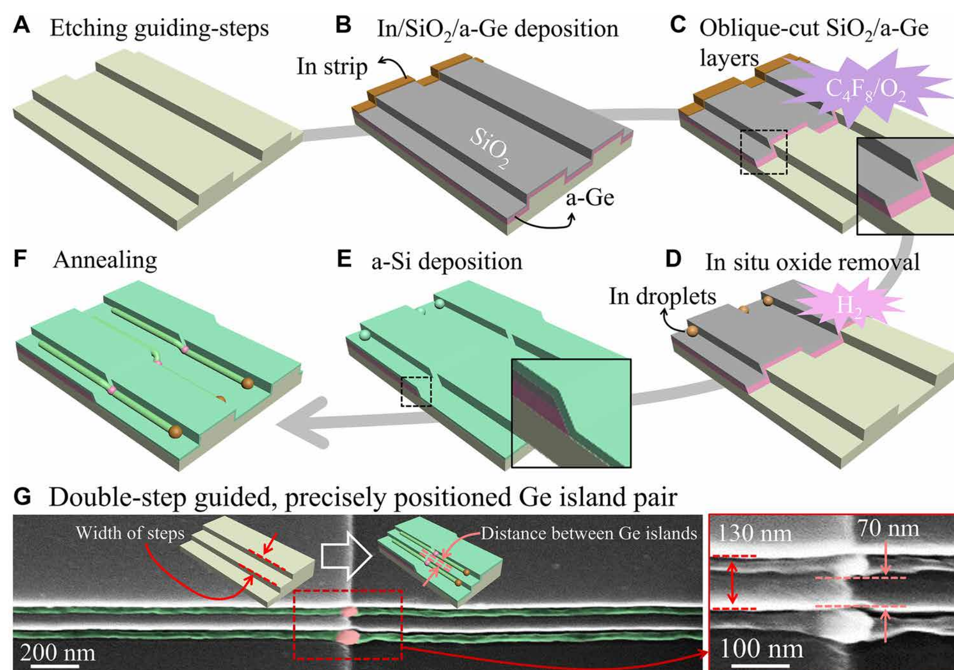

Fig. 2. Process flow of step-guided, precisely positioned Ge island growth based on oblique-cut precursors. (**A**) Formation of guiding steps by ICP etching. (**B**) Deposition of SiO_2/a-Ge bilayer and In catalyst strips. (**C**) Oblique cutting of the SiO_2/a-Ge stack with C_4F_8/O_2 plasma. (**D**) In situ oxide removal and droplet formation by H_2 plasma. (**E**) Deposition of the a-Si top layer. (**F**) IPSLS growth activated by annealing to form SiNW/Ge-QD/SiNW heterostructures. (**G**) SEM image of parallel SiNWs guided by double steps, each containing a precisely positioned Ge island (the inset shows a schematic of dual Ge islands grown on a dual-step substrate, while the right panel shows an enlarged SEM image of the Ge island pair).

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Ge source" design but also provide a solid structural foundation for the subsequent site-controlled and size-defined embedding of Ge-QDs within SiNWs.

To activate the IPSLS growth, the sample was annealed in the PECVD sample at a higher temperature at 350°C (Fig. 2F). This melts the In droplets again and allows them to consume the a-Si layer and produce crystalline SiNW along the guiding edges. When the In droplets came to grow over the narrow cutting edge region, with exposed a-Ge sidewall, the In droplets contacted and took in the buried a-Ge layer. As the solubility of Ge in In droplet is more than three orders of magnitude higher than that of Si ($C_{Ge_In}/C_{Si_In} > 10^3$) (*52*, *53*), the exposed a-Ge edge will be quickly absorbed into the In droplet to establish a supersaturation of Ge ingredient, followed by precipitation of c-Ge as granular QD island. When the exposed a-Ge edge layer was completely consumed, the In droplets will be limited by the capping SiO_2 layer that prevents the spreading of In to reach the buried a-Ge layer. So, the In droplet will continue to move on following the guiding edge and be refilled solely with the a-Si supply to produce pure but thinner SiNW segments, forming the lithography-free SiNW/Ge-QD/SiNW heterostructure with precise location control of the Ge-QD, as depicted in Fig. 1D. It should be emphasized that the term "lithography-free" pertains specifically to the formation and axial positioning of the Ge-QDs, which emerge self-aligned via the sc-HPS mechanism without the need for high-resolution patterning [e.g., electron-beam lithography (EBL) or extreme ultraviolet patterning]. While conventional photolithography may be used to define the initial step that guide NW growth, the QD dimensions and locations are intrinsically controlled by the oblique heterolayer design and catalyst dynamics, rendering nanoscale lithography unnecessary for QD integration.

While more experimental details and discussion of the IPSLS growth mechanism were provided in Materials and Methods and in our previous work (*47*, *48*), we would like to emphasize that this sc-HPM strategy can also be easily combined with other IPSLS growth control technologies, established in our previous works (*54*, *55*), to produce closely positioned QD pairs, as showcased for example in Fig. 2G, where a pair of closely spaced Ge-QDs were grown in two parallel SiNWs, separated only 70 nm apart (without using any sophisticated lithography), indicating the potential for achieving high-density array integration. Furthermore, thanks to its low-temperature operation (<350°C) and minimal substrate dependence, the sc-HPS strategy can potentially be extended to nonconventional substrates such as transparent glass or flexible polymers. Our prior work has already demonstrated the successful growth of ordered SiNW arrays via IPSLS on both glass and polyimide substrates (*56*–*58*), laying the foundation for future integration into flexible and transparent quantum electronic devices.

Structure and composition of SiNW/Ge-island/SiNW heterostructures

The morphology and composition of the SiNW/Ge-island/SiNW heterostructure were examined by STEM coupled with EDS. In Fig. 3A, a side-view STEM image of the heterostructure segment, prepared by FIB milling with a Pt protection layer deposited before thinning, and subsequently lift-out and transferred onto a Cu grid using a nanomanipulator, clearly reveals a distinctive Si/Ge heteroisland chain with pronounced diameter modulation along the NW. In addition to the NW structure, the SiO_2 isolation layer and the underlying a-Ge precursor layer are clearly visible, and the measured angle

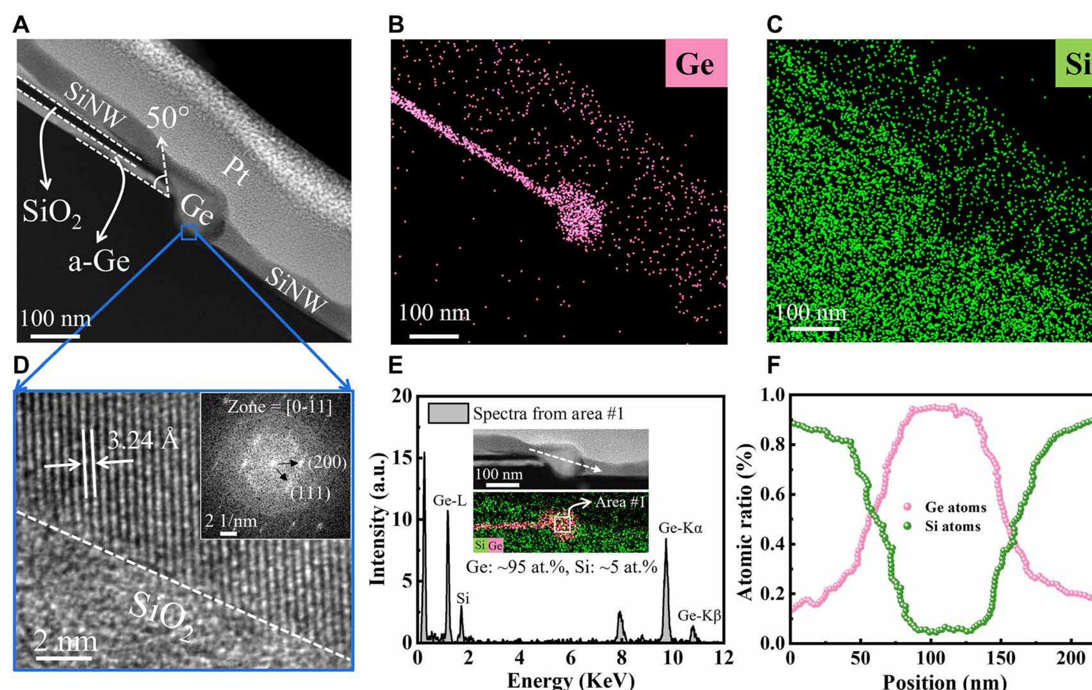

Fig. 3. Structural and compositional characterization of a precisely positioned Ge island in a SiNW. (**A**) STEM image showing a Ge island bridging two SiNWs. (**B** and **C**) EDS elemental maps for Ge (pink) and Si (green), clearly indicating the Ge island region. (**D**) HRTEM image of the Ge island, revealing a (111) lattice spacing of ~3.24 Å; inset: FFT diffraction pattern along the [0-11] zone axis. (**E**) EDS spectrum from the marked area #1 in the inset, showing Ge content of ~95 at % and Si content of ~5 at %. (**F**) Variation of Ge and Si atomic ratios along the white dashed arrow in the inset of (E), confirming a distinct compositional transition.

of the oblique cut is 50°. Figure 3 (B and C) presents the elemental maps, showing that the island is Ge-rich (pink), whereas the adjacent NW segments are Si-rich (green), consistent with selective Ge incorporation when the droplet traverses the oblique a-Si/a-Ge slope region.

The high-resolution TEM (HRTEM) image in Fig. 3D, acquired from the Ge-island region marked by the blue square in Fig. 3A, displays a lattice spacing of 3.24 Å corresponding to the Ge(111) plane; the inset shows the corresponding fast Fourier transform (FFT) indexed to the [0-11] zone axis. The EDS spectrum in Fig. 3E, collected from area #1 within the island (with the region of interest indicated in the inset), exhibits prominent Ge-L and Ge-Kα/Ge-Kβ peaks, together with a Si signal, yielding a composition of ~95 atomic % (at %) Ge and ~5 at % Si. Figure 3F presents a quantitative EDS line scan taken along the white dashed-arrow path indicated in Fig. 3E, showing anticorrelated atomic ratio profiles of Ge and Si, evidencing a sharp transition from Si-rich NW segments to the Ge-rich island and confirming the precise spatial control afforded by the obliquely cut a-Si/a-Ge precursor design.

Comprehensive cross-sectional structural analysis further reveals a fully coherent interface between the Ge-QD and the SiNW, with continuous lattice fringes, no detectable misfit dislocations, and an atomically sharp compositional transition spanning only ~3.5 nm. Geometric phase analysis confirms the absence of appreciable strain accumulation or shear distortion across the junction, indicating that the ~4.2% lattice mismatch is accommodated elastically without plastic relaxation, which is consistent with the strain-free nature of low-temperature IPSLS growth (*59*, *60*). These findings, detailed in figs. S2 to S4, demonstrate high-fidelity epitaxial integration and highlight the potential of this heterostructure for realizing well-defined quantum confinement.

Formation mechanisms and morphology control in SiNW/Ge-QD/SiNW heterostructures

Figure 4A illustrates more details of the hetero–a-Si/a-Ge precursor region, where a-Ge precursor is exposed only at the obliquely cut slope for the formation of Ge-QDs. Actually, the amount of a-Ge supply at this cutting slope can be approximated by the area of this triangle region, with

$$S_{\mathrm{a-Ge}} = \frac{1}{2}\tan\theta \cdot h_{\mathrm{a-Ge}}^{2} \quad (1)$$

where θ is the oblique angle of the slope and $h_{\text{a-Ge}}$ is the thickness of the buried a-Ge layer below the SiO_2 capping layer. Note that θ can be controlled by the O_2 flow rate during the ICP etching process, and was set to be θ ~ 50° in the following experiments. When an In droplet comes to grow over this step, it is the top a-Si layer that has to be first consumed, before the droplet contact and absorption of the underlying a-Ge layer. Otherwise, as seen for example in Fig. 4C, where the a-Si layer is relatively too thick of $h_{\text{a-Si}} > 15$ nm, and the In droplet grew over the hetero–a-Si/a-Ge stack slope without even touching the bottom a-Ge layer, thus leaving basically no Ge-QDs in the SiNWs, corresponding to the gray region of pure SiNW in Fig. 4B. Therefore, in the following parametric control experiments, the a-Si layer thickness was controlled to be <15 nm, that is, in the range of 7 to 14 nm, while all data were collected for the In droplet with similar In droplet diameter of $D_c \approx 100$ nm, so as to guarantee the eating-through of the <15-nm-thick top a-Si layer and exclude the influence of droplet size.

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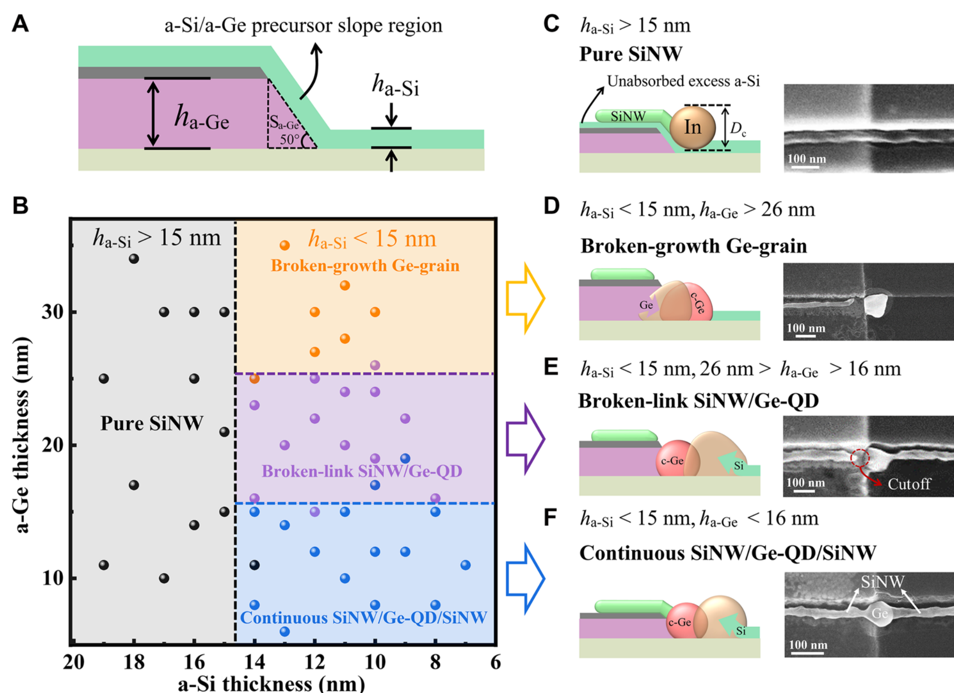

Fig. 4. Thickness window of the obliquely cut a-Si/a-Ge precursor slope region and the resulting morphologies. (**A**) Schematic of the precursor region and oblique-cut geometry (~50°), defining the effective thicknesses $h_{a\text{-}Ge}$ and $h_{a\text{-}Si}$. (**B**) Thickness-phase map (dots: experimental data): *x*-axis $h_{a\text{-}Si}$ and *y*-axis $h_{a\text{-}Ge}$. Regions correspond to (**C** to **F**): left gray, $h_{a\text{-}Si} > 15$ nm; top orange, $h_{a\text{-}Si} < 15$ nm and $h_{a\text{-}Ge} > 26$ nm; middle purple, $h_{a\text{-}Si} < 15$ nm and 26 nm $> h_{a\text{-}Ge} > 16$ nm; bottom blue, $h_{a\text{-}Si} < 15$ nm and $h_{a\text{-}Ge} < 16$ nm. (C) For $h_{a\text{-}Si} > 15$ nm, only pure SiNWs are obtained. [(D) to (F)] When $h_{a\text{-}Si} < 15$ nm, different morphologies appear with increasing $h_{a\text{-}Ge}$: broken-growth Ge-grain structure for $h_{a\text{-}Ge} > 26$ nm; broken-link SiNW/Ge-QD heterostructure for 26 nm $> h_{a\text{-}Ge} > 16$ nm; and continuous SiNW/Ge-QD/SiNW heterostructure for $h_{a\text{-}Ge} < 16$ nm. The schematics and SEM images on the right show representative morphologies for each regime.

To understand the impact of different a-Ge layer thicknesses on the formation of GeQDs and the overall connectivity of the NW/QD/NW heterostructure, a series of parametric investigations were carried out. There are three distinct geometries that have been observed, as summarized in Fig. 4B, and seen with corresponding SEM images in Fig. 4 (D and F).

First, for the very thick a-Ge layer $h_{a\text{-}Ge} > 26$ nm, the In droplet disappears after crossing the hetero–a-Si/a-Ge slope region, forming only a large c-Ge grain, as witnessed in Fig. 4D. This indicates that the In droplet can readily absorb the exposed a-Ge slope to precipitate c-Ge phase, and then preferentially drawn by the a-Ge/In interface to spread inward into the buried a-Ge layer. It is worthy to note that the solubility of Ge atoms in In at 350°C is $C_{Ge} \approx 2.4\%$ [corresponding to a volume fraction $\phi \approx 2$ volume % (vol %)] (*61*), which is much higher than that of 0.0032% for the Si ingredient in In droplet. Therefore, a-Ge layer will be absorbed by the In droplet at a much faster rate, and thus the In droplet will tend to squeeze into the underlying space below the SiO_2 capping layer. Whenever this happens, as allowed by a thick a-Ge layer thickness as observed for $h_{a\text{-}Ge} > 26$ nm, the integrity of the In droplet will be broken, and the catalyst In will tend to spread or mix with the buried a-Ge layer. Therefore, there is no further growth of the SiNW segment on the other hand of the large c-Ge grain (see in Fig. 4D).

Second, reducing the a-Ge layer thickness to 26 nm $> h_{a\text{-}Ge} > 16$ nm can indeed help to suppress spreading of the In droplet into the buried layer, as shown in Fig. 4E. This reasonable considering that the fact that squeezing a relatively large In droplet into a narrower space below the SiO_2 capping layer becomes more and more energetically unfavorable. However, the as-grown Ge-QDs are usually found to be disconnected to the incident SiNW branch, while being joint only by the outgoing one. Actually, similar phenomenon also existed for the growth of thicker a-Ge layer, as seen in Fig. 4D, which is undesired as it undermines the continuity of the NW/QD/NW heterostructure to serve as channel for SHT device. This ruptured growth also indicate that there was spontaneous nucleation of new c-Ge grain at the root of the heterostep that expanded quickly to push the droplet to detach from the rear deposition end of SiNW, as observed in the cut-off region in the SEM image of Fig. 4E. So, to guarantee a continuous growth, a heterogeneous epitaxy growth of GeQD at the rear SiNW end is desired, instead of spontaneous formation of new c-Ge nucleus at the root of step.

On the basis of a geometry consideration, the amount/or volume of the available Ge, exposed at the slope can be approximated by the produce of the diameter of droplet and the cross-section area, marked by the dashed triangle,

$$V_{a-Ge} = D_c \cdot S_{a-Ge} = \frac{D_c\, h^2_{a-Ge}}{2\tan\theta} \quad (2)$$

A complete absorption of this exposed Ge content into an In droplet with $V_c \sim D_c^3 \pi/6$ will establish a Ge concentration of

$$\phi^*_{Ge} \equiv \frac{V_{a-Ge}}{V_c} \quad (3)$$

which is just lower than the solubility of $\phi^*_{Ge} < \phi_{Ge} \sim 2$ vol % at 350°C. This critical condition guarantees that spontaneous nucleation of c-Ge will not happen randomly at the root of heterostep,

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which will otherwise lead to rupture of Ge-QD from the SiNW end. In this way, the dissolved Ge atoms will preferentially to attach to, and grow from, the rear heterogeneous deposition interface at the end of SiNW, to ensure the continuity of the NW/QD/NW channel structure.

Third, for the a-Ge layer thickness in the range of $h_{a-Ge} < h_{a-Ge}^{crit}$, a continuous growth of SiNW/Ge-QD/SiNW heterostructure, with pronounced island feature ($\frac{D_{QD}}{D_{NW}} \sim 2$), can be steadily obtained as showcased in Fig. 4F. Combining Eqs. 2 and 3, a critical a-Ge layer thickness can be estimated to be

$$h_{a-Ge}^{crit} = D_c \sqrt{\frac{\pi \tan\theta}{3} \phi_{Ge}} \sim 16 \text{ nm} \quad (4)$$

which agrees very well with the experimentally observation as showcased in Fig. 4B. Of course, with the decrease of the a-Ge layer thickness, the total amount of Ge content in the as-formed QD region will also drop, which will in turn reduce the band offset barriers required to confine holes in the QD islands. Therefore, it will be reasonable to seek a trade-off on the a-Ge layer thickness, to guarantee simultaneously the growth continuity in the NW/QD/NW structure, and a high enough Ge content for efficient QD confinement of SHT operation, as demonstrated in Fig. 3F.

It is essential to note that temperature has a decisive influence on the solubility of Ge and Si in the In catalyst, directly affecting supersaturation, nucleation kinetics, and ultimately, the size of the Ge-QD. Therefore, temperature defines the viable growth window for SiNW/Ge-QD/SiNW heterostructures. We fixed the growth temperature at 350°C to balance Si and Ge solubility, In droplet stability, and reaction kinetics, enabling reproducible formation of well-defined Ge-QDs within the SiNW channel.

Equation 4 also states that the critical a-Ge layer thickness is also proportional to the size of the leading In catalyst droplet. This also implicates that the diameter of this hetero-NW/QD/NW structure can be readily obtained over a wide range of diameter ranges, given a proper control of $h_{a-Ge} < h_{a-Ge}^{crit}$ to fall within the growth continuity window. For instances, Fig. 5 provides a statistic on the geometric scalability of the as-grown SiNW/Ge-QD/SiNW heterostructure, exhibiting linear scaling laws, with strong correlations of $R^2 = 0.97$ and 0.94 for the Ge-QDs and SiNW segments, respectively. Note that, the a-Ge layer thickness was adjusted from 4 to 25 nm, being proportional to the size of the leading In droplet. In addition, with the increase of the In droplet size, the embedded Ge-QDs become more prominent, with larger and larger $\frac{D_{QD}}{D_{NW}}$ diameter ratio that varies from 1.2 to 2.1. This can be attributed to two factors: First, the use of larger In droplets with thicker a-Ge buried layers increase the a-Ge/a-Si precursor supply ratio; second, the soft In droplets are still free to deform, drawn by the a-Ge/In interface, to touch and absorb nearby a-Ge layer. Larger droplets enjoy more freedom to spread out laterally to take in more a-Ge to form slightly larger Ge-QDs. Although a comprehensive understanding of this deformation/absorption dynamics is still lacking, probably demanding the aid of finite elemental simulation of the liquid droplet and deposition system, the geometry scaling capability observed here provides a key basis for the fabrication and optimization of the SHT devices.

Notably, in our sc-HPS approach, the combination of smaller In catalytic droplets and reduced a-Ge supply can, in principle, yield sub–20 nm Ge-QDs. The a-Ge supply is precisely tunable via the a-Ge layer thickness and the oblique-cut angle, which defines the spatially confined precursor feed at the step edge. Coupled with our previously developed edge-trimming catalyst formation strategy (*62*), the In droplet size can be accurately controlled by the width and thickness of narrow In stripes. Further integration with multistep edge architectures (*54*) or sidewall-confined trench structures (*63*) enables spatial confinement of the catalytic region, suppresses size fluctuations, and supports continued dimensional scaling. These techniques have already been validated for diameter scaling and uniform growth of SiNWs, demonstrating their feasibility for future Ge-QD miniaturization.

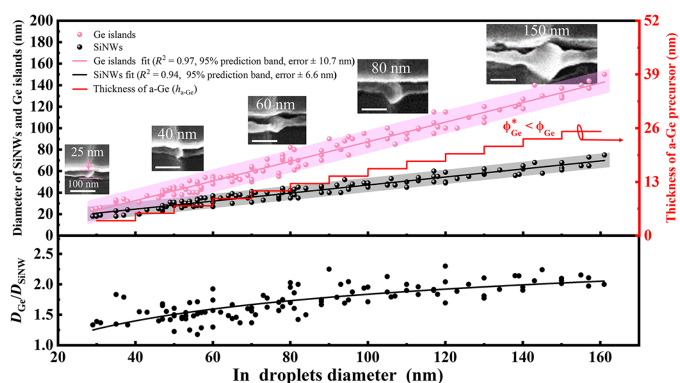

Fig. 5. Statistics of the scaling of Ge island diameters and SiNW diameters as a function of In droplet diameter. Pink dots represent Ge island diameters and black dots represent SiNW diameters, under the condition that the In droplet size and a-Ge thickness (red curve) satisfy $\phi_{Ge}^* < \phi_{Ge}$. The lower panel shows the evolution of the diameter ratio of D_{Ge}/D_{SiNW} with In droplet diameter.

Electrical performance of SiNW/Ge-QD/SiNW SHTs

On the basis of the precise control over size and structural continuity in the axial SiNW/Ge-QD/SiNW heterostructure, prototype SHT devices were fabricated, with an electric configuration as illustrated in Fig. 6A. This specific SHT device has a wider Ge-QD of ~30 nm in diameter, connected epitaxially by a pair of thinner SiNW segments with a diameter of ~20 nm. Pt/Au source (S) and drain (D) electrodes are patterned by using EBL, contacting the two SiNW segments on both sides. Note that there are still two serial SiNW connection segments between the edges of S/D pads to the central Ge-QD, which are of 300 and 600 nm, respectively. Then, A global Ti/Au top gate (G) electrode is fabricated that capacitively coupled to the SiNW/Ge-QD/SiNW channel through a 30-nm-thick Al_2O_3 dielectric layer. Figure 6B shows a 2D Silvaco simulation of the band profile of the channel structure, revealing a heteroconfinement region of holes in the valence-band-top realized in the Ge-QDs, bounded by a pair of hetero–band-offset interfaces and Schottky barriers extended into the SiNW segments. It is noteworthy that the Ge-QDs and the SiNW segments are both initially p-type doped, due to the incorporation of In catalyst atoms (*64*). While the In concentration in SiNWs has been verified in our previous works to be equivalently ~10^{17} cm^{-3}, it is supposed to two orders of magnitude higher in the Ge-QDs due to the higher solubility of In in c-Ge than that in c-Si (*65*).

According to the temperature-varied output characteristics (I_D-V_{DS}) shown in Fig. 6C, the SHT device exhibits nearly Ohmic contact at $V_{GS} = 0$ V at 300 K, while the transport currents decrease quickly and demonstrate more and more Schottky-like behavior with decreased temperature down to 50 K. Figure 6D shows the temperature evolution

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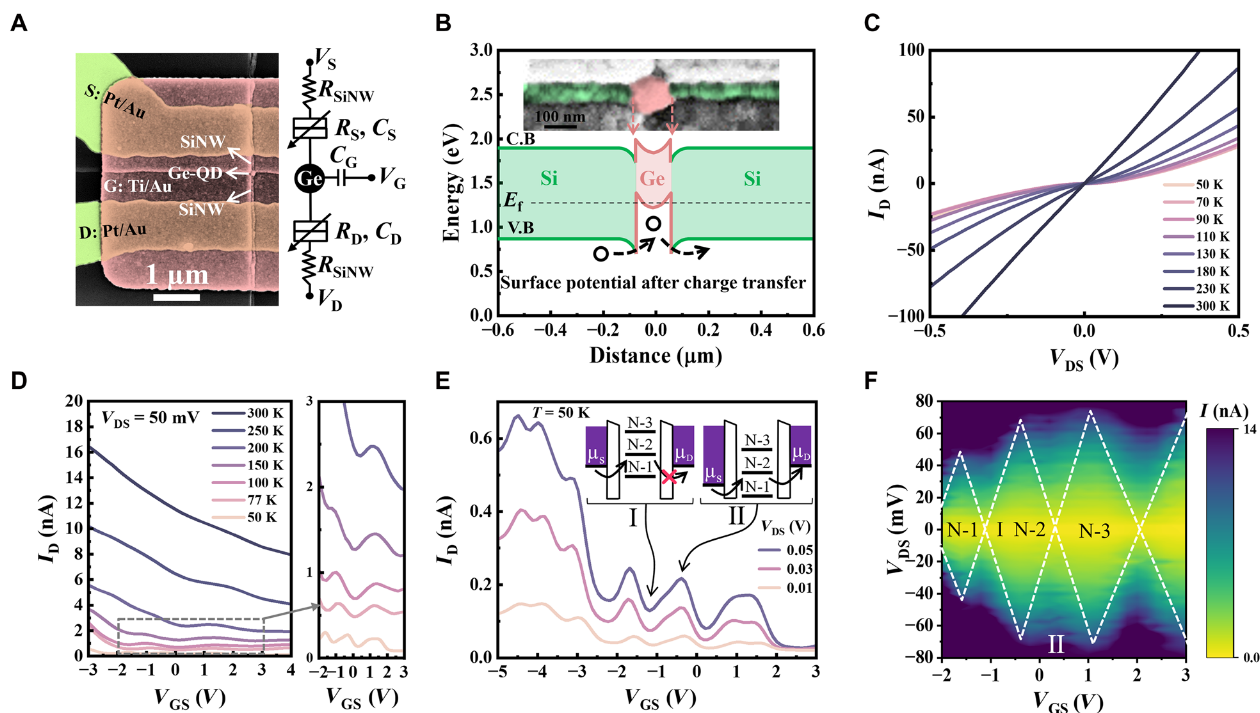

Fig. 6. Electrical transport properties of the SiNW/Ge-QD/SiNW SHT. (**A**) The equivalent circuit and false-color SEM image of the device. (**B**) Simulated band diagram of the SiNW/Ge island/SiNW heterostructure, showing the valence-band offset and Si/Ge interfacial barriers that confine holes within the Ge island. Inset: magnified SEM image of the Ge island. (**C** and **D**) Temperature-dependent measurements reveal a transition from single-hole tunneling at low temperatures to thermally activated Ohmic transport at higher temperatures, with Coulomb oscillations gradually suppressed. (**E**) The transfer characteristics exhibiting periodic Coulomb oscillations at 50 K. (**F**) Stability diagram showing well-defined Coulomb diamonds, confirming quantum SHT operation through the confined Ge island.

of the transfer behaviors of the SHT device measured under V_{DS} = 50 mV, where clear current oscillations are gradually revealed when temperature decreases to <150 K, particularly in the region of −2 V < V_{GS} < 3 V, also enlarged for the ease of observation in the right panel. More details of these peaky current oscillation curves measured at 50 K are provided in Fig. 6E, where amplitude of the Coulomb oscillations increases with higher channel bias from V_{DS} = 0.01 to 0.05 V. According to the diagrams sketched in the onsets of Fig. 6E, each conductance peak corresponds to the resonant transport condition with the alignment of the injecting valence band-top (V_{BT}) level in the SiNW electrodes with the discrete charging energy levels in the Ge-QD. On the contrary, the current dip or valley regions indicate the blockage of the transport holes through the Ge-QD due to the discrete additional charge energy (E_c) spacing and the energy level misalignment. This distinctive conducting/charging behavior can be better seen in the charge stability diagram of I_D (V_{GS}, V_{DS}) in Fig. 6F, where well-defined Coulomb blockade diamonds are resolved with the white dashed lines that delimiting the different charge-loading states in the Ge-QD. This distinctive conductive/charging behavior is more clearly observed in the charge stability diagram of I_D as a function of V_{GS} and V_{DS} shown in Fig. 6F, where well-defined Coulomb blockade diamonds are resolved. The white dashed lines delineate the boundaries between different charge states in the Ge-QD. Note that, within the current-forbidden diamonds in region I, the labeled N-1, N-2, and N-3 blocks correspond to the successive charging/or discharging of individual hole carriers in/or from the Ge-QD. The transport current is only permitted outside the diamond blocks in the darker region II, while the horizontal V_{GS} separation of the neighbored diamonds in region I corresponds to the adjacent current peaks in Fig. 6E. In comparison, the reference device fabricated with pure SiNW channel, but without Ge-QD island (see fig. S5) exhibits only linear I_D-V_{DS} relationship, without any peaky oscillation. These observations combined indicate that the observed current oscillation characteristics and the unique transport current patterns originate from the Coulomb charging/discharging behavior of holes in the confined Ge-QD.

It is also important to note that, the Coulomb diamond patterns observed here exhibit somehow distortions, in comparison to the SETs or SHTs with ideal Ohmic contacts (*66*). This is because of the extra serial resistances introduced by the two connecting SiNW electrode segments, as seen and indicated for example in the SEM image in Fig. 6A. Actually, because of the incorporation of catalytic In atoms, the SiNW segments are of p-type doped, and thus the serial resistances are also modulated by the top gating, while a portion of the applied V_{GS} and V_{DS} will be dropped over the SiNW segments. More specifically, Fig. 6E and fig. S5B show that both the heterostructure NW/QD/NW device, and the reference device with pure SiNW, display increasing transport currents at larger negative gating bias of V_{GS}, which is assigned to the hole accumulation in the p-type SiNW electrodes that make them more conductive. Conversely, the SiNW segments become more resistive under positive V_{GS}. This gating-induced serial resistance variation in SiNW segments also causes the somehow asymmetric distortion in the charge-state diamonds. For instance, in the positive V_{GS} regime, a larger fraction of the applied gate bias is dropped across the SiNW segments, resulting in elongated Coulomb diamonds. The opposite situation occurs at negative V_{GS} that leads to gradually compressed diamond patterns.

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Nevertheless, the charging energy can still be extracted or estimated based on a simplified electric model (as seen in Fig. 6A), by taking into account the voltage division effect of the terminal resistances of SiNW-connected SHT. First, the total serial resistance and their voltage dropping factors were estimated by comparing the transport characteristics of the SiNW FET devices with or without Ge-QDs, both measured at 50 K (see Fig. 6C and fig. S5A). On the basis of a voltage-division factor across the Ge-QD junction of $\eta \approx 0.2$, the measured diamond span $\Delta V_{DS}^{dia} \approx 0.14$ V corresponds to a charging energy of $E_c^{(A)} \approx e(\eta\, \Delta V_{DS}^{dia})/2 \approx 14$ meV. The gate capacitance is estimated from the Coulomb-oscillation period $\Delta V_{GS} \approx 1.2$ V as $C_G = e/\Delta V_{GS} \approx 0.13$ aF, while on the basis of the internal diamond-edge slope of $|S_{\pm}|$ (*67*) and $C_S \approx C_D \approx C_G/(|S_{\pm}|) \approx 5.56$ aF, the total capacitance and the gate-coupling factor are calculated to be $C_{\Sigma} = C_S + C_D + C_G \approx 11.26$ aF and $\alpha_G = C_G/C_{\Sigma} \approx 1.2\%$, respectively. This leads to a charging energy of $E_c^{(B)} = e^2/C_{\Sigma} \approx 14.23$ meV that agrees very well with the experimentally extracted $E_c^{(A)}$. It is noteworthy that this single-run grown SiNW/Ge-QD/SiNW heterostructure alone can provide strong enough spatial/heterointerface confinement in the deterministically site-controlled QD islands to demonstrate robust and high-temperature single-hole charge operation, as inferred from the well-defined Coulomb diamonds at 50 K. In addition, we present a systematic characterization of 11 additional SHTs fabricated via the lithography-free sc-HPS method, covering a wide range of SiNW/Ge-QD/SiNW dimensional combinations and measurement temperatures (see the Supplementary Materials for details).

In view of further improvements, a more advanced gate-all-around (GAA) gating configuration, together with thinner and better tuned higher-*k* dielectrics, could be adopted to improve the electrostatic coupling of α_G. Such GAA-FETs (*54*) have already been successfully fabricated based on the IPSLS-grown SiNW channels, and the channel releasing and fabrication techniques are also applicable to the SiNW/Ge-QD channel structures. On the other hand, to mitigate the bias partition and series resistance arising from semiconducting SiNW source/drain leads, the SiNWs can be grown with predoped a-Si precursor to achieve p+ or n+ doping in the SiNWs (*68*, *69*) or alloyed into more conductive silicide (*70*, *71*). Both approaches are fully compatible with the SHT fabrication and will help to reduce the voltage division, strengthen gate coupling to the Ge-QD, and lower access/series resistance. All these aspects will be explored systematically in our future work to achieve more reliable single charge operations and high-performance SHT logics for the construction and integration of more effective and scalable SiNW/Ge-QD based quantum sensing or computing applications.

Moreover, the sc-HPS strategy is not limited to Ge-QDs in SiNWs. Because the obliquely cut heterolayer confines precursor supply at the step, the strategy can selectively embed a second component into quasi-1D channels in other materials. For example, replacing the top a-Si layer with a-SiGe enables construction of SiGeNW/Ge-QD/SiGeNW axial heterostructures, while reversing the deposition order of a-Ge and a-Si is expected to yield GeNW/Si-QD/GeNW heterostructures. We have already demonstrated, within the IPSLS growth framework, composition-uniform SiGeNWs with precise Si/Ge ratio control (*60*), and, by using a lower growth temperature (200°C) together with a thinner a-Ge precursor (3 to 5 nm), we have successfully realized pure GeNWs. These results provide an experimental foundation for extending the sc-HPS approach to broader material systems.

DISCUSSION

In summary, we have proposed and demonstrated an sc-HPS strategy to deterministically fabricate SiNW/Ge-island/SiNW heterostructures in a single-run growth process, thereby eliminating the need for high-resolution lithography. Structural characterization by TEM and EDS confirmed the formation of compositionally sharp Ge-rich islands (~95 at % Ge) embedded within SiNWs, with well-defined Si/Ge interfaces. Low-temperature transport measurements on SHTs fabricated from these heterostructures revealed pronounced Coulomb blockade oscillations and well-defined Coulomb diamonds. Control experiments and temperature-dependent measurements further excluded parasitic effects, confirming robust single-hole confinement in the Ge islands. This lithography-friendly and CMOS-compatible approach not only provides a scalable route for precise position- and size-controlled Ge-QDs but also validates their functionality as stable single-hole quantum devices. The ability to engineer interisland spacing and dimensional uniformity across arrays opens opportunities for scalable implementations in single-hole sensing and spin-based quantum information processing.

MATERALS AND METHODS

Confined precursor and catalyst metal preparation

To begin with, Si wafers coated with a 500-nm-thick SiO_2 layer were sequentially cleaned in acetone, ethanol, and deionized water to remove organic and particulate contaminants. Subsequently, guiding steps were patterned by photolithography and etched to a depth of 100 nm using C_4F_8 plasma. By repeating the sequence of C_4F_8 plasma etching of SiO_2 and O_2 plasma lateral etching of the photoresist *n* times, multistep guiding platforms with inclined sidewalls were formed, providing well-defined step edges for later growth. Following this, a SiO_2/a-Ge bilayer was deposited at 100°C by PECVD: The a-Ge layer was grown using 5 standard cubic centimeter per minute (sccm) of 5% GeH_4 in 95% H_2 at a chamber pressure of 20 Pa and RF power of 10 W, while the SiO_2 barrier layer (15 nm thick) was deposited from 80 sccm SiH_4, 120 sccm N_2O, and 40 sccm N_2 at 100 Pa and 15 W RF power. In parallel, an 8-nm-thick In strip was defined at one end of each guiding step through photolithography, thermal evaporation, and lift-off, serving as the catalyst source. To further tailor the precursor geometry, the SiO_2/a-Ge stack was patterned perpendicular to the guiding steps and etched down to the substrate using C_4F_8/O_2 plasma, while lateral etching of the photoresist by O_2 plasma generated slope region with tunable widths.

SiNW/Ge-QD/SiNW heterostructure growth

Building on this precursor and catalyst architecture, the sample was first treated in a PECVD system at 230°C with 50 sccm H_2 at 130 Pa and 35 W RF power for 10 min. This step effectively removed native oxides from both In and Ge, while simultaneously melting and agglomerating the In strips into well-defined catalyst droplets. Next, an a-Si layer was deposited at 100°C using 5 sccm SiH_4 at 20 Pa and 1 W RF power, thereby forming a confined a-Si/a-Ge bilayer (~20 nm wide) along the edge region, whereas other regions were only covered by a-Si. Last, the substrate was annealed at 350°C for 1 hour in vacuum. During this process, the In droplets moved along the guiding steps and sequentially catalyzed the formation of the SiNW/Ge island/SiNW heterostructure via the IPSLS growth mechanism.

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Characterization of SiNW/Ge-QD/SiNW heterostructure

SiNW/Ge-QD/SiNW heterostructure structural characterization was performed using a SEM (SIGMA HV-0369). TEM and EDS characterizations were carried out on a high-resolution, double-aberration–corrected transmission electron microscope (Titan Cubed G2 60–300), and the TEM specimens were prepared using a FIB (Thermo Fisher Scientific Helios G4 CX).

Fabrication of SHTs

First, the source and drain electrode patterns were defined on the SiNWs at both sides of the Ge island by EBL. Then, the sample was dipped in a 4 weight % HF solution for 2 s before metal deposition to remove the native oxide on the SiNW surface. After that, 10/50 nm Pt/Au metal electrodes were deposited by electron-beam evaporation (EBE), and the metal lift-off was subsequently performed using a 70°C water bath. Next, the sample was placed in a plasma-enhanced atomic layer deposition system to deposit a 30-nm Al_2O_3 layer. Last, the gate region on top of the Ge island was defined by photolithography, followed by the deposition of a 20/60-nm Ti/Au gate electrode using EBE.

Electrical measurements

The *I-V* characteristics and transfer characteristics of the SiNW/Ge-QD/SiNW SHTs were measured using a Keithley 2636B source meter on a low-temperature platform (Lakeshore).

Simulation

Silvaco-TCAD was used to model the physical behavior of the SiNW/Ge-QD/SiNW heterostructure, and the corresponding band structure was obtained from the structure files generated by the device simulations.

Supplementary Materials

This PDF file includes:
Supplementary Text
Figs. S1 to S8

REFERENCES

1. R. Hanson, L. P. Kouwenhoven, J. R. Petta, S. Tarucha, L. M. K. Vandersypen, Spins in few-electron quantum dots. *Rev. Mod. Phys.* **79**, 1217–1265 (2007).
2. G. Burkard, T. D. Ladd, A. Pan, J. M. Nichol, J. R. Petta, Semiconductor spin qubits. *Rev. Mod. Phys.* **95**, 025003 (2023).
3. Y. He, S. K. Gorman, D. Keith, L. Kranz, J. G. Keizer, M. Y. Simmons, A two-qubit gate between phosphorus donor electrons in silicon. *Nature* **571**, 371–375 (2019).
4. J. R. Petta, A. C. Johnson, J. M. Taylor, E. A. Laird, A. Yacoby, M. D. Lukin, C. M. Marcus, M. P. Hanson, A. C. Gossard, Coherent manipulation of coupled electron spins in semiconductor quantum dots. *Science* **309**, 2180–2184 (2005).
5. J. Medford, J. Beil, J. M. Taylor, S. D. Bartlett, A. C. Doherty, E. I. Rashba, D. P. DiVincenzo, H. Lu, A. C. Gossard, C. M. Marcus, Self-consistent measurement and state tomography of an exchange-only spin qubit. *Nat. Nanotechnol.* **8**, 654–659 (2013).
6. G. Scappucci, C. Kloeffel, F. A. Zwanenburg, D. Loss, M. Myronov, J.-J. Zhang, S. De Franceschi, G. Katsaros, M. Veldhorst, The germanium quantum information route. *Nat. Rev. Mater.* **6**, 926–943 (2021).
7. C.-A. Wang, V. John, H. Tidjani, C. X. Yu, A. S. Ivlev, C. Déprez, F. van Riggelen-Doelman, B. D. Woods, N. W. Hendrickx, W. I. L. Lawrie, L. E. A. Stehouwer, S. D. Oosterhout, A. Sammak, M. Friesen, G. Scappucci, S. L. de Snoo, M. Rimbach-Russ, F. Borsoi, M. Veldhorst, Operating semiconductor quantum processors with hopping spins. *Science* **385**, 447–452 (2024).
8. D. Loss, D. P. DiVincenzo, Quantum computation with quantum dots. *Phys. Rev. A* **57**, 120–126 (1998).
9. A. Y. Kitaev, Unpaired Majorana fermions in quantum wires. *Phys. Usp.* **44**, 131–136 (2001).
10. T. W. Larsen, K. D. Petersson, F. Kuemmeth, T. S. Jespersen, P. Krogstrup, J. Nygård, C. M. Marcus, Semiconductor-nanowire-based superconducting qubit. *Phys. Rev. Lett.* **115**, 127001 (2015).
11. D. V. Bulaev, D. Loss, Spin relaxation and decoherence of holes in quantum dots. *Phys. Rev. Lett.* **95**, 076805 (2005).
12. M. Lodari, A. Tosato, D. Sabbagh, M. A. Schubert, G. Capellini, A. Sammak, M. Veldhorst, G. Scappucci, Light effective hole mass in undoped Ge/SiGe quantum wells. *Phys. Rev. B* **100**, 041304 (2019).
13. R. Pillarisetty, N. Thomas, H. C. George, K. Singh, J. Roberts, L. Lampert, P. Amin, T. F. Watson, G. Zheng, J. Torres, M. Metz, R. Kotlyar, P. Keys, J. M. Boter, J. P. Dehollain, G. Droulers, G. Eenink, R. Li, L. Massa, D. Sabbagh, N. Samkharadze, C. Volk, B. P. Wuetz, A. M. Zwerver, M. Veldhorst, G. Scappucci, L. M. K. Vandersypen, J. S. Clarke, in *2018 IEEE International Electron Devices Meeting (IEDM)*, (2018), pp. 6.3.1–6.3.4.
14. Z. Sadre Momtaz, S. Servino, V. Demontis, V. Zannier, D. Ercolani, F. Rossi, F. Rossella, L. Sorba, F. Beltram, S. Roddaro, Orbital tuning of tunnel coupling in InAs/InP nanowire quantum dots. *Nano Lett.* **20**, 1693–1699 (2020).
15. M. Asgari, D. Coquillat, G. Menichetti, V. Zannier, N. Diakonova, W. Knap, L. Sorba, L. Viti, M. S. Vitiello, Quantum-dot single-electron transistors as thermoelectric quantum detectors at terahertz frequencies. *Nano Lett.* **21**, 8587–8594 (2021).
16. L. A. Terrazos, E. Marcellina, Z. Wang, S. N. Coppersmith, M. Friesen, A. R. Hamilton, X. Hu, B. Koiller, A. L. Saraiva, D. Culcer, R. B. Capaz, Theory of hole-spin qubits in strained germanium quantum dots. *Phys. Rev. B* **103**, 125201 (2021).
17. F. P. García de Arquer, D. V. Talapin, V. I. Klimov, Y. Arakawa, M. Bayer, E. H. Sargent, Semiconductor quantum dots: Technological progress and future challenges. *Science* **373**, eaaz8541 (2021).
18. S. Conti, S. Saberi-Pouya, A. Perali, M. Virgilio, F. M. Peeters, A. R. Hamilton, G. Scappucci, D. Neilson, Electron–hole superfluidity in strained Si/Ge type II heterojunctions. *NPJ Quantum Mater.* **6**, 41 (2021).
19. S. Friedrich, High-mobility Si and Ge structures. *Semicond. Sci. Technol.* **12**, 1515 (1997).
20. M. L. Lee, E. A. Fitzgerald, M. T. Bulsara, M. T. Currie, A. Lochtefeld, Strained Si, SiGe, and Ge channels for high-mobility metal-oxide-semiconductor field-effect transistors. *J. Appl. Phys.* **97**, 011101 (2004).
21. M. Virgilio, G. Grosso, Type-I alignment and direct fundamental gap in SiGe based heterostructures. *J. Phys. Condens. Matter* **18**, 1021–1031 (2006).
22. T. Huckemann, P. Muster, W. Langheinrich, V. Brackmann, M. Friedrich, N. D. Komerički, L. K. Diebel, V. Stieß, D. Bougeard, Y. Yamamoto, F. Reichmann, M. H. Zoellner, C. Dahl, L. R. Schreiber, H. Bluhm, Industrially fabricated single-electron quantum dots in Si/Si—Ge heterostructures. *IEEE Electron Device Lett.* **46**, 868–871 (2025).
23. K.-P. Gradwohl, L. Cvitkovich, C.-H. Lu, S. Koelling, M. Oezkent, Y. Liu, D. Waldhör, T. Grasser, Y.-M. Niquet, M. Albrecht, C. Richter, O. Moutanabbir, J. Martin, Enhanced nanoscale Ge concentration oscillations in Si/SiGe quantum well through controlled segregation. *Nano Lett.* **25**, 4204–4210 (2025).
24. N. W. Hendrickx, W. I. L. Lawrie, M. Russ, F. van Riggelen, S. L. de Snoo, R. N. Schouten, A. Sammak, G. Scappucci, M. Veldhorst, A four-qubit germanium quantum processor. *Nature* **591**, 580–585 (2021).
25. N. W. Hendrickx, D. P. Franke, A. Sammak, G. Scappucci, M. Veldhorst, Fast two-qubit logic with holes in germanium. *Nature* **577**, 487–491 (2020).
26. T. McJunkin, B. Harpt, Y. Feng, M. P. Losert, R. Rahman, J. P. Dodson, M. A. Wolfe, D. E. Savage, M. G. Lagally, S. N. Coppersmith, M. Friesen, R. Joynt, M. A. Eriksson, SiGe quantum wells with oscillating Ge concentrations for quantum dot qubits. *Nat. Commun.* **13**, 7777 (2022).
27. B. Paquelet Wuetz, M. P. Losert, S. Koelling, L. E. A. Stehouwer, A.-M. J. Zwerver, S. G. J. Philips, M. T. Mądzik, X. Xue, G. Zheng, M. Lodari, S. V. Amitonov, N. Samkharadze, A. Sammak, L. M. K. Vandersypen, R. Rahman, S. N. Coppersmith, O. Moutanabbir, M. Friesen, G. Scappucci, Atomic fluctuations lifting the energy degeneracy in Si/SiGe quantum dots. *Nat. Commun.* **13**, 7730 (2022).
28. N. W. Hendrickx, D. P. Franke, A. Sammak, M. Kouwenhoven, D. Sabbagh, L. Yeoh, R. Li, M. L. V. Tagliaferri, M. Virgilio, G. Capellini, G. Scappucci, M. Veldhorst, Gate-controlled quantum dots and superconductivity in planar germanium. *Nat. Commun.* **9**, 2835 (2018).
29. L. E. A. Stehouwer, C. X. Yu, B. van Straaten, A. Tosato, V. John, D. Degli Esposti, A. Elsayed, D. Costa, S. D. Oosterhout, N. W. Hendrickx, M. Veldhorst, F. Borsoi, G. Scappucci, Exploiting strained epitaxial germanium for scaling low-noise spin qubits at the micrometre scale. *Nat. Mater.* **24**, 1906–1912 (2025).
30. T. McJunkin, E. R. MacQuarrie, L. Tom, S. F. Neyens, J. P. Dodson, B. Thorgrimsson, J. Corrigan, H. E. Ercan, D. E. Savage, M. G. Lagally, R. Joynt, S. N. Coppersmith, M. Friesen, M. A. Eriksson, Valley splittings in Si/SiGe quantum dots with a germanium spike in the silicon well. *Phys. Rev. B* **104**, 085406 (2021).
31. F. Gao, J.-H. Wang, H. Watzinger, H. Hu, M. J. Rančić, J.-Y. Zhang, T. Wang, Y. Yao, G.-L. Wang, J. Kukučka, L. Vukušić, C. Kloeffel, D. Loss, F. Liu, G. Katsaros, J.-J. Zhang, Site-controlled uniform Ge/Si hut wires with electrically tunable spin–orbit coupling. *Adv. Mater.* **32**, e1906523 (2020).
32. H. Watzinger, J. Kukučka, L. Vukušić, F. Gao, T. Wang, F. Schäffler, J.-J. Zhang, G. Katsaros, A germanium hole spin qubit. *Nat. Commun.* **9**, 3902 (2018).
33. G. Katsaros, P. Spathis, M. Stoffel, F. Fournel, M. Mongillo, V. Bouchiat, F. Lefloch, A. Rastelli, O. G. Schmidt, S. De Franceschi, Hybrid superconductor–semiconductor devices made from self-assembled SiGe nanocrystals on silicon. *Nat. Nanotechnol.* **5**, 458–464 (2010).

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34. L. Du, D. Scopece, G. Springholz, F. Schäffler, G. Chen, Self-assembled in-plane Ge nanowires on rib-patterned Si (1 1 10) templates. *Phys. Rev. B* **90**, 075308 (2014).
35. J. J. Zhang, G. Katsaros, F. Montalenti, D. Scopece, R. O. Rezaev, C. Mickel, B. Rellinghaus, L. Miglio, S. De Franceschi, A. Rastelli, O. G. Schmidt, Monolithic growth of ultrathin Ge nanowires on Si(001). *Phys. Rev. Lett.* **109**, 085502 (2012).
36. G. Katsaros, J. Tersoff, M. Stoffel, A. Rastelli, P. Acosta-Diaz, G. S. Kar, G. Costantini, O. G. Schmidt, K. Kern, Positioning of strained islands by interaction with surface nanogrooves. *Phys. Rev. Lett.* **101**, 096103 (2008).
37. H. Watzinger, C. Kloeffel, L. Vukušić, M. D. Rossell, V. Sessi, J. Kukučka, R. Kirchschlager, E. Lausecker, A. Truhlar, M. Glaser, A. Rastelli, A. Fuhrer, D. Loss, G. Katsaros, Heavy-hole states in germanium hut wires. *Nano Lett.* **16**, 6879–6885 (2016).
38. N. Ares, V. N. Golovach, G. Katsaros, M. Stoffel, F. Fournel, L. I. Glazman, O. G. Schmidt, S. De Franceschi, Nature of tunable hole *g* factors in quantum dots. *Phys. Rev. Lett.* **110**, 046602 (2013).
39. W. Lu, J. Xiang, B. P. Timko, Y. Wu, C. M. Lieber, One-dimensional hole gas in germanium/silicon nanowire heterostructures. *Proc. Natl. Acad. Sci. U.S.A.* **102**, 10046–10051 (2005).
40. M. Brauns, J. Ridderbos, A. Li, E. P. A. M. Bakkers, F. A. Zwanenburg, Electric-field dependent *g*-factor anisotropy in Ge-Si core-shell nanowire quantum dots. *Phys. Rev. B* **93**, 121408 (2016).
41. A. P. Higginbotham, T. W. Larsen, J. Yao, H. Yan, C. M. Lieber, C. M. Marcus, F. Kuemmeth, Hole spin coherence in a Ge/Si heterostructure nanowire. *Nano Lett.* **14**, 3582–3586 (2014).
42. Y. Hu, F. Kuemmeth, C. M. Lieber, C. M. Marcus, Hole spin relaxation in Ge–Si core–shell nanowire qubits. *Nat. Nanotechnol.* **7**, 47–50 (2012).
43. Y. Hu, H. O. H. Churchill, D. J. Reilly, J. Xiang, C. M. Lieber, C. M. Marcus, A Ge/Si heterostructure nanowire-based double quantum dot with integrated charge sensor. *Nat. Nanotechnol.* **2**, 622–625 (2007).
44. S. P. Ramanandan, A. Morelle, M. Masseroni, S. Ben-David, S. Martí-Sánchez, V. Boureau, A. Rudra, T. Ihn, J. Arbiol, W. C. Carter, K. Ensslin, A. Fontcuberta i Morral, Gate-tunable hole transport in in-plane ge nanowires by V-groove confined selective epitaxy. *Adv. Funct. Mater.* **35**, 2423734 (2025).
45. Y. Wu, R. Fan, P. Yang, Block-by-block growth of single-crystalline Si/SiGe superlattice nanowires. *Nano Lett.* **2**, 83–86 (2002).
46. B. Eisenhawer, V. Sivakov, A. Berger, S. Christiansen, Growth of axial SiGe heterostructures in nanowires using pulsed laser deposition. *Nanotechnology* **22**, 305604 (2011).
47. Y. Zhao, H. Ma, T. Dong, J. Wang, L. Yu, J. Xu, Y. Shi, K. Chen, P. Roca i Cabarrocas, Nanodroplet hydrodynamic transformation of uniform amorphous bilayer into highly modulated Ge/Si island-chains. *Nano Lett.* **18**, 6931–6940 (2018).
48. X. Gan, J. An, J. Wang, Z. Liu, J. Xu, Y. Shi, K. Chen, L. Yu, Self-oscillated growth formation of standing ultrathin nanosheets out of uniform Ge/Si superlattice nanowires. *Chin. Phys. Lett.* **40**, 066101 (2023).
49. L. Yu, P.-J. Alet, G. Picardi, P. Roca i Cabarrocas, An in-plane solid-liquid-solid growth mode for self-avoiding lateral silicon nanowires. *Phys. Rev. Lett.* **102**, 125501 (2009).
50. L. Wu, Z. Hu, L. Liang, R. Hu, J. Wang, L. Yu, Step-necking growth of silicon nanowire channels for high performance field effect transistors. *Nat. Commun.* **16**, 965 (2025).
51. J. Yan, Y. Zhang, Z. Liu, J. Wang, J. Xu, L. Yu, Ultracompact single-nanowire-morphed grippers driven by vectorial Lorentz forces for dexterous robotic manipulations. *Nat. Commun.* **14**, 3786 (2023).
52. C. D. Thurmond, Equilibrium thermochemistry of solid and liquid alloys of germanium and of silicon. I. The solubility of Ge and Si in elements of groups III, IV and V. *J. Phys. Chem.* **57**, 827–830 (1953).
53. J. Kühnle, R. B. Bergmann, J. H. Werner, Role of critical size of nuclei for liquid-phase epitaxy on polycrystalline Si films. *J. Cryst. Growth* **173**, 62–68 (1997).
54. W. Liao, W. Qian, J. An, L. Liang, Z. Hu, J. Wang, L. Yu, High-performance gate-all-around field effect transistors based on orderly arrays of catalytic Si nanowire channels. *Nano-Micro Lett.* **17**, 154 (2025).
55. Y. Sun, T. Dong, L. Yu, J. Xu, K. Chen, Planar growth, integration, and applications of semiconducting nanowires. *Adv. Mater.* **32**, 1903945 (2020).
56. W. Liao, Y. Zhang, D. Li, J. Wang, L. Yu, High-density integration of uniform sub-22 nm silicon nanowires for transparent thin film transistors on glass. *Appl. Surf. Sci.* **679**, 161213 (2025).
57. X. Song, J. Fan, B. Sun, Y. Gu, S. Wang, J. An, D. Liu, J. Wang, L. Yu, Direct growth and integration of silicon nanowire transistors on polymer substrates. *ACS Appl. Mater. Interfaces* **17**, 48503–48510 (2025).
58. X. Song, Y. Gu, S. Wang, J. Fan, J. An, L. Yan, B. Sun, J. Wang, L. Yu, Scalable integration of high sensitivity strain sensors based on silicon nanowire spring array directly grown on flexible polyimide films. *Nano Lett.* **25**, 2290–2297 (2025).
59. J. An, Z. Hu, S. Hu, X. Song, J. Wang, L. Yu, Stable, step-guided growth of planar germanium nanowires at 200 °C via the in-plane solid-liquid-solid mechanism. *Adv. Sci.*, e14875 (2025).
60. J. An, L. Wu, Z. Hu, X. Song, J. Wang, L. Yu, In-plane growth control of uniform SiGe nanowires for thin film electronics. *Appl. Surf. Sci.* **718**, 164889 (2026).
61. F. A. Trumbore, Solid solubilities of impurity elements in germanium and silicon. *Bell Syst. Tech. J.* **39**, 205–233 (1960).
62. Y. Cheng, Z. Liu, J. Wang, J. Xu, L. Yu, Deterministic single-row-droplet catalyst formation for uniform growth integration of high-density silicon nanowires. *ACS Appl. Mater. Interfaces* **16**, 23625–23633 (2024).
63. M. Xie, W. Qian, J. Wang, L. Yu, Diameter scaling limit of catalytic silicon nanowires confined by optimized ultrafine sidewall grooves. *Appl. Phys. Lett.* **126**, 223103 (2025).
64. L. Yu, W. Chen, B. O'Donnell, G. Patriarche, S. Bouchoule, P. Pareige, R. Rogel, A. Claire Salaun, L. Pichon, P. Roca i Cabarrocas, Growth-in-place deployment of in-plane silicon nanowires. *Appl. Phys. Lett.* **99**, 203104 (2011).
65. R. Feng, F. Kremer, D. J. Sprouster, S. Mirzaei, S. Decoster, C. J. Glover, S. A. Medling, J. L. Hansen, A. Nylandsted-Larsen, S. P. Russo, M. C. Ridgway, Electrical and structural properties of In-implanted $Si_{1-x}Ge_x$ alloys. *J. Appl. Phys.* **119**, 025709 (2016).
66. M. Sistani, J. Delaforce, K. Bharadwaj, M. Luong, J. Nacenta Mendivil, N. Roch, M. den Hertog, R. B. G. Kramer, O. Buisson, A. Lugstein, C. Naud, Coulomb blockade in monolithic and monocrystalline Al-Ge-Al nanowire heterostructures. *Appl. Phys. Lett.* **116**, 013105 (2020).
67. Z.-Z. Zhang, Q. Hu, X.-X. Song, Y. Ying, H.-O. Li, Z. Zhang, G.-P. Guo, A suspended silicon single-hole transistor as an extremely scaled gigahertz nanoelectromechanical beam resonator. *Adv. Mater.* **32**, 2005625 (2020).
68. T. Dong, Y. Sun, J. Wang, J. Xu, K. Chen, L. Yu, Bismuth-catalyzed n-type doping and growth evolution of planar silicon nanowires. *Appl. Phys. Lett.* **117**, 243103 (2020).
69. Y. Sun, W. Qian, S. Liu, T. Dong, J. Wang, J. Xu, K. Chen, L. Yu, Unexpected phosphorus doping routine of planar silicon nanowires for integrating CMOS logics. *Nanoscale* **13**, 15031–15037 (2021).
70. R. Yuan, W. Qian, Y. Zhang, Z. Liu, J. Wang, J. Xu, K. Chen, L. Yu, Orthogonal-stacking integration of highly conductive silicide nanowire network as flexible and transparent thin films. *Adv. Electron. Mater.* **9**, 2201185 (2023).
71. R. Yuan, W. Qian, Z. Liu, J. Wang, J. Xu, K. Chen, L. Yu, Designable integration of silicide nanowire springs as ultra-compact and stretchable electronic interconnections. *Small* **18**, 2104690 (2022).

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Lithography-free, site-controlled germanium quantum dots in silicon nanowires for single-hole transistors operating up to 50 K

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