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Nanoscale Additive Manufacturing of Sub-24 nm Spacing Silicon Nanowire Arrays and High-Performance GAA FET Based on SiO_2/SiN_x Stacked Multilayers

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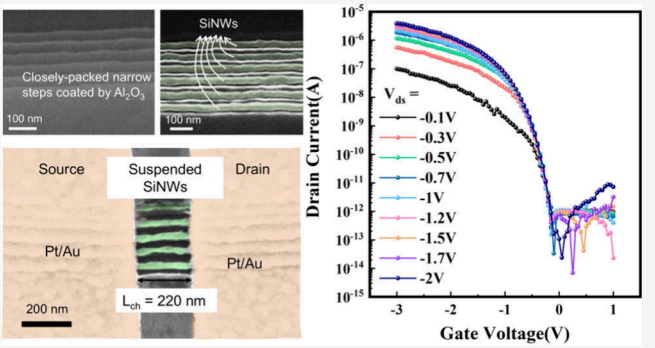
ABSTRACT: Deploying gate-all-around (GAA) field effect transistors (FETs) in the back-end-of-line (BEOL) represents a promising pathway to extend Moore's law. Although the in-plane solid−liquid−solid (IPSLS) approach can produce planar silicon nanowires (SiNWs) with precise positions and alignment at low temperatures, the SiNW density should be further enhanced for higher integration density. Here, we employed SiO_2/SiN_x stacked multilayers to fabricate ultranarrow guiding steps with controllable widths of 30−75 nm via conventional lithography, followed by producing dense ordered SiNWs with diameters of 25.9 ± 2.0 nm, horizontal spacing of 21.3 ± 2.3 nm, and vertical spacing of <22 nm. Facilitated by the alumina sacrificial layer for SiNW suspension, high-performance GAA-FETs were successfully fabricated, demonstrating an $I_{on}/I_{off} > 10^7$ and a steep subthreshold swing of ∼63.3 mV/dec. These results underscore the potential of IPSLS growth as a wafer-free additive manufacturing route in BEOL for monolithic 3D integration.



KEYWORDS: *Silicon nanowires, Monolithic 3D integration, GAA FET, Catalytic growth, Additive manufacturing*

As the miniaturization of field effect transistors (FETs) has approached the limits, monolithic 3D (M3D) integration has been proposed as a promising approach to extend Moore's law through a vertically stacked architecture.[1−3] In this architecture, the high-precision top-down photolithography and etching processes are employed on the high-quality silicon (Si) wafer for fabricating the logics in the front-end-of-line (FEOL), as indicated in Figure 1a, accompanied by the high-temperature process.[4−6] The additional logic, memory, and sensor layers are directly fabricated above the underlying device layer, as illustrated in the schematic of Figure 1b. However, there is no crystalline silicon (c-Si) wafer provided in the back-end-of-line (BEOL) layers, and the thermal budget must be strictly controlled (typically <450 °C) to maintain the integrity of the underlying FEOL devices,[7−9] which hinder the employment of top-down fabrication processes in the BEOL.

To address these challenges, nanoscale additive manufacturing of monocrystalline channels on the amorphous substrate at low temperatures (low-T) presents a promising method for achieving multidimensional integration. The well-established vapor−liquid−solid (VLS) mechanism can absorb a silane precursor via a catalyst to produce thin monocrystalline silicon nanowires (SiNWs), which are ideal quasi-one-dimensional (1D) channels.[10−12] However, even though a wide range of high-performance logic and sensor applications based on VLS-grown SiNWs have been demonstrated,[13−17] a critical challenge remains in precisely transferring and assembling these vertical building blocks onto a planar substrate, which typically requires complex and costly synthesis-then-transfer processes. Therefore, the VLS-grown SiNWs are unsuitable for fabricating the mainstream gate-all-around (GAA) FET architecture[18−20] in the BEOL.

Fortunately, the low-T in-plane solid−liquid−solid (IPSLS) growth has been proposed and developed, where indium (In) catalyst droplets absorb a solid amorphous silicon (a-Si) thin film precursor coated on the surface and then directly synthesize planar crystalline SiNWs at the rear deposition interface on the insulating layer,[21−23] as depicted in Figure 1c. In was selected as the optimal catalytic metal because of its low melting point (∼157 °C) and extremely low solubility within silicon,[24,25] ensuring highly controllable and stable SiNW growth. What's more, by using simple alternating C_4F_8 plasma anisotropic etching and O_2 plasma isotropic shrinkage, the terraced guiding steps were formed to assemble the SiNW

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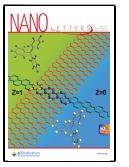

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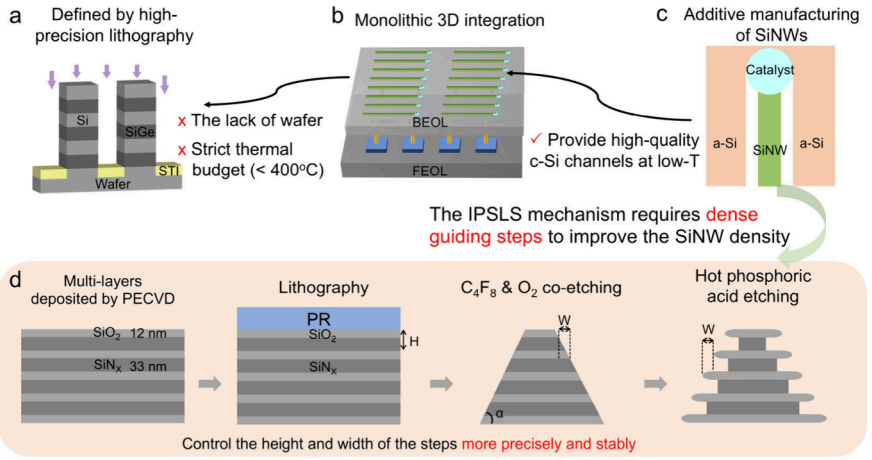

Figure 1. (a) Schematic of wafer-based Si/SiGe superlattice epitaxy and top-down high-precision lithography/etching processes. (b) Schematic of the monolithic 3D integration architecture, where upper-tier devices are fabricated directly on the wafer-free layer. (c) Schematic of the low-temperature IPSLS growth of SiNWs. (d) Fabrication workflow for multilayer narrow steps based on SiO_2/SiN_x stacked multilayers.

arrays with horizontal spacings of hundreds of nanometers,[26−28] followed by successfully fabricating high-performance devices and even GAA-FETs.[29−32] To further enhance the density of the SiNW arrays for higher integration density, the planar[33] or sidewall grooves[34,35] have been explored. However, these SiNWs remain embedded within the grooves, which lead to poor source/drain (S/D) metal contacts and difficult channel suspension, thereby constraining the practical fabrication of GAA-FETs.

In this work, we propose a method for fabricating multilayer narrow guiding steps with precise control over both step heights and widths using SiO_2/SiN_x stacked multilayers without high-precision lithography. Based on multisteps with widths of ∼50 nm, closely packed and ordered SiNW arrays were successfully fabricated, with diameters of 25.9 ± 2.0 nm, horizontal spacings of 21.3 ± 2.3 nm, and vertical spacings of <22 nm, achieving a density boost of >360% over the previous terraced step strategy with 90−100 nm NW−NW spacings. By releasing the alumina sacrificial layer to suspend the SiNWs, high-performance GAA FETs with a gate length of approximately 220 nm were successfully fabricated by EBL, exhibiting a high on/off current ratio of $>10^7$ and a steep subthreshold slope (SS) of down to 63.3 mV dec^{-1}.

Figure 1d illustrates the fabrication process of dense narrow guiding steps based on SiO_2/SiN_x stacked multilayers that were alternately deposited in the plasma-enhanced chemical vapor deposition (PECVD) system. After conventional photolithographic patterning with a precision of 3 μm, the samples were subjected to a dry co-etching process using a C_4F_8/O_2 gas mixture in the inductively coupled plasma (ICP) system. During this process, C_4F_8 plasma anisotropically etched the stacked multilayers, while O_2 simultaneously isotropically ablated the photoresist mask. This synergistic effect created a sloped profile/structure (which can be alternatively achieved via angled ion etching). Finally, hot phosphoric acid was employed to selectively etch the SiN_x layers at 140 °C for 5 min, yielding a multilayer guiding step structure, in which the height (H) is defined by the thickness of a single SiO_2/SiN_x period, whereas the step width (W) is determined by the thickness of SiN_x (t_{SiNx}) and the slope angle (α), governed by the relationship $W = t_{SiNx}/\tan \alpha$.

The 6-cycle stacked multilayer film was employed, with the SiO_2/SiN_x thickness of 12/33 nm. Figures 2a−c present an SEM cross-sectional view of the multilayer narrow guiding steps formed under varying O_2 flow rates. As the oxygen flow rate gradually increased from 40 to 60 sccm, the lateral erosion rate of the photoresist mask accelerated, causing the etched profile to transition from a steep to a gentler slope. Cross-sectional views for O_2 flow rates ranging from 10 to 30 sccm are provided in Figure S1 in the Supporting Information, revealing the gradual transformation from a strictly vertical profile to that with a slight inclination.

The corresponding SEM top views are shown in Figures 2d−f, where the arrow direction shows 5-layer steps from high to low. As the oxygen flow gradually increases, a gradually monotonic increase in step width was correspondingly observed. The narrow step width of each layer under different O_2 flow rates was quantified in Figures 2g−i. Specifically, under an oxygen flow rate of 40 sccm, the step width per layer is approximately 30 nm. When the flow rate was increased to 50 and 60 sccm, the step width of each layer was widened to 50 and 75 nm, respectively. When the guiding ministeps are too narrow, In droplets on adjacent steps could touch and merge into a larger one, leading to some empty guiding steps without SiNW growth due to the lack of a catalyst droplet. What's more, the larger droplets will produce thicker SiNWs with significant fluctuations in diameter. To maintain a high SiNW density while preventing large In droplets from crossing or striding over the ultradense steps, the optimized gas ratio of C_4F_8/O_2 = 18/50 sccm was selected, yielding stable 5-layer narrow steps with the width of approximately 50 nm. To achieve a further improvement of integration density in the future, the supply of In layers should be properly controlled by reducing the thickness of the In film and integrating an edge-trimming technique[36] to form smaller and more uniform In droplets, which is critical for enabling the stable guided growth of ultrathin SiNWs on narrower steps.

However, direct growth of SiNWs within deep SiN_x grooves poses a significant challenge for subsequent device integration, as the S/D metal cannot effectively wrap around the SiNWs to form a reliable contact. To address this problem, an Al_2O_3 layer was deposited via atomic layer deposition (ALD) to close the grooves while preserving the guiding step morphology, as illustrated in Figure 3a. At the same time, the Al_2O_3 film as a sacrificial layer also facilitates the subsequent release of the SiNWs. Figure 3b presents the SEM top view after depositing

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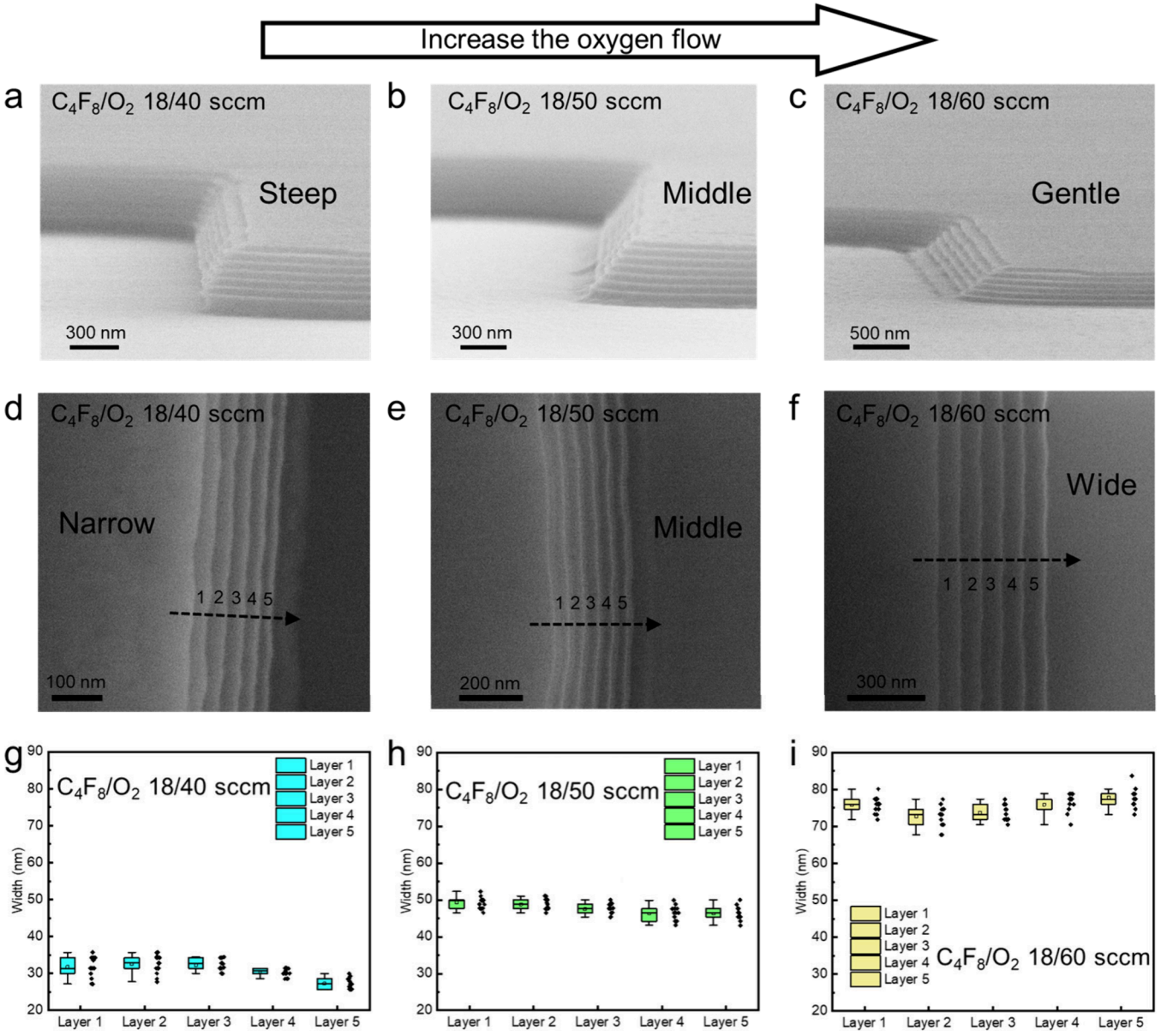

Figure 2. Cross-sectional (a–c) and corresponding top-view (d–f) SEM images of the multilayer narrow steps fabricated with O_2 flow rates of 40, 50, and 60 sccm, respectively. (g–i) Statistical distributions of the step widths for each layer under the respective O_2 flow conditions.

25 nm thick Al_2O_3, confirming highly conformal deposition, where the step width remains consistent with that before deposition. It can also be proven from Figure 3g, which shows 80 narrow steps after Al_2O_3 deposition, with an average width of 47.9 ± 3.7 nm. The SEM side view in Figure 3c reveals that the SiN_x grooves wet-etched by hot phosphoric acid were almost completely closed, leaving only a shallow recess. This residual recess arises from the curved edges of the protruding SiO_2 spacers and sunken SiN_x grooves, which help the conformal Al_2O_3 deposition to form a shallow recess between adjacent layers ($t_{SiNx} < 2t_{Al2O3}$).

Subsequently, the catalyst region was defined via 3 μm-precision conventional photolithography, followed by thermally evaporating a nominal 1.8 nm-thick In film, as shown in Figure 3d. The In particles are well separated by each narrow step with the step width strictly limiting the In supply for each layer. Then, the samples were treated by H_2 plasma with the power of 10 W for 5 min @200 °C in the PECVD system to reduce the native oxide layer on the In particles, making them diffuse and merge into discrete droplets. The temperature was then lowered to 100 °C to freeze the In droplets, prior to coating a thin a-Si film with a thickness of ∼10 nm by using silane plasma with a power of 1 W. Finally, the temperature was raised up to 300 °C for annealing under vacuum. During this process, In droplets were molten again to absorb the a-Si precursor at the front interface along the guiding steps and precipitate Si atoms at the rear interface due to supersaturation, thereby assembling crystalline SiNWs along the moving path. Further details of the experiments and growth mechanism are available in our previous works.[37−40]

Figure 3e presents the SEM image after IPSLS growth, revealing six SiNWs densely aligned along the multilayer narrow guiding steps. A high-magnification close-up is provided in Figure 3f, where the nanowires are false-colored light green and denoted by white arrows for better observation. It can be seen that the SiNWs grown on these narrow guiding

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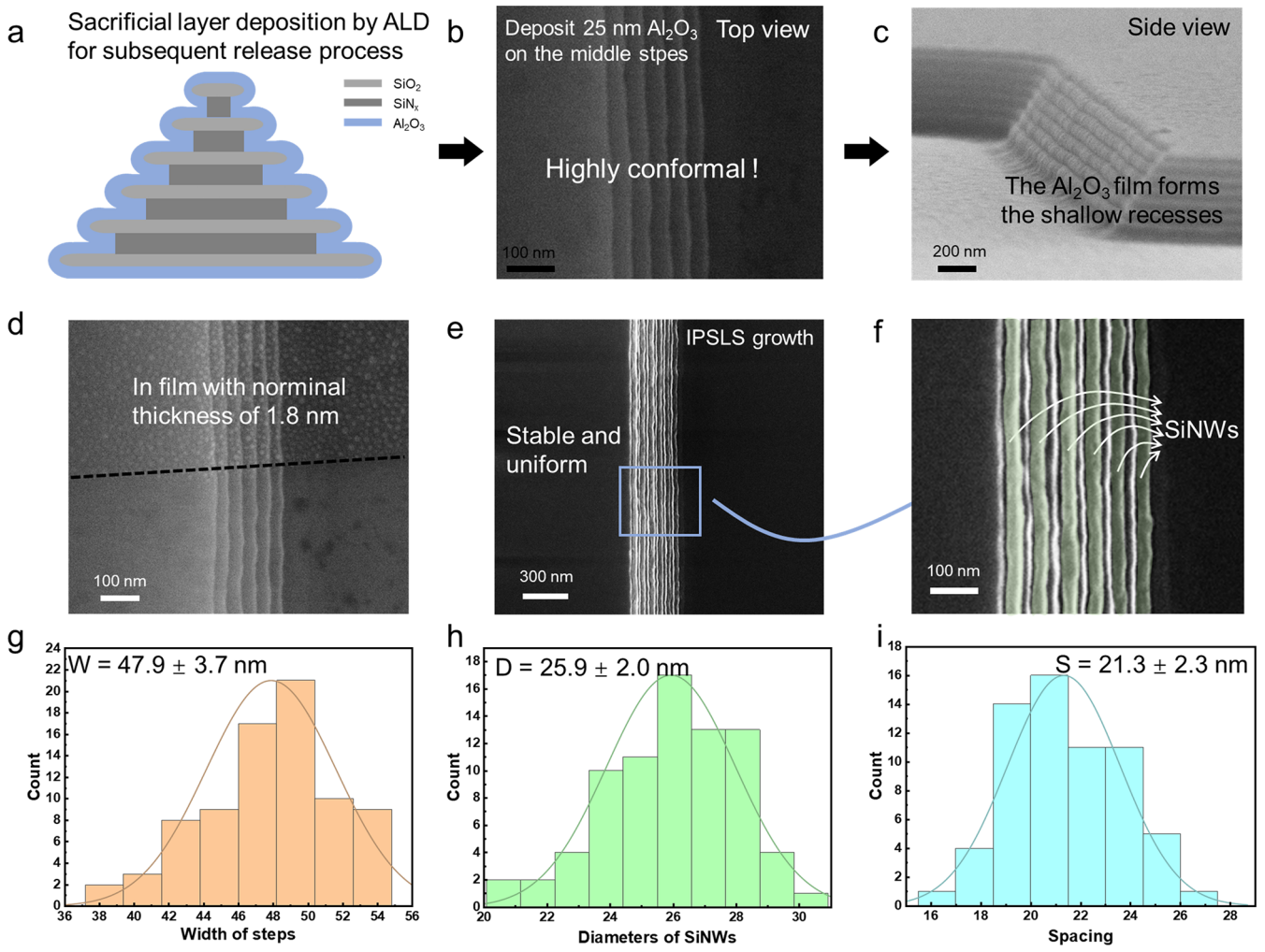

Figure 3. Schematic (a), corresponding top-view (b) and side view (c) SEM images of the multilayer narrow step structure after Al_2O_3 deposition, where the Al_2O_3 layer closed the grooves while creating shallow recesses on the steps. (d) SEM image of a sample with a 1.8 nm thick In film defined by conventional photolithography. (e) SEM image of the uniform, densely packed IPSLS-grown SiNWs on the narrow steps, with a high-magnification view shown in (f). Statistical distributions of the step widths after Al_2O_3 deposition (g), SiNW diameters (h), and horizontal NW−NW spacings (i).

steps exhibit exceptional dimensional uniformity, with an average diameter of 25.9 ± 2.0 nm, as shown from the statistics of 77 as-grown SiNWs in Figure 3h, demonstrating a diameter deviation of less than 10%. Furthermore, the SiNW arrays feature an ultrahigh integration density with an NW−NW spacing of 21.3 ± 2.3 nm (quantified in Figure 3i), achieving a density enhancement exceeding 360% compared to the previous terraced step strategy with 90−100 nm NW−NW spacings.[26] This growth integration strategy can compete with the state-of-the-art top-down process such as the high-precision lithography and etching[41] or self-aligned double/quadruple patterning process.[42,43]

Figure 4a schematically illustrates the contact situation of In droplets upon the multilayer narrow guiding steps. The shallow recesses formed by the Al_2O_3 layer previously mentioned effectively constrained the In droplets, thereby preventing the In droplets from crossing/striding over the steps and allowing SiNWs to grow stably along the step edges.

Focused ion beam (FIB) milling combined with transmission electron microscopy (TEM) analysis was carried out on the SiNWs grown on the multilayer narrow steps, as shown in Figure 4b. The light-blue area corresponds to the Al_2O_3 layer deposited by ALD, within which the step structures with shallow recesses are clearly resolved. As observed, the SiNWs falsely colored pale green exhibit stable growth closely adjacent to shallow recesses on the narrow steps. The inset provides the energy dispersive spectroscopy (EDS) elemental mapping of silicon for the #5 SiNW, confirming its material composition. The regions false-colored in light-yellow represent the residual unconsumed a-Si, which can be subsequently selectively removed via CF_4 plasma etching in the reactive ion etching (RIE) system, as demonstrated by the SEM image of the SiNWs after etching the a-Si in Supplementary Figure S2. In addition, the black dashed lines denote the tight vertical separation between adjacent SiNWs with a vertical spacing of <22 nm, highlighting the high degree of vertical integration. Figure 4c and 4d respectively present representative high-resolution TEM images of the #2 and #4 SiNWs, revealing high-quality single-crystalline structures, with the corresponding fast Fourier transform (FFT) patterns in the insets, which indicate that the growth orientations align along the <100> and <110> as the two predominant crystallographic orientations.

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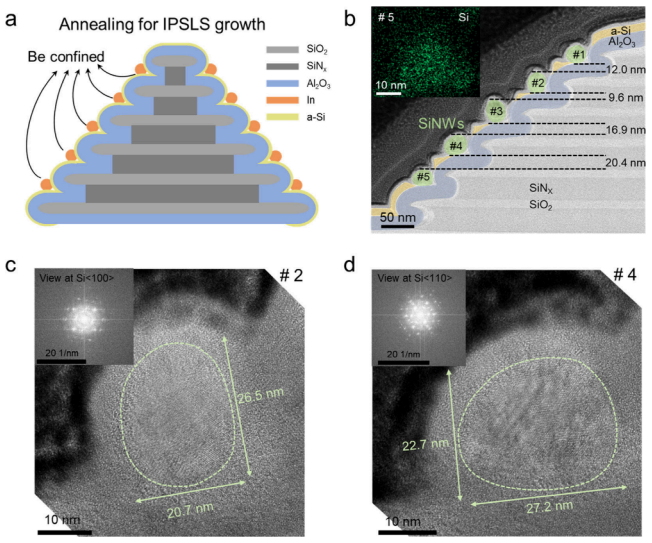

Figure 4. (a) Schematic illustrating the contact situation of In droplets on the narrow steps coated by a-Si. (b) Cross-sectional TEM image of the densely packed SiNW array grown on the narrow steps. High-resolution TEM images of (c) #2 and (d) #4 SiNWs, with the corresponding Fast Fourier Transform (FFT) patterns in the inset, exhibit high-quality single-crystal structures.

The short-channel source/drain (S/D) electrodes were defined by EBL, followed by evaporation of Pt/Au with thicknesses of 12/55 nm via electron beam evaporation (EBE). With the SiNWs firmly anchored by the S/D electrodes, a wet etching process using tetramethylammonium hydroxide (TMAH) was employed to selectively remove the underlying Al_2O_3 layer, thereby resulting in the release and suspension of the SiNWs, as illustrated schematically in Figure 5a. Subsequently, a gate dielectric stack consisting of 2/6 nm thick Al_2O_3/HfO_2 was conformally deposited by ALD. Finally, the gate region was defined by EBL and then covered by a 60 nm thick Ni layer via magnetron sputtering to form the surrounding gate electrode, completing the fabrication of the GAA-FET. Figure 5b presents the typical SEM image of the suspended SiNWs with a channel length of ~220 nm. It can be seen that after removing the sacrificial layer, the SiNWs situated between the S/D electrodes remain well aligned, exhibiting a relatively bright contrast. The underlying region beneath the SiNWs appears dark, indicating the presence of the interspace due to the removal of alumina, which confirms the successful suspension of the SiNWs. In contrast, the SiNW segments that were not anchored by S/D electrodes collapse randomly onto the steps or planar substrate, exhibiting a noticeably darker contrast, as highlighted by the white box in Figure 5b. As the suspended channel length increases, the middle portion of the SiNWs with a darker contrast is dragged down by surface tension, while the segments near the electrodes remain securely suspended, exhibiting a brighter contrast, as shown in Supplementary Figure S3.

Figure 5c presents the SEM image of a complete GAA-FET device, where the S/D leads with a width of approximately 700 nm were fully covered by the gate electrode. A typical transfer characteristic of the GAA-FET was shown in Figure 5d, demonstrating an ultralow off-state leakage current, a high on/off current ratio of $\gg 10^7$, and a large on-state current of 16.7 $\mu A/\mu m$ under a bias of $V_{gs} = -3$ V and $V_{ds} = -2$ V. Notably, with increasing gate voltage, the transfer characteristics exhibited negligible threshold voltage drift and no significant rise in off-state current, demonstrating excellent electrostatic control. The corresponding output characteristics are shown in Figure 5e, which exhibit a linear relationship under the low drain voltage, indicating the formation of an Ohmic-like contact between the Pt/Au electrodes and SiNW channels. The extracted subthreshold slope (SS) values at different V_{gs} are summarized in Figure 5f, which are consistently lower than 80 mV/dec for all gate biases, with a minimum value of 70.3 mV/dec.

To evaluate the consistency between devices, the transfer characteristics of 26 devices at $V_{ds} = -0.3$ V are presented in Figure 5g. It can be observed that all devices exhibit a high on/off current ratio, low off-state current down to the <0.1 pA level, and fast switching speeds. The threshold voltages among the devices show slight variation, with a main variation range of within ±0.3 V, which is primarily attributed to fabrication processes, such as channel length variations during EBL and batch-to-batch nonuniformities introduced during the deposition of S/D metal, dielectric layers, and a gate electrode. The SS values extracted from the 26 transfer characteristic curves are shown in Figure 5h, exhibiting an average of 74.9 ± 5.3 mV/dec with a minimum of 63.3 mV/dec. Figure 5i shows the statistics of the on/off current ratios for these 26 devices, all of which exhibit a high $I_{on}/I_{off} > 10^6$, with some reaching as high as 3×10^7. This variation may be attributed to differences in threshold voltage, which lead to inconsistent switching windows across different devices. Nevertheless, these results demonstrate the ultrahigh device performance of the GAA-FETs based on the multilayer narrow step structures, which can serve as a wafer-free additive manufacturing route for BEOL in M3D integration architecture.

We have compared our GAA-FET with those described in other literature and summarized the results in Table 1 to provide a clearer overview. The IPSLS growth paradigm successfully bridges the critical gap between bottom-up and top-down approaches. It not only resolves the positioning, guiding, assembly, and low-density issues inherent in traditional bottom-up growth methods, but also achieves high-performance devices comparable to GAA-FETs fabricated via top-down etching processes. A benchmark plot summarizing the SS and ON/OFF current ratio (I_{on}/I_{off}) is presented in Supplementary Figure S4.

It should be noted that the IPSLS-grown SiNW channels with an average diameter of 25.9 ± 2.0 nm should expect an orientation-dependence of the carrier mobilities in the SiNW channels, which is similar to that in the bulk silicon. However, the SiNW GAA-FETs are fabricated based on a group of 6 parallel SiNWs. So, the mixture of <100> and <110> oriented SiNWs will effectively average out the effect of orientation variations in individual SiNWs. As demonstrated in the experimental results, the smooth, hump-free transfer characteristic curves exhibit a steep, uniform SS and comparable I_{on} levels. As the SiNW diameter continues to scale down, achieving controllable and strict crystallographic consistency is undoubtedly crucial for advanced device manufacturing in the future.

In summary, the multilayer narrow step structures with controllable widths of approximately 30−75 nm were successfully fabricated via SiO_2/SiN_x stacked multilayer films patterned by combination with conventional photolithography and a collaborative etching process. Subsequently, highly uniform and densely packed SiNW arrays were synthesized at a

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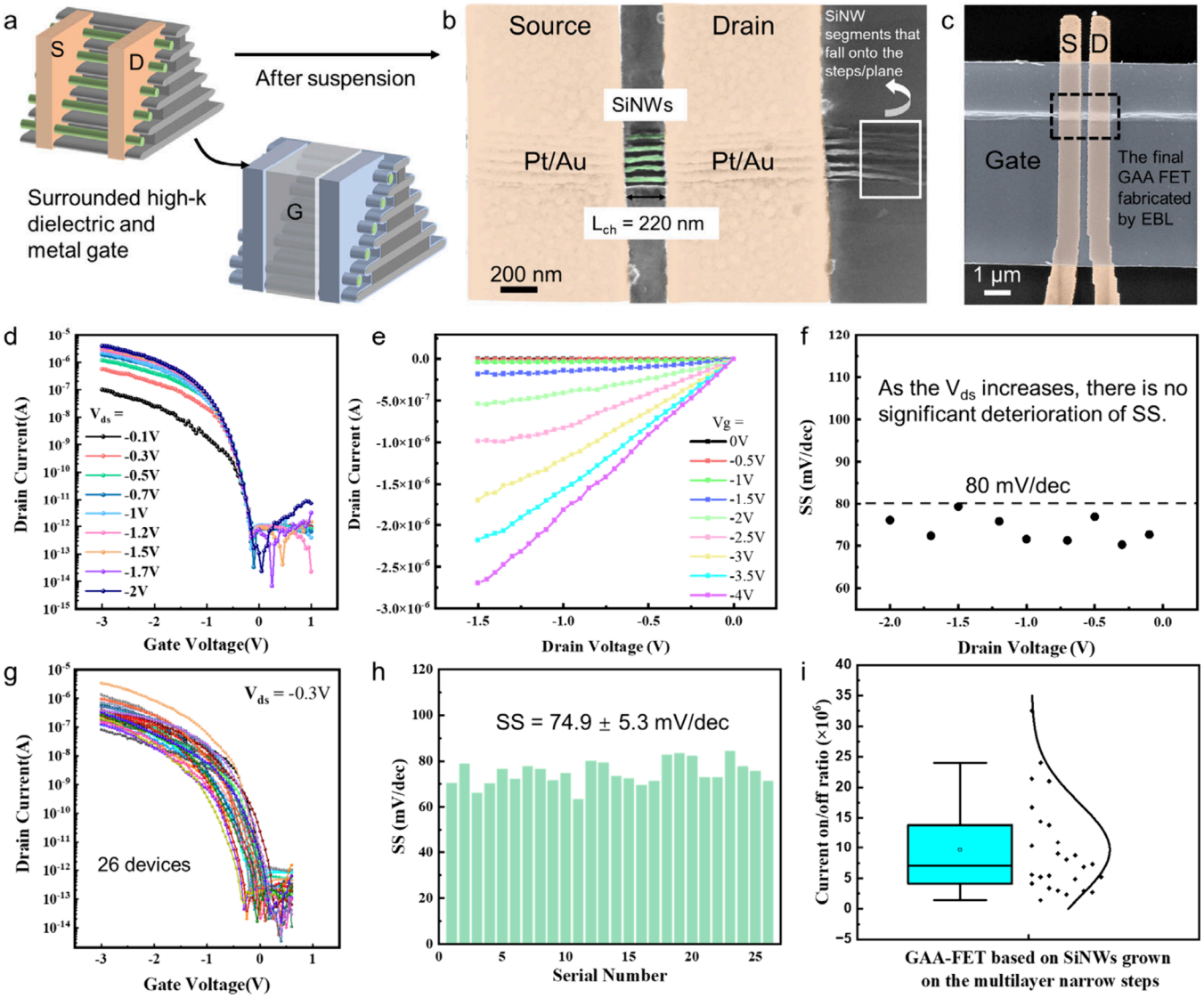

Figure 5. (a) Schematic illustration of the GAA-FET structure, where SiNWs anchored by S/D electrodes are suspended via the selective removal of the sacrificial layer. (b) SEM image of representative suspended SiNWs with a channel length of 220 nm. (c) SEM image of the completed GAA-FET fabricated on dense SiNW arrays on narrow steps. Transfer characteristics (d), output characteristics (e), and SS extracted under different V_{gs} (f) values of a typical GAA-FET. (g) The transfer characteristic curves of 26 devices measured at V_{ds} = −0.3 V, with the corresponding extracted SS in (h) and on/off current ratios in (i).

Table 1. Comparison of Our GAA-FET to Those in Other Literature

Channel	Fabrication	CD (nm)	V_{ds}/V_{gs} (V)	I_{ON} (A)	I_{ON}/I_{OFF}	SS (mV/dec)
VLS growth[44]	Transfer	25−60	−0.5/−1	10^{-7}	10^{6}	105 (P)
VLS growth[45]	Transfer	20−150	1/2	10^{-8}	10^{5}	121 (N)
VLS growth[46]	Confinement	120	−0.05/−6	10^{-7}	10^{6}	146 (P)
Si/SiGe epitaxy[47]	SADP	8	−0.9/−1	10^{-4}	10^{7}	85 (P)
Si/SiGe epitaxy[48]	-	13	−0.65/−1.5	10^{-6}	10^{6}	65 (P)
Si/SiGe epitaxy[49]	SADP	21	−0.8/−1.5	10^{-6}	10^{6}	63 (P)
Si/SiGe epitaxy[50]	SADP	28.1	−0.9/−1.2	10^{-6}	10^{7}	60.3 (P)
Si/SiGe epitaxy[51]	DUV	30	−0.9/−1.2	10^{-5}	10^{6}	65.8 (P)
IPSLS growth (This work)	**Conventional lithography**	**25.9**	**-0.3/−3**	$\mathbf{10^{-6}}$	$\mathbf{10^{7}}$	**63.3 (P)**

low T of 300 °C via the IPSLS mechanism, featuring diameters of 25.9 ± 2.0 nm, horizontal spacings of 21.3 ± 2.3 nm, vertical spacing of <22 nm, and a density boost of >360% compared to the previous terraced step strategy with 90−100 nm NW−NW spacings. These additive manufacturing SiNW arrays grown on the multilayer narrow steps are comparable to a top-down process with the aid of EBL/EUV lithography. Thanks to the Al_2O_3 sacrificial layer, the SiNWs were successfully suspended, enabling the subsequent fabrication of high-performance GAA-FETs which exhibit a high I_{on}/I_{off} of >10^7 and a steep SS down to 63.3 mV/dec These results demonstrate a reliable low-T growth integration strategy for fabricating high-density

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crystalline silicon channels and high-performance GAA-FETs, which can serve as a wafer-free additive manufacturing approach for BEOL implementation in M3D integration architectures.

■ ASSOCIATED CONTENT

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

Supporting Information

The Supporting Information is available free of charge at https://pubs.acs.org/doi/10.1021/acs.nanolett.6c00801.

Cross-sectional SEM images of the multilayer narrow steps fabricated with O_2 flow rates of 10, 20, and 30 sccm, respectively; SEM image of the SiNWs after etching the a-Si; SEM images of SiNWs with a suspension length of 638 and 720 nm, respectively; benchmark plot summarizing the comparison of our GAA-FET to those in other literature (PDF)

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Wentao Qian and Le Weng contributed equally to this work.

Notes

The authors declare no competing financial interest.

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