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Deterministic Single-Row-Droplet Catalyst Formation for Uniform Growth Integration of High-Density Silicon Nanowires

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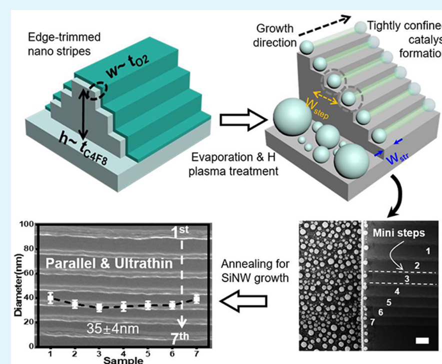
ABSTRACT: Planar silicon nanowires (SiNWs), grown by using low temperature catalytic approaches, are excellent 1D channel materials for developing high-performance logics and sensors. However, a deterministic position and size control of the metallic catalyst droplets, that lead to the growth of SiNWs, remains still a significant challenge for reliable device integration. In this work, we present a convenient but powerful edge-trimming catalyst formation strategy, which can help to produce a rather uniform single-row of indium (In) catalyst droplets of D_{cat} = 67 ± 5 nm in diameter, with an exact one-droplet-on-one-step arrangement. This approach marks a significant achievement in self-assembled catalyst formation and offers a foundation to attain a reliable and scalable growth of density SiNW channels, via an in-plane solid−liquid−solid (IPSLS) mechanism, with a uniform diameter down to D_{nw} = 35 ± 4 nm, and do not rely on high-precision lithography techniques. Prototype SiNW-based field effect transistors (FETs) are also fabricated, with a high I_{on}/I_{off} current ratio and small subthreshold swing of >10^7 and 262 mV·dec^{-1}, respectively, indicating a reliable new routine to integrate a wide range of SiNW-based logic, sensor, and display applications.



KEYWORDS: *Silicon nanowires, Edge-trimming, Diameter control, IPSLS growth; Indium droplets; Field effect transistors*

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1. INTRODUCTION

Silicon nanowires (SiNWs) are an important quasi-one-dimensional (1D) semiconducting channel materials,[1−7] with excellent electrostatic control and unique structural, optoelectronic and transport characteristics. They are also the most advantageous building blocks to construct high-performance electronic logics,[8,9] thin film transistors,[10−12] and chemical or biosensors.[13−16] Though thin SiNWs can be directly etched out of c-Si wafer by using sophisticated electron beam lithography (EBL) or extreme ultraviolet (EUV) lithography technologies (Figure. 1a),[17−22] a reliable fabrication and integration of orderly 1D SiNW channel array, directly upon low-cost glass or flexible polymer substrates for display or sensor application,[23] remains still a technical challenge. Alternatively, these narrow SiNWs may be produced via a bottom-up catalytic growth, for example the famous vapor−liquid−solid (VLS) approach, where tiny metallic catalyst droplets take in gaseous precursors of silane to precipitate crystalline SiNWs with diameters controlled by the sizes of the leading droplets.[24−28] The VLS-grown SiNWs have been successfully explored to fabricate a wide range of high performance prototype devices, such as SiNW-based logics,[29] sensors,[30] and thin film transistors (TFTs).[31] However, as the gaseous precursor feeding in VLS growth tends to produce vertical bundles of standing SiNWs, they need to be collected, transferred and rearranged into precise locations on planar surface for reliable logic device integration.[32] Though many research efforts have been developed to achieve planar growth of VLS SiNWs,[33,34] surface faceted groove-guided planar growth,[35,36] or postgrowth rearrangement of them,[37,38] a scalable integration of orderly VLS-grown SiNWs on planar surface is still missing.

In order to address this challenge, an in-plane solid−liquid−solid (IPSLS) growth mode was proposed in our previous works,[39] where indium (In) catalyst droplets were employed to absorb amorphous silicon (a-Si) precursor layer deposited on substrate surfaces to produce crystalline planar SiNWs. By this way, the In catalyst droplets can be further guided by predefined multistep edges to produce well aligned SiNW arrays at desired locations (the middle panel of Figure 1a), which is highly beneficial for scalable electronic device integration. Similar to the famous VLS growth,[40−42] the diameter of the IPSLS SiNWs is also determined by the size of the leading catalyst droplets (the right panel of Figure 1a). Therefore, the size dispersion of the initial metallic catalyst droplets will be inherited and passed on to the as-grown SiNWs, and thus it has to be well-controlled for seeking a

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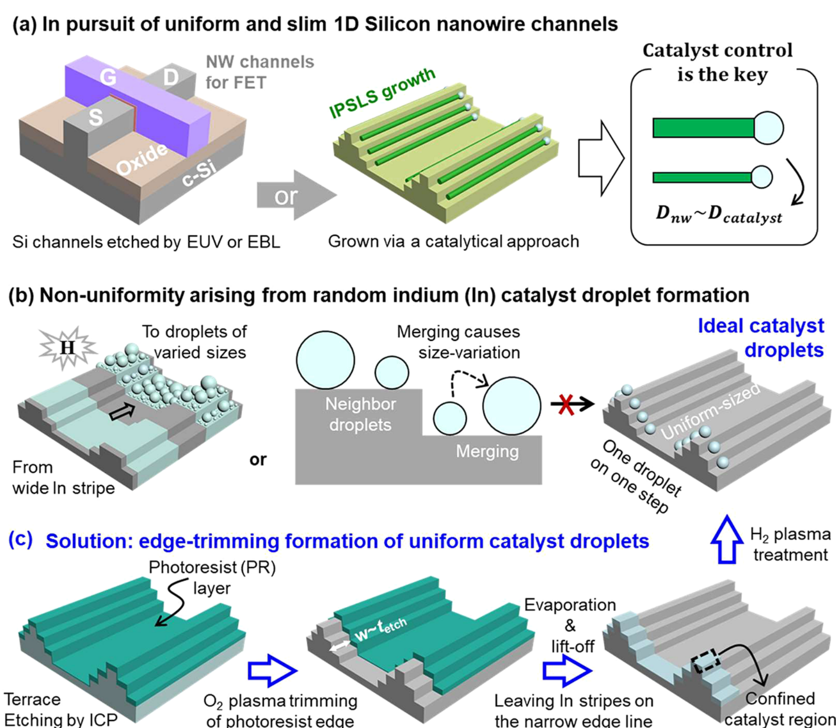

Figure 1. (a) Schematic illustration of a FET with thin nanowire-like quasi-1D channels etched via EUV or EBL technology, compared to a catalytic growth formation of a dense array of thin SiNWs led by metallic catalyst droplets, where the size uniformity and position control of SiNWs arrays are largely determined by the initial size and location of catalyst droplets. (b) Large size dispersion of In droplets arises mainly from the random droplet merging among wide indium stripe during the H_2 plasma treatment, while **c** proposes a deterministic edge-trimming strategy to form single-row of discrete In droplets at the end-edges of a truncated guiding terrace, ready for leading a uniform IPSLS growth of an orderly SiNW array.

highly uniform and reliable fabrication (Figure 1b). Though many strategies have been adopted to tailor successfully the size of the catalyst droplets in the VLS growth approach, such as electron beam lithography (EBL) catalyst patterning[43] and template assisted growth.[44] Recently, we also explored the use of EBL to pattern narrow stripes of indium (In) catalyst, with initial width down to 100 nm, and found that this size confinement is beneficial for forming uniform rows of In droplets.[45] However, all of these sophisticated catalyst formation technologies are not applicable for integration of electronics.

In this work, we propose and demonstrate a new edge-trimming approach for the formation of uniform single-row catalyst droplets (Figure 1c), without the use of any high precision electron beam or DUV lithography technologies. Here, the narrow nanostripes were formed by trimming/burning the exposed photoresist sidewalls by using an O_2 plasma, at the ends of truncated multistep guiding terraces, where the receded width formed by the trimming process defines the width of the nanostripe for later In catalyst deposition. As this receding process can be well controlled by the plasma treatment duration, to <100 nm, as depicted schematically in Figure 1c, individual catalyst droplets can be precisely obtained at each terrace step, as orderly single-row array, as depicted in the rightmost panel in Figure 1c. Note that this unique deterministic catalyst formation control has never been accomplished before, and more importantly, it can help to achieve a uniform growth of orderly and high density planar SiNWs, with diameter fluctuation reduced to ~35 ± 4 nm, which is desirable for the fabrication of high performance SiNW-based TFT devices.

2. EXPERIMENTAL SECTION

2.1. Preparation of Dense Mini-steps. The c-Si (100) wafer substrates (2 × 2 cm) were subsequently cleaned by using acetone solution and ethanol solution in an ultrasonic system for 5 min, rinsed with deionized water three times, and then dried at 100 °C for 10 min. For the formation of multiple guiding mini-step, the oblique sidewall mini-steps are prepared by using alternating etching of the C_4F_8 and O_2 in ICP. The anisotropic C_4F_8 etching step was used to define the depth of the mini-steps, while the O_2 plasma burning step erodes the edge of photoresist (PR) layer, forcing it to recede for a width of the mini-steps. The width of steps can be easily controlled by the plasma treatment duration via alternating the durations of the C_4F_8 and the O_2 etching periods.

2.2. Edge-Trimming Droplet Formation. Second lithography was conducted to expose the end of the guiding terraces. Then, the terrace end was etched by using C_4F_8 by ICP for 150 s to a depth of 300 nm, prior to a O_2 plasma treatment that trimmed the edge of the photoresist layer and exposed a stripe of ~100 nm wide. After that, a thin In layer of nominally 16 nm thick was deposited by using thermal evaporation. After standard lift-off procedure, a narrow stripe of In layer of ~100 nm wide was left along the truncated terrace edge lines. Then, the samples were loaded into a PECVD system and subject to a H_2 plasma treatment at 300 °C, with gas flow rate, chamber pressure, and RF power density of 13 SCCM, 140 Pa, and 125 mW cm^{-2}, respectively, for 5 min. During this process, the native surface In oxide layer on the In stripe was reduced and the In thin film was allowed to melt and agglomerate into discrete droplets, single catalyst droplets can be precisely formed at each terrace step as orderly single-row array.

2.3. Growth of Uniform and High-Density SiNW. Amorphous silicon (a-Si) layer with thickness of 16 nm was deposited at a lower temperature of 150 °C (below the melting point of In), with 2 SCCM pure SiH_4 plasma, with 20 Pa pressure, and 20−60 mW cm^{-2} power density, for 3 min. Then, the substrate temperature was raised to 350

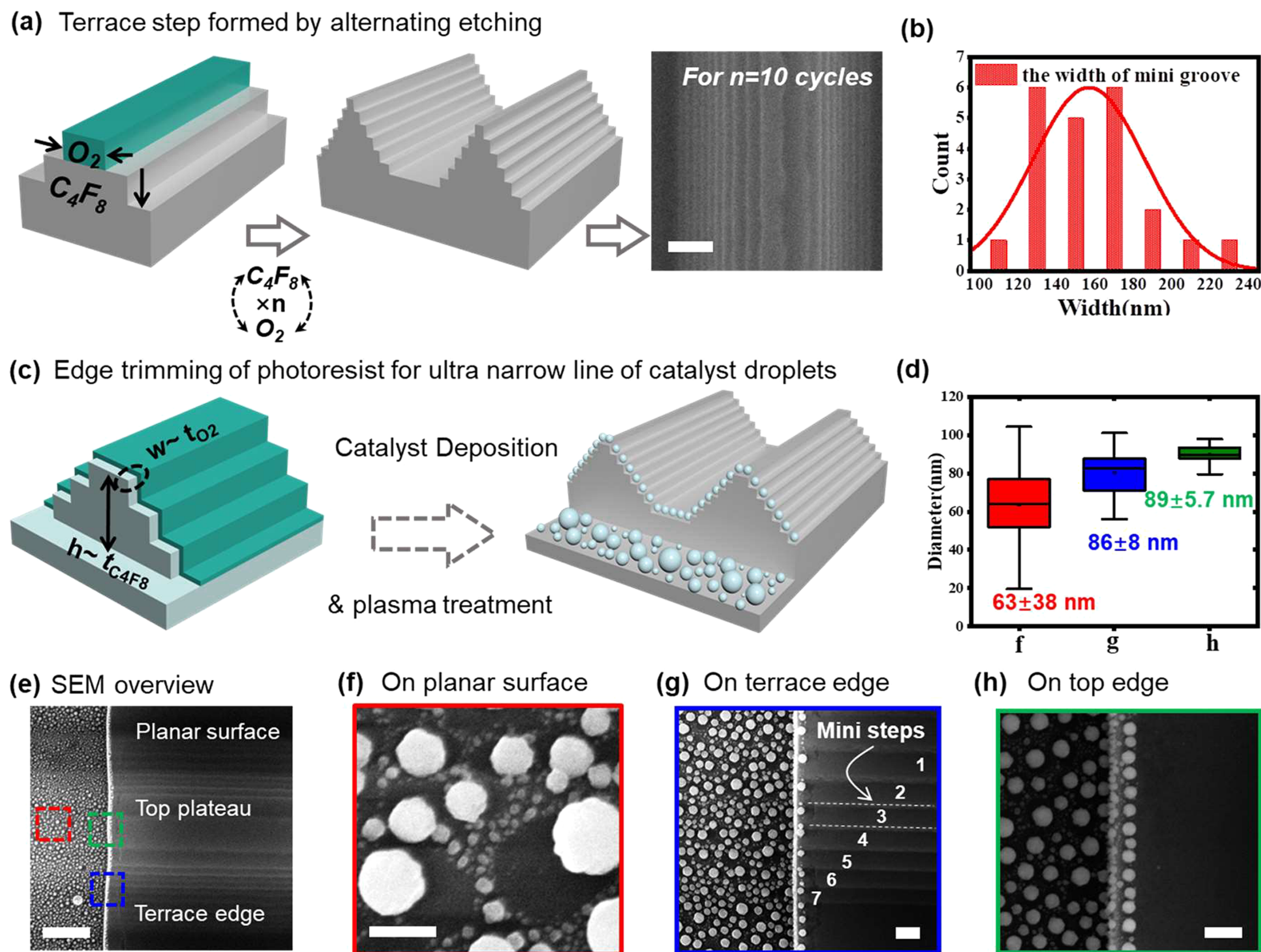

Figure 2. (a) Schematic illustration of the formation of guiding terrace with dense mini-steps produced by alternating O_2 plasma burning of photoresist and vertical C_4F_8 etching of SiO_2 substrate. A typical 10-steps prepared via 10 cycles is also shown on the right panel, with step width statistics shown in panel b. (c) Edge-trimming of the photoresist, after vertical truncation at the edge of a terrace, which has a controllable receding depth of $d \sim t_{O_2}$. After evaporation of the In layer and H_2 plasma treatment, a uniform single-row of catalyst droplets was formed on the edge lines of multistep terraces. (d) The diameter statistics of the catalyst droplets formed on planar surface (red), terrace edge (blue), and top flat edge (green). (e−h) SEM images of the In droplets formed at the different locations, marked by different colors. Scale bars in a and e stand for 1 μm, and in f, g, and h stand for 200 nm.

°C under vacuum for 1 h, and the In droplets became molten again and started to move around by absorbing the nearby a-Si layer to produce crystalline SiNWs. When the In droplets ran into the mini guiding steps, the extra a-Si supply on the step edges can help to attract the In droplets to move along the edge lines and produce guided growth of SiNWs. At the end of the SiNW growth, the remnant a-Si layer can be selectively removed by using H_2 plasma etching at 180 °C.

2.4. FET Fabrication and Measurement. Upon the SiNW arrays grown on dense mini steps via IPSLS mode, lithography was carried out to define the source (S) and drain (D) electrode regions. Before the evaporation of platinum (5 nm)/Al (50 nm) electrodes by EBE, the native oxide layer on the SiNWs was removed in a 4% HF solution for 10 s. After that, the photoresist was cleaned in a standard lift-off procedure. Then, the SiNW channels were coated with a dielectric Al_2O_3 layer of 25 nm thick by atomic layer deposition, and the top gate was defined by lithography and evaporation of 60 nm Al electrode. The electronic transport characteristics were measured by using a Keithley 2636B instrument at room temperature.

3. RESULTS AND DISCUSSION

3.1. Uniform Catalyst Droplet Formation on the Trimmed Edge. The guiding oblique terrace, as seen in Figure 2a, was first formed by ICP alternating the etching durations in the C_4F_8 and the O_2 plasma cycles. Specifically, an anisotropic C_4F_8 etching step was carried out to define the depth of the first SiO_2 mini-step, followed by a O_2 plasma treatment step to erode the edge of the photoresist layer, forcing it to recede to a certain width and form the guiding step. For example, a side-view SEM image of an oblique 10-layer terrace, formed after alternating gas etching steps of $t_{C_4F_8}$ = 30 s and t_{O_2} = 50 s for 10 cycles, is shown in the rightmost panel of Figure 2a, while statistics of the width of the mini steps is presented in Figure 2b.

After the fabrication of the multistep guiding terrace edges, a second lithography was conducted to expose the end of the guiding terraces, as diagrammed in Figure 2c. Then, the terrace end was etched by using ICP to a depth of ~300 nm, prior to a O_2 plasma treatment that trimmed the edge of the photoresist

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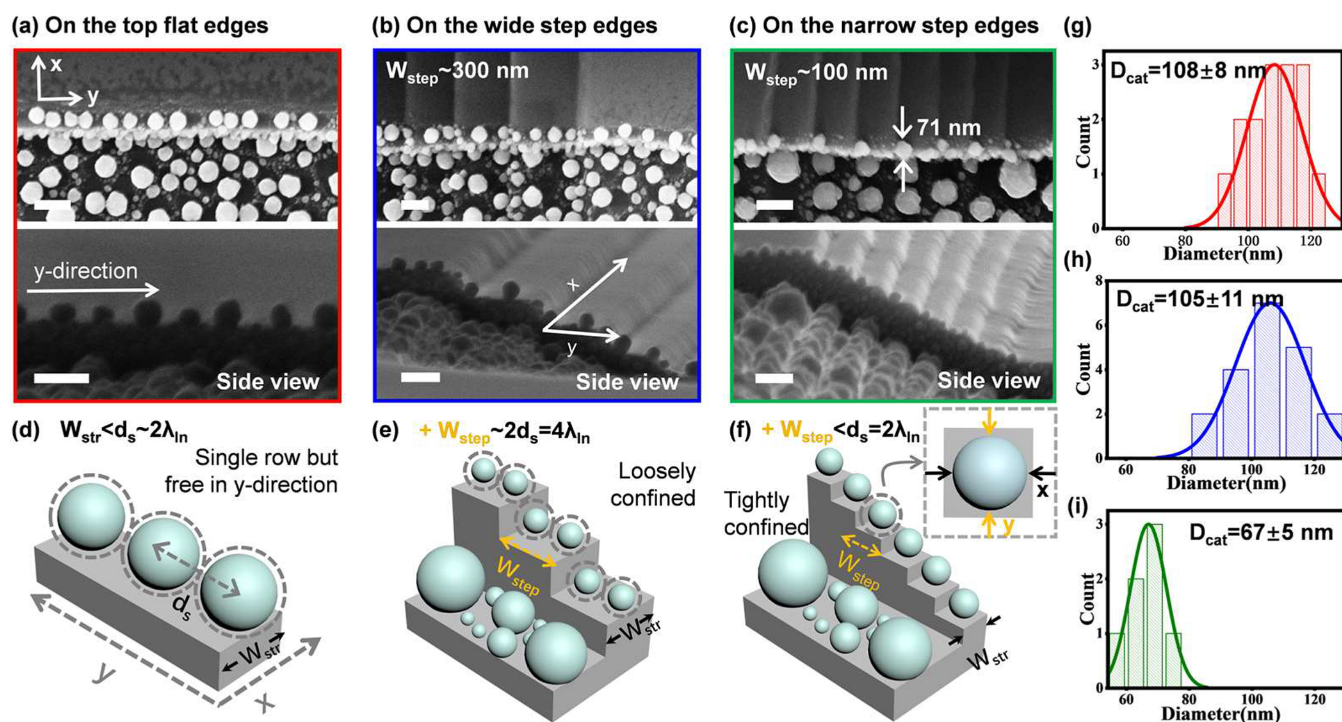

Figure 3. (a−c) Droplet formation on the top flat edges, on the wider step edges of W_{step} ∼ 300 nm, and on the narrow step edges of W_{step} ∼ 100 nm, respectively, after H_2 plasma treatment, with a constant edge-trimming width W_{str} of ∼100 nm. (d−f) Schematic illustration of the corresponding droplet formation on the different places on a terrace. (g−i) Diameter statistics of the catalyst droplets formed for different W_{step}. Scale bars are all 200 nm.

layer and exposed a stripe of ∼100 nm wide. After that, a thin In layer of nominally 16 nm thick was deposited by using thermal evaporation. After standard lift-off procedure, a narrow stripe of In layer of ∼100 nm wide was left along the truncated terrace edge lines. To grow IPSLS SiNWs, the prepared samples were loaded into a plasma-enhanced chemical vapor deposition (PECVD) system and treated with H_2 plasma at 250 °C to remove the oxide layer on the In catalysts; then the reduced indium (In) atoms will diffuse on the surface and agglomerate into droplets. So, the size of the In droplet is determined by, or proportional to, the collection zone area around a nucleation site, separated by the typical diffusion length of the In atoms λ_{In} at least during its initial stage. Figure 2e−h shows the typical SEM overview and three representative locations, that is on the planar bottom surface (marked by red), on the oblique terrace edge (marked by blue), and on the top flat edge (marked by green).

Compared to the random In droplets formed on the planar bottom surface (Figure 2f), with a dispersive diameter distribution of 63 ± 38 nm (see the red marks in Figure 2d), a uniform catalyst formation has been observed on the terrace edge lines; particularly, a very impressive single-row-droplet arrangement was achieved on the top flat edge, with a diameter of 89 ± 5.7 nm (Figure 2h). Interestingly, the droplet formation on the oblique terrace edges seem to be strongly regulated by the narrow multisteps, with only 1−2 nano-droplets sitting on each step (see Figure 2g) and a diameter variation of 86 ± 8 nm. We also found that the diameter of droplets formed at the edge-ends was found to be 92 ± 14 nm with a thicker In layer of 32 nm (see Figure S1 in the Supporting Information), which is very close to the width of the mini-step edge of W_{step} = 100 nm. But these large droplets are also prone to get in touch with their neighbors and merge into a thicker SiNWs during the subsequent IPSLS growth. This finding indicates that the edge-trimming of photoresist provides a rather efficient way to define narrow stripes of In catalyst, which is beneficial for achieving uniform-sized catalyst formation, without the need of high precision and expensive lithography technology.

3.2. Confining Effect of Mini-steps on Droplet Uniformity. To better understand the confinement effect of the width of mini steps (W_{step}) on catalyst droplet formation, a series of different W_{step}, ranging from 300 to 100 nm, were prepared by controlling the O_2 plasma edge etching time, while keeping a constant edge-trimming width or the In stripe width W_{str} of 100 nm. As shown in Figure 3a−c and the corresponding statistics in Figure 3g−i, reducing the width of the mini-steps can help to impose an additional spatial confinement on the In droplet formation, that is, along the edge lines (y-direction). For example, along the flat edge line found on top of the terrace, the In droplets have a diameter of 108 ± 8 nm (Figure 3g). On the wider oblique terrace steps, with width W_{step} of 300 nm (Figure 3b), 2−3 In droplets were found on each step, with a diameter of 105 ± 11 nm (Figure 3h). When the W_{step} is scaled down to 100 nm, as seen in Figure 3c, only a single In droplet is found on each mini-step, with a rather uniform diameter of 67 ± 5 nm (Figure 3i). Note that this single-row and one-droplet-on-one-step catalyst distribution is exactly what we need to achieve a deterministic size and position control of the IPSLS growth of the SiNW array but has remained extremely difficult to accomplish due to the initial random formation of catalyst droplets.

Similar to the catalyst droplet formation on the nanostripes patterned by EBL[45], when the In adatoms were evaporated and landed on the terrace surface, they diffused on the empty surface until they collide to form stable nuclei. Then, more

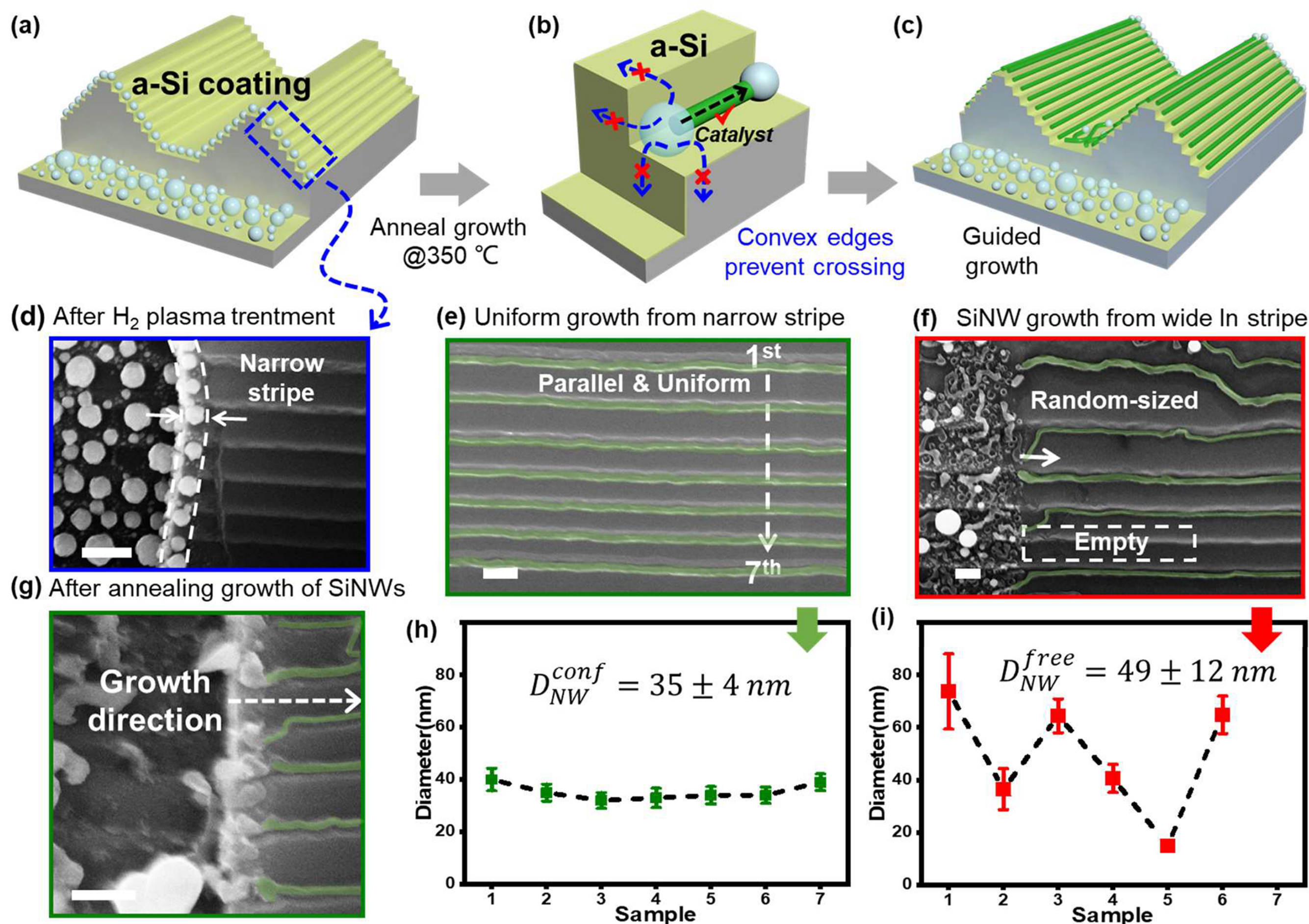

Figure 4. (a) Uniform growth of thin SiNWs, led by the discrete In droplets (as seen for example in the SEM image shown in panel d, with discrete In droplets formed on the trimmed edge after H_2 plasma treatment, prior to the growth of SiNWs), along the mini-steps on the oblique terraces, after coating a-Si precursor layer and annealed growth via an IPSLS growth mode. (b) The In droplet, sitting on a mini-step and close to the truncated cliff edge, has 4 different moving directions to go across the convex edge lines, plus 1 guided growth direction following the extension of the mini-step. (c) Orderly SiNW arrays, with uniform diameter, grown along the guiding min-steps, with close SEM image of the as-grown SiNWs shown in panel e, compared to the SiNWs with large diameter variation grown with wide In stripe that is without edge-trimming and thus large size dispersion of the In droplets. (f) The SEM image of SiNWs grown from wider catalyst stripe (>2 μm). (g) SEM image of the initial kick-off locations of the SiNWs, which all preferred to grow along the guiding direction of the mini-steps. (h and i) Diameter statistics of the as-grown SiNWs, found at different mini-step level numbered as 1 to 7 from top to bottom [see the labels in panel e], with and without the use of the edge-trimming catalyst confinement technology, respectively. Scale bars here are all for 200 nm.

adatoms continue to arrive and become trapped by the nearest nuclei if they fall within the surface collection zone, which is roughly measured by the diffusion length of an In adatom λ_{In}. Therefore, on the planar surface, the collection area can be expressed as $S_{ad_planar} \sim d_s^2 \sim 4\lambda_{In}^2$, where $d_s \sim 2\lambda_{In}$ is the separation between the initial nucleation sites.

For the catalyst droplet formation on the top flat edge lines (see those found along the edge in Figure 3a), the surface diffusion of In adatoms is restricted within a confined on both sides, that is, by the photoresist boundary and the truncated cliff (convex edge) in the x-direction. This thus suppresses the random distribution of the initial nucleation sites, confining them into a narrow stripe with smaller collective region of the adatoms, with $W_{str} < d_s$, which also help to achieve a narrower size dispersion of the as-formed In droplets, as witnessed indeed in Figure 3a, compared to those found in Figure 2f. However, on this top flat edge, there is no confinement imposed in the lateral y-direction, which is a challenging issue for achieving precise alignment of the droplets to the guiding mini-steps. Ideally, the catalyst droplets should be assigned one-by-one to each ministep, for the subsequent growth of a dense parallel SiNW array.

Fortunately, the additional y-direction confinement can be applied naturally on the oblique mini-steps, given a small enough step width. For instance, on the wide mini steps of 300 nm wide, approximately $W_{step} \sim d_s = 4\lambda_{In}$, the droplet formation was only loosely confined in the y-direction (see Figure 3e), and thus two or more droplets can be formed on each mini step. With a tighter confinement established in the lateral y-direction, that is reducing $W_{step} < d_s = 2\lambda_{In}$ to ∼100 nm, all In adatoms landed on the a small regular square pad can diffuse and merge into a single site of droplet, sitting at the end of each step, as depicted schematically in Figure 3f. More importantly, combining the confinement effects of the terrace-steps and the edge-trimming stripe enables also a precise mass, and thus size, control of each discrete In catalyst droplets, as now the total amount of In adatoms received by each square pad, as highlighted in Figure 3f, is tightly limited to $D_{In_stp}^3 \sim W_{str}W_{step}t_{In}$. Note that all of these dimensional parameters can be easily tuned to establish eventually a deterministic position

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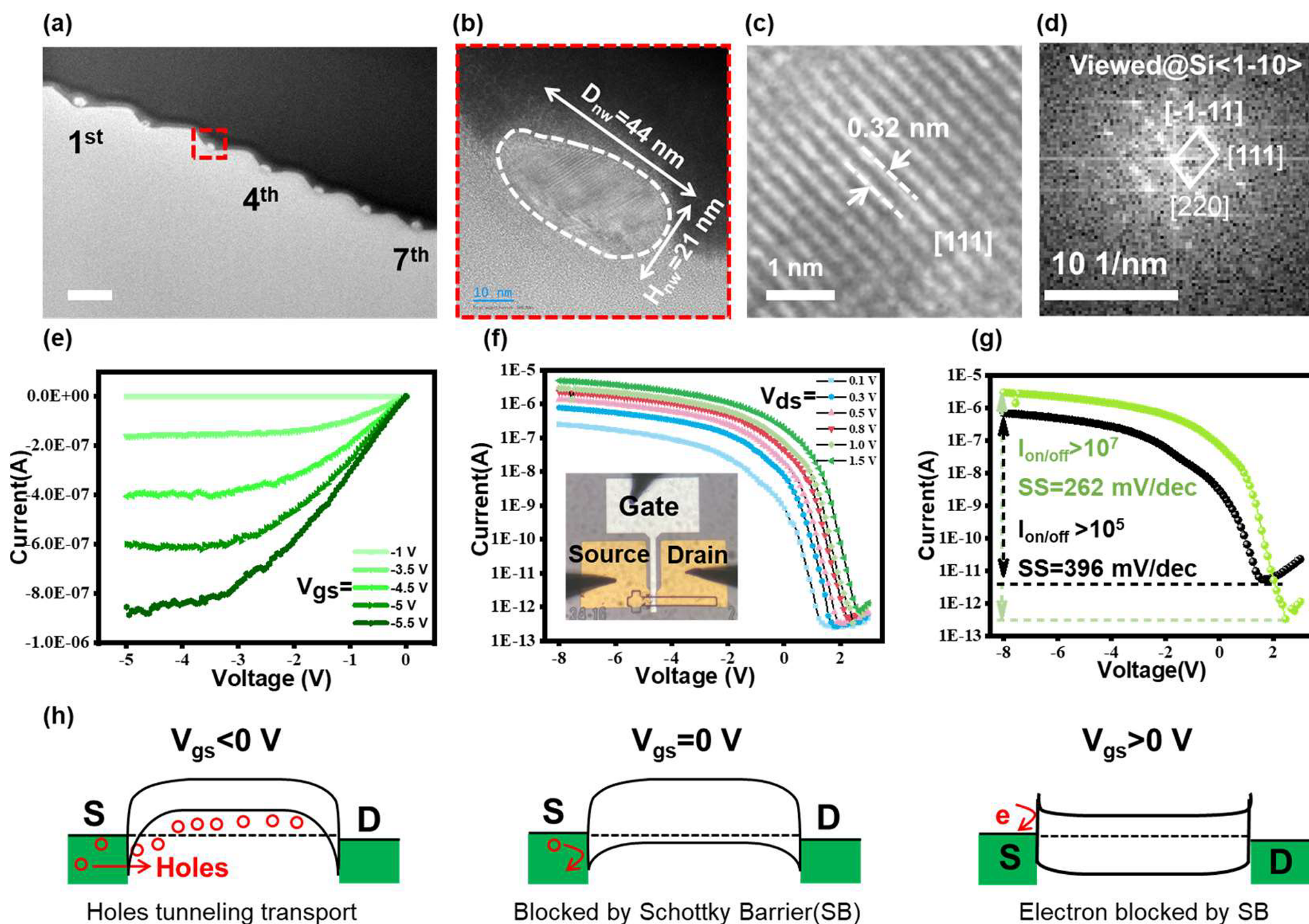

Figure 5. (a−d) The cross-section structural analysis of 7-layer SiNWs grown on oblique terrace mini-steps. (e and f) Output and transfer curves of the tunneling Schottky barrier FET (SB-FET) devices, fabricated on the uniform SiNW arrays, with a photo of the FET electrode layout in insert in panel f. (g) Typical transfer curves of SB-FET devices fabricated on the uniform (green curve) and random (black curve) SiNW arrays. (h) Illustration of the hole tunneling transport band profiles in the SB-FET device under different gating bias conditions.

and size control of the In droplets, which is a prerequisite for achieving uniform growth integration of SiNW-based electronics.

3.3. Uniform Growth of Orderly SiNW Array. The well-positioned In catalyst droplets were employed to grow orderly and dense array of SiNWs, via the IPSLS mode, where the SiNW diameter is known to be proportional to the leading In catalyst droplets, with $D_{nw} \sim f\, D_{In}$.[46] After the edge-trimming step, nominally 16 nm thick In film was deposited and lift-off as described above, with optimized $W_{str} \sim W_{step}$ = 100 nm. After that, the samples were loaded into a PECVD system and treated by H_2 plasma to form single-row and discrete catalyst droplets, as diagrammed and seen for example in the close view shown Figure 4a and 4d, respectively, followed by the deposition of an a-Si thin film by SiH_4 plasma at 100 °C (Figure 4a). Upon raising the temperature to 350 °C and annealing in a vacuum, the In droplets were activated to absorb the nearby a-Si thin film and move along the guiding mini-steps to produce aligned SiNWs. It is interesting to note that, for the In droplet sitting on a mini-step and close to the truncated cliff edge, it has 4 different moving directions to go across the convex edge lines, as marked in Figure 4b, plus 1 guided growth direction following the extension of the mini-step. As pointed out in our previous work,[47] the convex edge-crossing growth is not the most energetically favorable, as they usually lead to a shortage of a-Si supply, compared to the smoother guided growth along the straight mini-steps. Therefore, this helps to establish a beneficial fencing mechanism that enforces the growth of the individual In droplets to grow into the desired guided directions, as indeed observed in the experiments. For instance, Figure 4g and 4e show respectively the enlarged SEM characterizations of the growth kicking-off place at the truncated edge, and in the stabilized middle guiding places. In addition, the truncated cliff also prevented the growth of other SiNWs from the lower bottom (the left part in Figure 4g) to the top ministeps due to the insufficient a-Si supply on the vertical cliff sidewall (Figure S2). Though guiding IPSLS growth has been known in our previous work, adding the convex cliff-edge is the key to push or enforce the droplet to grow always into the right direction, which is a new powerful control and has never been reported ever. As a result, compared to relatively random sized SiNWs grown on the same ministeps but without the use of edge-trimming technology, the diameter dispersion of the SiNWs can be greatly suppressed, as witnessed in the corresponding statistics summarized in Figure 4h and 4i. Specifically, for the SiNWs grown on different mini-steps, labeled 1−7 from top to bottom, the edge-trimming technology can help to produce rather uniform thin SiNWs with diameter of D_{nw} = 35 ± 4 nm, 100% growth filling rate (Figure 4h). In contrast, the SiNWs

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grown with wider catalyst stripe (>2 μm) (Figure 4f) has a much larger diameter variation of D_{nw} = 49 ± 12 nm (Figure 4i). Note that the thinnest diameter of SiNWs grown stably on the terrace guiding edge is around 13.7 nm (Figure S3) when the diameter of leading catalyst droplets decreases to ∼40 nm at the edge-ends of the truncated guiding terrace, by reducing the In thickness to 13 nm and controlling the In pad width to ∼80 nm.

3.4. As-Grown SiNW Channels and FET Devices. The crystallinity of the as-grown SiNWs were also examined by using high resolution transmission electron microscopy (HR-TEM) of a terrace with 7-layer SiNW array, cut by focused ion beam milling (as shown in Figure 5a). Close HR-TEM examinations in Figure 5b and 5c reveal that the SiNWs are mostly ellipsoidal in cross section, with a shorter height of H_{nw} ∼ 21 nm and a wider width of D_{nw}∼ 44 nm, showing coherent crystalline lattice with clear fringe spacing of d = 0.32 Å, corresponding to that of Si[6] planes, and a preferential growth orientation of Si <110> as seen in Figure 5d. Note that the ellipsoidal cross section of the as-grown SiNW is related to the fact that all of the precursor supply comes from the surface-coating amorphous thin film (a-Si), and thus, the droplet will tend to deform in that way, drawn by the front absorption interface, to contact more a-Si during its planar growth movement.

A simple prototype FET device was also fabricated to testify the electronic transport property of the SiNW channels, a column of 7-layer-steps SiNWs, with an average diameter about 24 nm, was chosen and connected by a pair of composite Pt (5 nm)/Al (50 nm) source/drain (S/D) electrodes, defined by conventional lithography as diagrammed in Figure S4, with a channel length of ∼2 μm. After that, a thin Al_2O_3 dielectric layer of 25 nm thickness was deposited by using atomic layer deposition (ALD), followed by the preparation of a 60 nm Al side-gate electrode. This thus formed a top-gated configuration with a photograph of the final device layout presented in the inset in Figure 5f. The output and transfer characteristics of the as-fabricated FET are provided in Figure 5e−5g, showing a high $I_{on/off}$ ratio >10^7 and subthreshold swing (SS) of 262 mV dec^{-1} (green curve in Figure 5g). For comparison, the FET fabricated by random SiNW arrays (black curve in Figure 5g) showed only an $I_{on/off}$ ratio >10^5 and high SS of 396 mV dec^{-1}. Since the off current and SS performances of the FET device are highly dependent on the diameter of the SiNW channel, considering the influence of Debye screening on the control of mobile charge carrier in the semiconductor channel,[48,49] the current in the thin channel is easier to close than that in the large and random channel diameter. This can also be experimentally demonstrated by the performances of FET device fabricated by using thicker SiNW arrays with diameter of ∼45 nm and ∼100 nm in Figure S5, with $I_{on/off}$ ratio >10^5 and high SS of 320 mV dec^{-1}. Therefore, thanks to the thin and uniform SiNW obtained by the new edge-trimmed approach, the I_{off} and SS of the fabricated FET device can be obviously reduced. These findings and knowledge are also very important for establishing catalytic SiNWs as competitive channels for high performance thin film electronics. It has been known that the dissolution of In atoms into the SiNWs gives rise to a p-type doping with an equivalent B-doping of ∼10^{18} cm^{-3}.[50] The I_{ds}−V_{ds} characterization is in Figure S6 indicated that the Pt/Al electrode contacts to the as-grown p-type SiNWs formed typical Schottky barrier (SB) junctions, with a band gap alignment profile as depicted schematically in Figure 5h (under V_{gs} = 0 V). Therefore, a pair of such SB junctions connected back-to-back in serial fashion blocked the transport of hole carriers under positive V_{gs} ≥ 0 V gating biases. In contrast, when a negative gating voltage is applied, a significant amount of holes are accumulated in the p-type SiNW channels, causing a thinning of the SB that will allow the holes to easily tunnel through the triangle barriers and to turn ON the transport state.

4. CONCLUSIONS

In summary, a new edge-trimming catalyst formation strategy has been established in this work, which can help to achieve an unprecedented uniform size and precise location control of the leading catalyst droplets, as a critical basis to batch produce 100% guided, dense, and thin crystalline SiNW, with D_{nw} = 35 ± 4 nm. It was found that catalyst deposition and droplet formation can be precisely controlled by convenient tuning of W_{step} and W_{str}. Note that all these have been accomplished via large-area compatible fabrication processes, and this has never been demonstrated before, providing a solid basis for the construction of integration of high-performance SiNWs based electronic logics and sensor applications.

■ ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge at https://pubs.acs.org/doi/10.1021/acsami.4c03991.

SEM image of formed droplets on the guiding terrace (W_{step} ∼ 100 nm) with the In thickness of 32 nm; schematic illustration of SiNW growth led by under catalyst droplets; the thinnest diameter of SiNWs grown on the terrace guiding edge is around 13.7 nm when the diameter of droplets down to ∼40 nm, by reducing the In thickness to 13 nm and controlling the In pad width to ∼80 nm; schematic illustration of fabrication process of SiNW-FET device; the transfer characteristics of the FET devices fabricated on the planar SiNW arrays with diameter of ∼24 nm, ∼45 nm, and ∼100 nm.; and the I_{ds}−V_{ds} characterization of the SiNW FET using Pt/Al as the S/D electrodes, which indicated a typical Schottky barrier (SB) junctions (PDF)

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Notes

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■ ABBREVIATIONS

SiNWs, silicon nanowires; In, indium; IPSLS, in-plane solid−liquid−solid; FETs, field effect transistors; EBL, electron beam lithography; EUV, extreme ultraviolet; VLS, vapor−liquid−solid; TFTs, thin film transistors; PR, photoresist; PECVD, plasma-enhanced chemical vapor deposition; W_{step}, width of mini steps; HR-TEM, high resolution transmission electron microscopy

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