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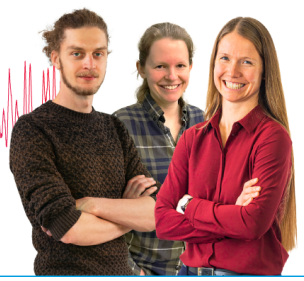

Diameter scaling limit of catalytic silicon nanowires confined by optimized ultrafine sidewall grooves

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ABSTRACT

The fabrication of quasi-one-dimensional silicon nanowires (SiNWs) with ultrathin diameters below 10 nm is crucial for enhancing field-effect control in state-of-the-art transistors and is beneficial for building high-performance optoelectronics and biosensors. In this study, we explore the limits of diameter control during the catalytic growth of SiNWs by using an in-plane solid–liquid–solid (IPSLS) mechanism, where SiNWs are guided and confined within narrow sidewall grooves. To achieve tighter growth confinement, a selective etching strategy was developed to produce stable and significantly finer guiding grooves, with heights, depths, and pitches of 15, 16, and 10 nm, respectively. Notably, this innovative groove design enables the production of parallel arrays of ultrathin, monocrystalline-like SiNWs, achieving critical cross-sectional dimensions smaller than 6 nm in one direction or less than 10 nm in both directions. Additionally, we propose a driving-energy-parity model that establishes a lower-bound diameter limit for IPSLS-grown SiNWs at approximately 2.5–4.2 nm. This finding indicates that further dimensional scaling remains feasible by employing even finer sidewall grooves. These results underscore the potential for scaling down ultrathin SiNWs, which is vital for exploring high-performance microelectronics based on a catalytic growth integration strategy.

Ultrathin quasi-one-dimensional crystalline silicon nanowires (SiNWs), with a critical dimension (CD) below 10 nm, as illustrated in Fig. 1(a), are essential components for the development of next-generation microelectronics, sensors, logic devices, memory elements, and charge qubits.[1–5] Their unique physical properties, including an exceptionally high surface-to-volume ratio[6] and quantum confinement effects,[7,8] make them ideal candidates for these applications. Ultrathin SiNWs have garnered significant attention for the fabrication of cutting-edge high-performance field-effect transistors (FETs), with faster speed, reduced power consumption, and higher integration density.[9–12] Indeed, reliable fabrication and integration of such delicate c-Si channels with CD < 10 nm represents one of the most critical challenges. Conventional top-down approaches, by using extreme ultraviolet (EUV) lithography[13,14] as depicted in Fig. 1(b), electron beam or helium ion beam lithography,[15,16] or multi-step self-aligned quadruple patterning (SAQP),[17,18] are facing increased complexity and costs. Alternatively, bottom-up catalytic growth techniques like the vapor–liquid–solid (VLS) method,[19,20] as shown in Fig. 1(c), or the metal-assisted chemical etching (MACE) based on the silicon wafer,[21,22] offer cost-effective and promising alternative routes for synthesizing ultrathin SiNW channels. However, these SiNWs are usually obtained as randomly oriented vertical bundles,[23,24] and need to be individually transferred and arranged onto planar substrates to serve as ultrathin 1D channels. These, thus, pose a fundamental challenge to achieving a scalable and high-precision integration of various SiNW-based microelectronics.

In comparison, the in-plane solid–liquid–solid (IPSLS) mechanism, employing metallic droplets to consume an amorphous Si (a-Si) thin film to produce planar crystalline SiNWs, enables a directional guided growth of SiNWs into desired locations along predefined edges.[25–27] In pursuit of a stronger guiding confinement and further scaling of the IPSLS SiNWs, narrow guiding grooves can be formed on a planar surface by using electron beam lithography (EBL)[28] or the vertical sidewall of an SiN_x/SiO_2 superlattice.[29] The latter one, with fabrication steps illustrated in Fig. 1(d), is particularly attractive as it exempts the use of sophisticated EBL patterning and has demonstrated

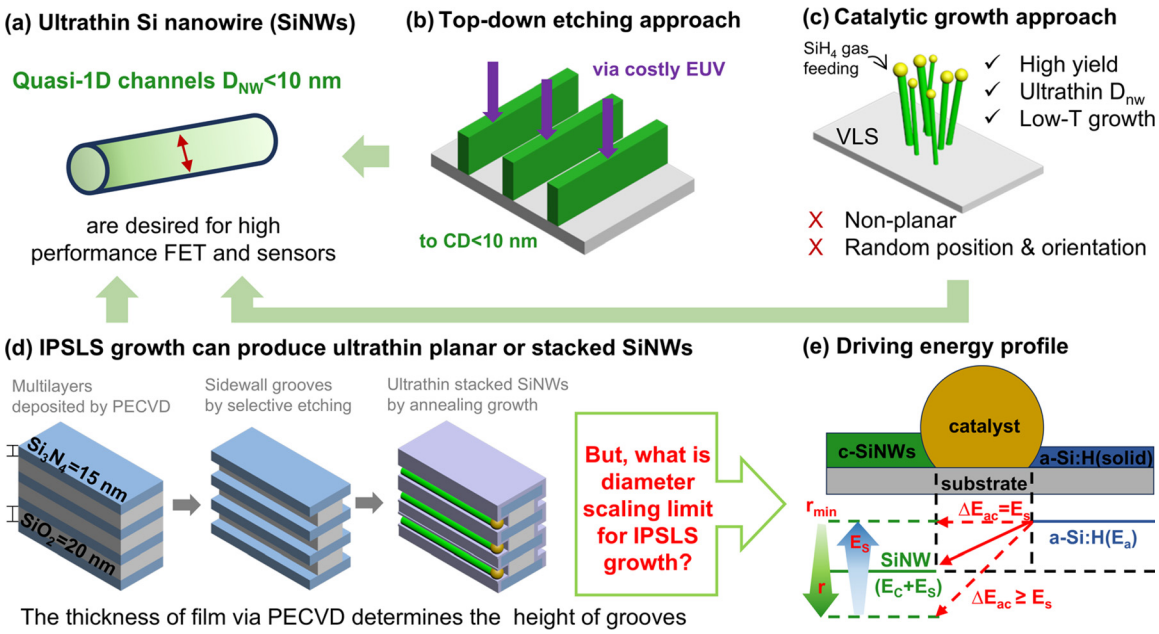

FIG. 1. (a) Schematic diagram of an ultrathin SiNW. (b) Fin structures patterned by the top-down techniques. (c) Vertical or randomly oriented SiNWs via a VLS growth approach. (d) The fabrication steps of ultra-confined 3D stacked SiNWs via IPSLS growth approach. (f) Schematic diagram of the driving-energy-parity model for IPSLS-grown SiNWs under ideal conditions.

the growth of 10-layer stacked ultrathin SiNW with CD approaching sub-10 nm.[29] Recently, high-performance GAA or planar FETs have been fabricated based on the IPSLS-grown catalytic SiNW channels.[30,31] However, there still remains an intriguing question regarding the fundamental diameter scaling limit of the IPSLS SiNWs, which is highly relevant for the catalytic SiNWs to fulfill their potential in high-density integration and high-performance FET applications. Though, in principle, a thinner SiNW diameter should be achieved by reducing the heights or widths of the guiding grooves, this straightforward scaling down encounters two primary challenges: (1) how to fabricate such intricate sidewall grooves to confine the growth of ultrathin SiNWs with critical dimensions (CD) less than 10 nm, considering that the structural stability of the protruding ultrafine groove edges also decreases with this aggressive scaling; and (2) whether a fundamental limit exists for the diameter scaling of IPSLS SiNWs.

In order to address these questions, we here explore an alternative sidewall groove etching technique that guarantees a more stable formation on the vertical sidewalls. Then, based on these optimized ultrafine sidewall grooves, ultrathin SiNWs with a single dimension smaller than 6 nm or near-circular cross section SiNWs with both lateral and longitudinal dimensions less than 10 nm have been fabricated. Furthermore, we propose also a driving-energy-parity model for the IPSLS growth of SiNWs, as illustrated in Fig. 1(e), which puts a lower-bound limit of the diameter scaling to around 4 nm.

As diagrammed schematically in Fig. 1(d), the sidewall grooves are etched out of a stacked multilayer of SiO_2 and Si_3N_4 thin films, with layer thicknesses of $t_O = 20$ nm and $t_N = 15$ nm, respectively, which are deposited upon a c-Si wafer substrate with a 500 nm thick SiO_2 by using alternating precursor gases plasma in a plasma-enhanced chemical vapor deposition (PECVD) system. Then, the sidewall positions are defined by conventional photolithography, followed by vertical etching using inductively coupled plasma (ICP), leaving a truncated vertical sidewall. After that, a buffered oxide etchant (BOE) solution has been used in our previous works[29] to selectively erode the exposed SiO_2 layer (BOE etches SiO_2 at a rate approximately 8–10 times faster than that of Si_3N_4 (Refs. 32 and 33)] and to form sidewall grooves with a depth controlled by etching duration. However, during the groove-forming etching step, the BOE also erodes the Si_3N_4 layer, leading to a significant thinning of protrusive wall/or spacer layers, as illustrated in Fig. 2(a) and witnessed in a series of scanning electron microscope (SEM) images shown in Figs. 2(b)–2(d). For example, the outer edge of the spacer layer becomes only 7 nm thick after only 1 min BOE treatment, which is too fragile and prone to collapse during the wet etching process.

To address this issue, we turned to explore another complementary etching approach, by using a more selective etchant of phosphoric acid (PA) that will etch off SiN_x, instead of the SiO_2 layer, with a much higher etching selectivity ratio of 50:1 for the Si_3N_4/SiO_2 etching rate.[34] Here, an 85% hot PA solution is used to etch only the Si_3N_4 layer, while preserving very well the protrusive SiO_2 spacer layer with uniform height and depth controlled by etching duration. As seen in the SEM images of the SiN_x-etched sidewalls shown in Fig. 2(h), where the edge thickness of the sidewall grooves remains basically the same as the designed layer thickness of $t_O = 20$ nm.

On the contrary, it is important to note that the pre-etching annealing of the multilayer stack is also a critical control parameter as illustrated in Fig. 2(e). For example, if the annealing temperature is decreased from 750 to 550 °C, the groove edge thickness also decreases to 13 nm (annealed @550 °C), as shown in Fig. 2(f), leading to similar unstable sidewall-layer collapse after the hot PA wet etching. This

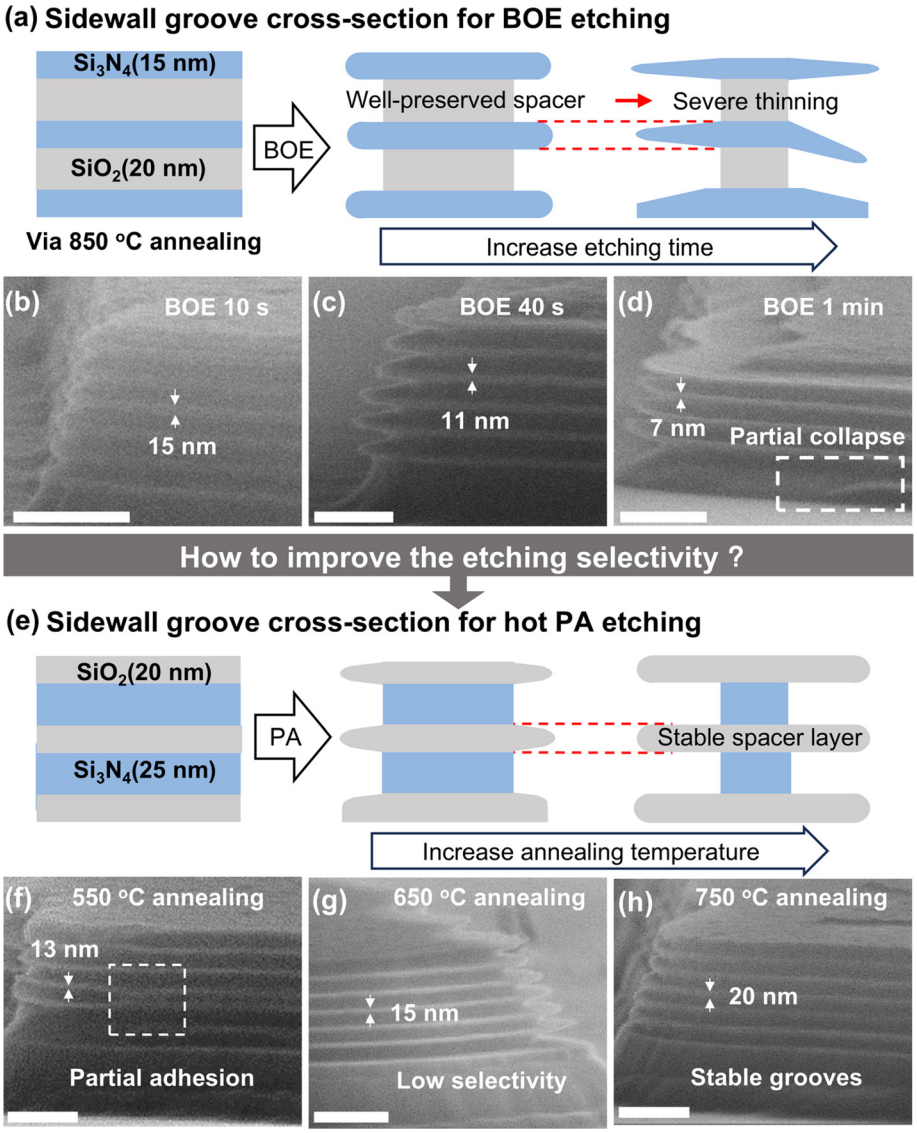

FIG. 2. (a) Schematic illustration of sidewall SiO_2 grooves with low aspect ratio by increasing BOE etching time. (b)–(d) SEM images of the sidewall Si_3N_4 layers after BOE solution erosion for 10 s, 40 s, and 1 min, respectively. (e) Schematic illustration of sidewall Si_3N_4 grooves exhibiting gradually stable space layer with increasing annealing temperature. (f)–(h) SEM images of the sidewall Si_3N_4 grooves with different annealing temperatures of 550, 650, and 750 °C, respectively. Scale bars in (b)–(d) and (f)–(h) are all for 200 nm.

phenomenon can be attributed to the higher stress and defect density in the as-deposited SiO_2 films, and a higher concentration of hydrogen in the stacked layers,[35,36] which leads to an accelerated etching rate of the oxide layer and thus a reduced selectivity ratio. Therefore, a high-T annealing @750 °C can be effective in achieving stable grooves. Furthermore, the PA temperature impact on the etching selectivity is also examined for the optimized stacked SiO_2/SiN_x multilayers annealed @750 °C. As shown in Fig. 3(a), for a constant etching duration of 7 min, the groove depth increases with increased temperature. This indicates that the etching rate of Si_3N_4 in hot PA is accelerated with increased temperature, but unfortunately accompanied by a decrease in the etching selectivity ratio, as witnessed in the SEM image of a sample etched@150 °C. Conversely, lower etching temperatures yield an excellent selectivity ratio but come with a slower etching rate. Seeking a trade-off between the etching rate and selectivity, the PA etching temperature has been fixed to 140 °C in the following experiments.

As illustrated in Fig. 3(b), with 85% hot PA etching @140 °C, the Si_3N_4 layer can now steadily recede linearly with the increased etching time, leading to a well-controlled groove depth, while preserving the SiO_2 spacer thickness basically unchanged, which can be seen from the SEM images in Fig. 3(c). According to the statistics shown in Fig. 3(d), the groove depth is indeed proportional to the etching duration, with a receding/etching rate of approximately 5.5 nm/min. This linearity, as well as the groove structure integrity, is a crucial basis for implementing tighter guided growth confinement of ultrathin SiNWs within the ultra-narrow sidewall grooves.

Based on the optimized SiN_x-etching strategy, even thinner guiding grooves have been fabricated with an ultrafine stacked layer thickness of Si_3N_4: SiO_2 = 15 nm: 10 nm, which results in ultrafine sidewall

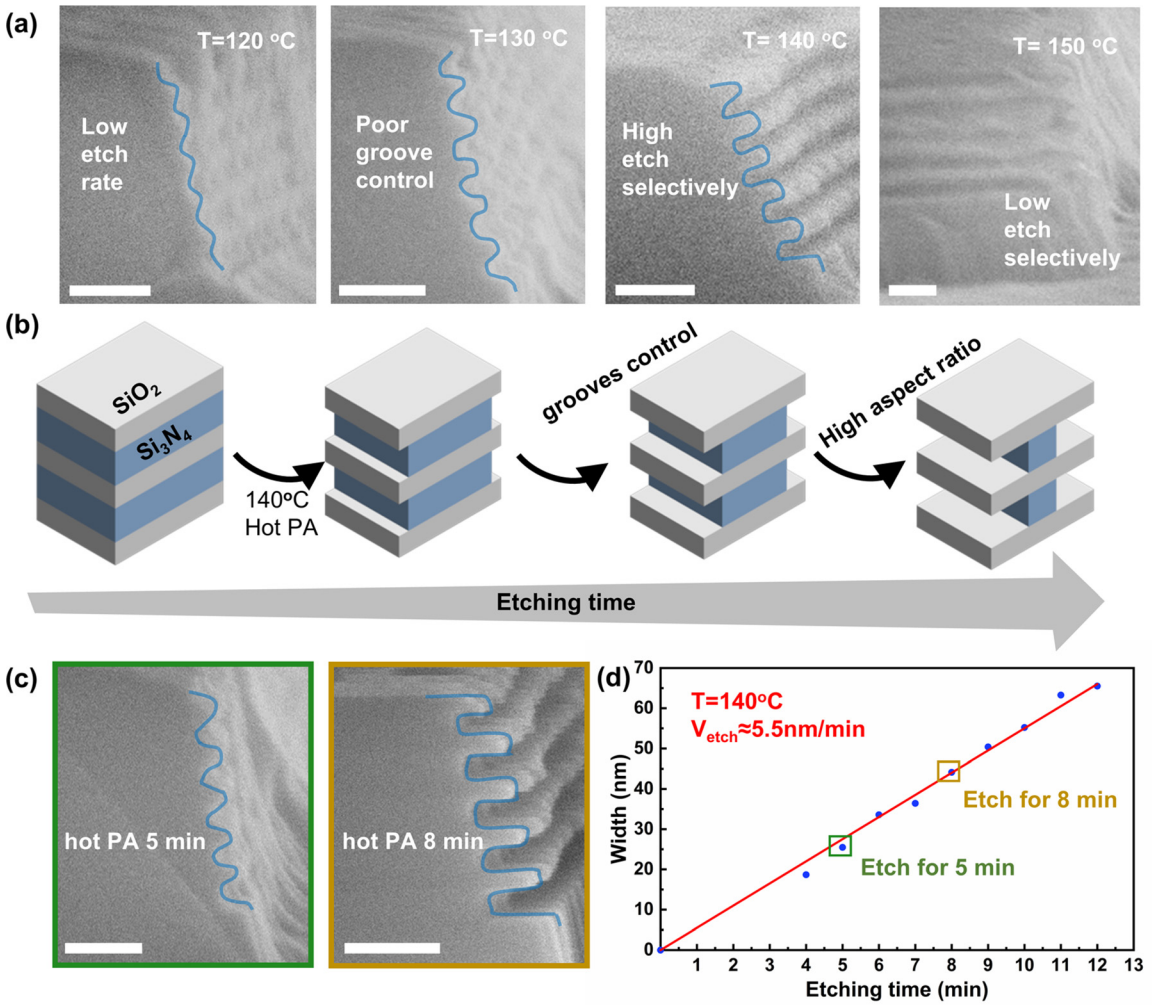

FIG. 3. Sidewall Si_3N_4 groove formation. (a) SEM images of the sidewall grooves etched for 7 minutes in hot PA at temperatures of 120, 130, 140, and 150 °C, respectively. (e) Schematic illustration of steadily increasing groove width while barely etching the spacer layer. (c) SEM images of the sidewall grooves etched for 5 and 8 minutes, respectively, in hot PA at 140 °C. (d) A linear plot showing the relationship between groove width and etch time. Scale bars in (a) and (c) are all 100 nm.

grooves with dimensions of $W_g \times H_g \approx 16\ (\pm 2)\ \times 15\,nm^2$. Then, a nominally 3 nm thick indium (In) layer is patterned and deposited at one end of the vertical grooves with a tilted incident angle of 60°, and then treated by H_2 plasma at 250 °C in a PECVD system to reduce the surface In_2O_3 oxide layer and form discrete In droplets, followed by the coating of a thin precursor a-Si: H film over the sidewall grooves by using SiH_4 plasma at 150 °C (below the melting point of In droplets). Figure 4(a) shows an SEM image of the resulting In droplets sitting at the ends of sidewall grooves before the growth of SiNWs. Due to the angular evaporation of the ultrathin In film, the sidewall grooves can help to further separate the In layer into discrete droplets on the protruding sidewalls. To kick off the IPSLS growth, a low-temperature annealing in vacuum is carried out at 350 °C, where the droplets become molten again and start to move forward along the sidewall grooves, absorbing the a-Si to produce crystalline SiNWs sitting or confined within the ultrafine sidewall grooves, as seen in Fig. 4(b), where the SiNWs grown within grooves are highlighted in green. Note that, for these tightly confined IPSLS growth within sidewall grooves, the ultrafine SiNWs can grow over a length of typically >3.5 μm, as measured from direct SEM observations. More theoretical and experimental details of the IPSLS growth and fabrication procedures are available in our previous works.[29,37]

High-resolution transmission electron microscopy (HRTEM) cross-sectional analysis, as shown in Fig. 4(c), reveals that monocrystalline SiNWs are present within the lower sidewall grooves. In contrast, adjacent grooves without SiNW growth maintain the coating or filling profile of the a-Si: H layers (pseudo-colored yellow), which is intentionally preserved to showcase the growth environment and can be selectively removed after the SiNW growth.[29] Notably, the magnified HRTEM image in Fig. 4(d) shows that the SiNW observed in the 5th layer grows along the Si ⟨011⟩ direction and exhibits a rounded rectangular shape with both height and width measuring approximately 9.1 nm. This represents the thinnest IPSLS SiNW reported to date with all dimensions confined below 10 nm critical dimension

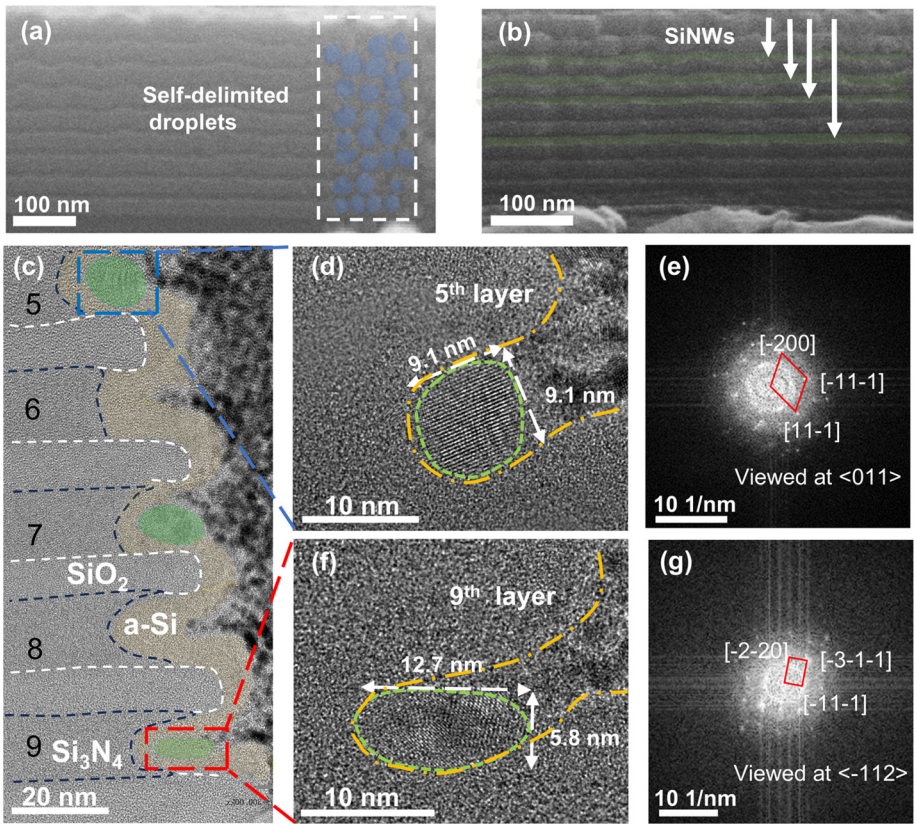

FIG. 4. (a) and (b) The SEM images of the self-delimited Indium droplets coated by a thin precursor a-Si: H film on the sidewall and the as-grown SiNWs, respectively. (c) The cross-sectional TEM image of the SiNW stacks, where the residual a-Si and NWs are tinted yellow and green, respectively. (d)–(f) Enlarged TEM views of NW on the 5th and 9th layers, respectively, where the edges of a-Si and SiNW are yellow dashed and green dashed. (e)–(g) The corresponding electron diffraction pattern of SiNWs on 5th and 9th layer.

(CD). Meanwhile, it is interesting to note that, with a gradual decrease in the groove height, from the top 5th to the bottom 9th grooves, the SiNWs are also squeezed to become lower and wider, with an increased aspect ratio from $r_{nw} = W_{nw}/H_{nw} = 1$ to 2.1. Particularly, a rather thin height of $H_{nw} = 5.8$ nm, with a width of $W_{nw} = 12.7$ nm, has been achieved in the bottom guiding groove as shown in Fig. 4(f). This reflects the unique capability of a growth formation of ultrathin SiNW with a tunable aspect ratio, which is a key capability to tailor the desired channels for future GAA-FET device fabrication.

However, two critical observations warrant further investigation and understanding. First, the growth orientation of the bottom-layer-situated squeezed SiNW was identified to be <211>, suggesting that aspect ratio control can influence the channel orientation of catalytically grown SiNWs. This phenomenon may be attributed to the varied interfacial environments experienced by the droplet/SiNW growth system within the varied groove confinement profiles. Second, the success rate of the guided SiNW growth within tightly confined grooves is only approximately 60%–70%, significantly lower than the near-unity filling rates observed for thicker SiNWs in our previous studies.[29] This discrepancy can be attributed to the suboptimal growth equilibrium conditions within the confined sidewall grooves. Therefore, optimizing these conditions—primarily by adjusting the a-Si thickness and the size of the In droplet—is expected to enhance the growth yield.

Here, it is intriguing to consider whether there exists a fundamental limit for diameter scaling during the IPSLS process. In this context, we propose a simple yet heuristic model based on driving-energy parity: according to the law of conservation of energy, the primary driving force for the IPSLS growth is the higher Gibbs free energy stored in the amorphous phase in a-Si precursor, over the as-grown crystalline phase in SiNW,[38,39] which is approximately $\Delta E_{ac} = 0.12$–0.15 eV/atom for the phase transition in bulk materials. As sketched in Fig. 1(e), the IPSLS growth should proceed as long as the atomic transition from the a-Si phase into the c-SiNW phase is energetically favorable, that's $\Delta E_{ac} > 0$.

However, with the down-scaling of the diameter of ultrathin SiNWs, the surface energy acting on the highly curved sidewall surface induces an ever-increasing inner pressure that increases the energy state of Si atoms in the crystalline SiNWs, which can be written as

$$E_s = P_s \Omega_{Si} = \frac{\sigma_{Si}}{r} \Omega_{Si}, \quad (1)$$

where Ω_{Si} is the atomic volume of Si and σ_{Si} the surface energy coefficient on crystalline SiNW, which is typically in the range of 1.5–2.0 N/m[40] depending on the surface facet orientation. So, there is at least a fundamental lower bound or limit for the diameter scaling of IPSLS SiNWs, that is,

$$\Delta E_{ac} > E_s \rightarrow r \geq \frac{\sigma_{Si}}{\Delta E_{ac}} \Omega_{Si} \text{ or } d \geq \frac{2\,\sigma_{Si}}{\Delta E_{ac}} \Omega_{Si} = 2.5 \sim 4.2\,\text{nm}. \quad (2)$$

It can be seen that there is still room for further scaling of the diameter of SiNWs to even < 4 nm, which is close to the exciton Bohr radius in c-Si.[41] It is noteworthy that this driving-energy-parity model also implicates that the growth of even thinner SiNWs is possible, considering that there are plenty of ways to raise the inner energy of the a-Si precursor layer (i.e., the driving energy), for example, by

adjusting the disorder, H_2 content in the a-Si layer, or by Ar/H_2 plasma treatment, as demonstrated in our previous works.

In summary, the diameter scaling limit of catalytic SiNWs, grown via IPSLS confined within ultrathin sidewall grooves, has been explored both experimentally and theoretically. A very stable and selective groove formation technology has been established to fabricate ultrafine guiding grooves with desired heights, depths, and pitches of 15, 16, and 10 nm, respectively. Then, monocrystalline-like ultrathin SiNWs have been obtained with cross-sectional dimensions <6 nm in one direction (or 9.1 nm in both directions), approaching or comparable to the top-down patterning resolution of the cutting-edge EUV lithography. In addition, a driving-energy-parity model has been proposed, which puts a lower bound on the diameter limit of IPSLS-grown SiNWs at approximately 2.5–4.2 nm, indicating that there is still room for further diameter scaling. These findings emphasize the critical diameter scaling capability of catalytic growth of SiNWs while also providing important guidance for the development of high-performance logics, optoelectronics, and biosensor applications.

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AUTHOR DECLARATIONS

Conflict of Interest

The authors have no conflicts to disclose.

Author Contributions

Mingyu Xie and Wentao Qian contributed equally to this paper.

Mingyu Xie: Data curation (equal); Formal analysis (equal); Investigation (equal); Methodology (equal); Visualization (equal); Writing – original draft (lead). **Wentao Qian:** Conceptualization (equal); Data curation (equal); Formal analysis (equal); Investigation (equal); Methodology (equal); Validation (equal); Visualization (equal); Writing – review & editing (equal). **Junzhuan Wang:** Data curation (supporting); Funding acquisition (equal); Investigation (equal); Writing – review & editing (supporting). **Linwei Yu:** Conceptualization (lead); Data curation (equal); Formal analysis (equal); Funding acquisition (lead); Investigation (lead); Methodology (equal); Project administration (lead); Resources (lead); Supervision (lead); Validation (equal); Visualization (equal); Writing – review & editing (lead).

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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