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Ultra-Confined Catalytic Growth Integration of Sub-10 nm 3D Stacked Silicon Nanowires Via a Self-Delimited Droplet Formation Strategy

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Fabricating ultrathin silicon (Si) channels down to critical dimension (CD) <10 nm, a key capability to implementing cutting-edge microelectronics and quantum charge-qubits, has never been accomplished via an extremely low-cost catalytic growth. In this work, 3D stacked ultrathin Si nanowires (SiNWs) are demonstrated, with width and height of W_{nw} = 9.9 ± 1.2 nm (down to 8 nm) and H_{nw} = 18.8 ± 1.8 nm, that can be reliably grown into the ultrafine sidewall grooves, approaching to the CD of 10 nm technology node, thanks to a new self-delimited droplet control strategy. Interestingly, the cross-sections of the as-grown SiNW channels can also be easily tailored from fin-like to sheet-like geometries by tuning the groove profile, while a sharply folding guided growth indicates a unique capability to produce closely-packed multiple rows of stacked SiNWs, out of a single run growth, with the minimal use of catalyst metal. Prototype field effect transistors are also successfully fabricated, achieving $I_{on/off}$ ratio and sub-threshold swing of >10^6 and 125 mV dec^{-1}, respectively. These results highlight the unexplored potential of versatile catalytic growth to compete with, or complement, the advanced top-down etching technology in the exploitation of monolithic 3D integration of logic-in-memory, neuromorphic and charge-qubit applications.

1. Introduction

Ultrathin quasi-one-dimensional crystalline silicon (c-Si) channels, with critical dimension (CD) <10 nm, are the key building blocks to construct the latest generation of microelectronics, sensors, and charge-qubits.[1–5] Up to date, a reliable fabrication and integration of such delicate c-Si channels can only be accomplished via state-of-the-art top-down technologies, such as the sophisticated electron (or helium ion) beam lithography,[6,7] the extreme ultraviolet (EUV) lithography,[8,9] or via a multi-steps self-aligned quadruple patterning (SAQP) processing backed with 193 nm immersion lithography.[10,11] In face of the exponentially soaring fabrication cost, accompanied with the shrinkage of CD, a complementary bottom-up catalytic growth that produces slim nanowires (NWs) via a layer-by-layer piling of atoms at the deposition interface of tiny catalyst droplets, seems to indicate a more efficient, high-throughput and low-cost alternative. However, despite of successful growth of ultrathin SiNWs with diameters of tens or several nanometers[12,13] and a plethora of electronics and sensor prototypes,[14–16] a reliable growth integration of the ultrathin c-Si channels into an orderly array, with CD control <10 nm and high uniformity, has never been achieved so far.

The advantages of a direct growth formation of such tiny SiNW channels, instead of etching, are manifold: First, this additive growth can help to avoid the top-down etching damages to the ultrathin channels; Second, a parallel growth of multiple vertically stacked SiNWs provides the beneficial channels for building the most advanced gate-all-around field effect transistors (GAA-FET, to be adopted in <5 nm technology nodes), as depicted schematically in **Figure 1**a–c, which can help to maximize the gate-channel capacitive coupling and achieve a much stronger electrostatic control[2,17–19] compared to the fin-gated FET[20,21] in use for <22 nm Node; Third, the low temperature catalytic growth (<450 °C) of SiNWs can be carried out upon foreign amorphous substrates, without the need of preexisting c-Si wafer as substrate, making it a promising candidate to achieve a monolithic 3D integration of multilayers of logic and memory units within a given footprint area, to push further the scaling limit[22–24] or implement more advanced neuromorphic and memory-in-computing functionalities.[25–27]

Built upon our previous works,[28–30] demonstrating the possibility of growing parallel SiNWs upon the vertical sidewall grooves via an indium (In) droplet-mediated in-plane solid-liquid-solid (IPSLS) mechanism,[31–35] we here develop a new self-delimited growth control strategy, which enables an ultra-confined and uniform growth of 3D stacked SiNW array, and thus an aggressive reduction of the width and height of the SiNW channels to W_{nw} = 9.9 ± 1.2 nm (down to 8 nm) and

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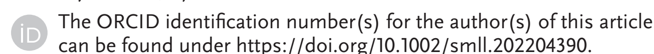
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H_{nw} = 18.8 ± 1.8 nm, respectively, on par with the CD control in 10 nm node. The key growth control parameters and the potential of channel cross-section engineering via a convenient groove profile design are also investigated and discussed.

2. Results and Discussion

2.1. Ultra-confined Growth on Sidewall Grooves

First, a N_{stk}-period stack of SiO_2/SiN_x multilayers was deposited by using conventional plasma-enhanced chemical vapor deposition (PECVD) system, followed by a vertical etching to expose the superlattice sidewalls. Then, ultrafine sidewall grooves were formed by a selective erosion of the oxide layers, against the more resistive nitride layers, via a buffered oxide etch (BOE) solution dipping. This treatment produced a concave groove cross-session profile, as indicated in Figure 1b, controlled by the etching depth t_{etch} and the amorphous SiO_2/SiN_x thin film deposition thicknesses of t_{dep_O}/t_{dep_N}. After that, In metal catalytic layer was evaporated onto the sidewall grooves, at different incident tilted angles θ_{in} (see Figure 1e). In the following steps, the samples were loaded into PECVD system and treated by using H_2 plasma to form discrete In droplets, prior to be coated with precursor a-Si:H layer and then annealed at a higher temperature of T_{grow} = 350 °C to activate the growth of SiNWs. During such an IPSLS growth process, the In droplets moved along the predefined sidewall grooves, while absorbing a-Si:H layer to produce crystalline SiNWs. More experimental details and discussion of the IPSLS growth mechanism are provided in the Supporting Information Section and in our previous works.[14,31,33,36,37]

As depicted in Figure 1f, the sidewall grooves provide not only a directional guidance, but also a strong means to the tailor their diameter and cross-section geometry of the as-grown and confined SiNWs. For example, a typical scanning electron microscopy (SEM) image of the SiNWs grown on the sidewall grooves is presented in Figure 1h with NWs tinted to light-green for the ease of observation, where the brighter spot found at the end of a SiNW is the leading In catalyst droplet,

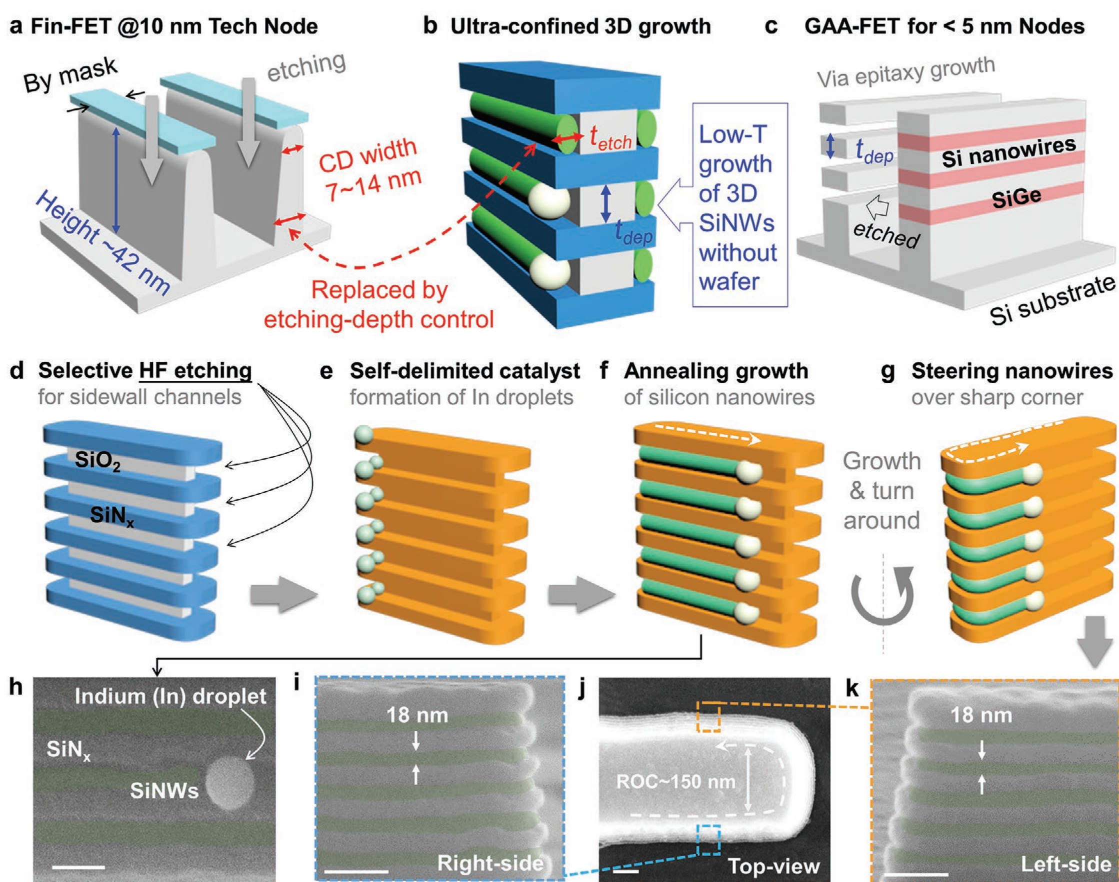

Figure 1. Ultra-confined 3D guided growth on sidewall grooves. a) Schematic illustration of a fin gate structure patterned by the top-down EUV and SAQP lithography and etching approach for 10 nm Node, where the CD is defined by mask resolution. b) Ultra-confined 3D growth of stacked NWs via a bottom-up IPSLS growth approach without the need for preexisting c-Si wafer, while the width and height are controlled by the etching depth of the groove and the deposition thickness of the SiO_2 layer, respectively. c) Advanced GAA-FET channels of stacked Si NWs for <5 nm Node, fabricated via Si/SiGe multilayer epitaxy, mask-defined channel width, and selective etching to form suspended SiNWs. d–g) The main fabrication steps for the groove-guided IPSLS growth integration of stacked SiNWs over a sharp turning 3D corner. h) SEM image of a SiNW led by an In droplet, where the SiNWs are pseudo-colored into light-green for the ease of observation. i–k) The continuous growth of uniform SiNWs over a turning corner track, with ROC of 150 nm. The scale bars in h-k stand for 100 nm.

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which is apparently wider than the SiNW, with $D_{In} \approx 1.8*H_{nw}$ approaching to the pitch of the SiN_x walls. Under proper growth balance control, requiring matched a-Si layer thickness and the In droplet size,[31 38,39] the SiNWs can be steadily confined within the sidewall grooves, which provides a new convenient and tunable strategy to translate the sidewall groove profile into the critical dimensions of the as-grown SiNWs. Specifically, as indicated in Figure 1b, the a-SiO_2/SiN_x layer deposition thickness (t_{dep}) and the subsequent etching depth (t_{etch}) are copied by the running In droplets to produce ultrathin c-Si channels of $H_{nw} \sim t_{dep}$ high and $W_{nw} \sim t_{etch}$ wide, without the need of the Si/SiGe multilayer epitaxial growth, SAQP/EUV patterning and selective etching steps, required in the formation of standard GAA-FET channel structures.[17]

More interestingly, the guiding sidewalls can be intentionally designed to fold, as diagrammed in Figure 1g, thus directing the growth of SiNW to travel around the bending corners continuously, and thus produce closely-packed array of stacked SiNW in parallel rows, each with enough channel length to devise individual FET units. An example is showcased in Figure 1i–k, where 5-layer stacked SiNWs, with uniform height of $H_{nw} \approx 18$ nm, were observed to grow around a ledge finger with a local radius of curvature (ROC) of only ≈150 nm. In this way, multiple rows of stacked SiNW channels are produced via a single-run growth of catalyst droplets, one droplet for each level/row, which also greatly enhances the uniformity of the SiNWs, with yet the least use of metal catalyst droplets for the construction of 3D stacked multi-channels needed in <10 nm Node FETs units.

2.2. Self-Delimited Catalyst Formation and Growth

To achieve a uniform growth of the SiNWs, the catalyst droplet formation on the sidewall grooves, with periodic protruding SiN_x walls and receding SiO_2 trenches, must be precisely controlled. In our previous work,[28] it was found that the SiO_2 trench layers should be ≈2 times wider than the thinner SiN_x walls, to effectively suppress the diameter fluctuations of the SiNWs grown in the neighbored grooves. However, this brings a challenge in pursuit of even thinner SiNWs. To grow SiNW with a diameter (H_{nw} or t_{dep_O}) <20 nm, the SiN_x wall layers need to be $t_{dep_N} \approx t_{dep_O}/2 < 10$ nm, which is difficult to guarantee the groove structure integrity during the selective HF etching to form the sidewall grooves, see for example the smeared grooves on the sidewall with $t_{dep_N} \approx 10$ nm design in Figure S1, Supporting Information. So, in this work, a new tilted-angle-controlled formation technique has been developed to accomplish a self-delimited and uniform catalyst distribution on the ultrafine sidewall grooves (as will be explained in more detail later), even for the use of stable and thick oxide/nitride layer thicknesses of $t_{dep_O} \approx 25$ nm/$t_{dep_N} \approx 15$ nm, respectively, as shown in the cross-section SEM image in **Figure 2**a. Then, after evaporating nominal 5 nm In catalyst layer at a tilted angle of $\theta_{in} \approx 70°$, parallel lines of dense In droplets were formed on the SiN_x walls, with typical diameters of 13 nm, as seen in Figure 2b and the statistics in the inset. It is important to have these catalyst droplets separated in lines, which is a key to suppressing the cross-groove-merging and random droplet size fluctuations.

A typical SEM image of the SiNWs, grown under such tight sidewall groove confinement, is presented in Figure 2c, revealing a uniform growth of five ultrathin SiNWs with typical diameter or $H_{nw} \approx 16$ nm. The cross-section profiles of a 10-layer stacked SiNW structure are exposed by focused ion beam (FIB) milling, examined by using transmission electron microscope (TEM) and shown in Figure 2d–f. Remarkably, all the sidewall grooves were grown/filled with a single SiNW, pseudo-colored into light-green, bounded by the protrusive SiN_x walls. An enlarged view of the 10th SiNW in Figure 2e reveals that there is still remnant a-Si layer (light-yellow) around the SiNW, implicating that the catalyst droplet consumes only a portion of the a-Si supply during the IPSLS growth. This partial a-Si absorption phenomenon has also been observed for the IPSLS growth of SiNWs on planar surface,[31,40] usually for the oversupply of a-Si for the relatively smaller catalyst droplets. Figure 2f presents the high resolution (HR)-TEM characterization of the 3rd layer SiNW channel, revealing a monocrystalline core and elliptic shape, with $H_{nw} = 17$ nm and $W_{nw} = 8$ nm. The calculated electron diffraction pattern in Figure 2g indicates that the growth orientation is along Si<110> direction. Meanwhile, statistics of the height, width and growth orientation of the SiNWs are extracted and shown in Figure 2h,i,j, respectively, indicating that these SiNW channels, with an aspect ratio of $H_{nw}/W_{nw} \approx 2$, can be tightly-confined by the sidewall grooves to achieve a mean width of $W_{nw} = 9.9 \pm 1.2$ nm, approaching to the CD width in the 10 nm technology Node.[21]

2.3. Critical Catalyst Formation Control

The uniform size control of the as-grown ultrathin SiNWs has been accomplished via a tilted-angle-controlled catalyst formation strategy, representing an unexplored dimension of control upon the vertical sidewall grooves. First of all, as depicted schematically in **Figure 3**a, when the In evaporation flux is directed to the vertical sidewall grooves at a small tilted angle of $\theta_{in} < 50°$, with respect to the stacking up direction, most of the incoming In atoms are landed on the top of the SiN_x walls, as seen in the SEM image shown in Figure 3d. In the subsequent H_2 plasma treatment step conducted above the melting point of In, this wall-riding In droplets have 50%–50% chance to fall/move into the upper or the lower grooves, thus causing a random distribution of larger droplets in the grooves and empty ones in their neighborhoods. When the incident angle is set to $\theta_{in} \approx 90°$, the In layer will cover both the SiN_x wall-top and the SiO_2 trench-bottom surfaces, as observed indeed in Figure 3f, leaving a similar chance for the droplets to move and merge in the upper or the lower sidewall grooves (Figure 3c), and thus causing large diameter fluctuations among the closely packed grooves, as witnessed in Figure 3i.

Fortunately, there exists still an optimum parametric window for the incident angle in between $60° < \theta_{in} < 80°$ (Figure 3b), where the In droplets are deposited onto the wall-top (with the false color of green) and the lower-edge (pink) surfaces. This special droplet landing configuration is also observed in the SEM imaging, as shown in Figure 3e. During the IPSLS growth, the wall-top-riding droplets are most likely to touch and merge with the nearest lower-edge droplets, and thus get

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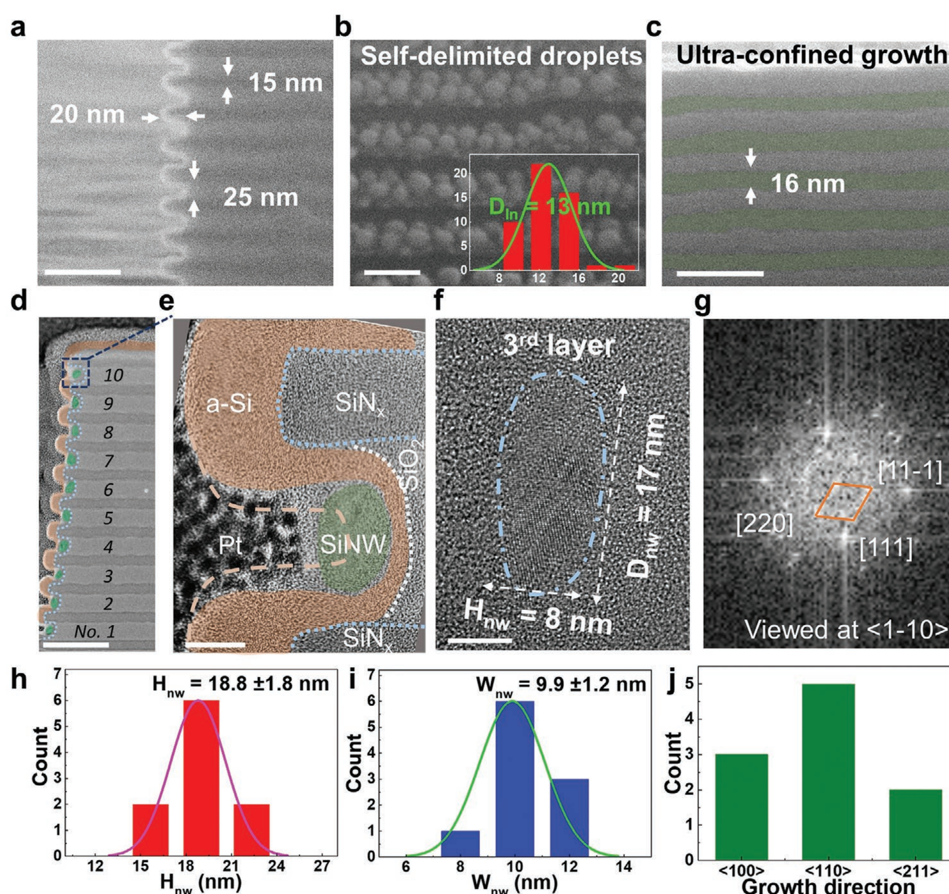

Figure 2. Morphology and statistics of 3D stacked SiNWs. a–c) The typical SEM images of the etched sidewall grooves, self-delimited In droplets on the sidewall, and the as-grown SiNWs with proper parameter controls, respectively. d) The cross-sectional TEM image of the SiNW array. e,f) Enlarged TEM view of NW on 10th and 3rd layer, where the residual a-Si and NW are tinted to light-yellow and green. The dashed line in (e) delineates roughly the original surface profile of the a-Si coating layer in the groove before the growth of SiNW. g) The corresponding electron diffraction pattern. h–j) Statistics on height, width, and growth direction of SiNWs. Scale bars in (a,c,d) are for 100 nm, while (b) for 50 nm, (e) for 10 nm, and (f) for 5 nm.

directed to move into the upper guiding grooves. This directed-merging dynamic helps to ensure simultaneously the size uniformity of the catalyst droplets and a close-to-unity guided growth of a single SiNW within each groove, as seen for example in Figure 3h showing 10 layers of SiNWs grown within all the sidewall grooves, obtained under the proper tilted-angle control.

2.4. Cross-section Geometry Control

Another outstanding capability of this groove-confined growth is to confine or tailor the cross-section shape of the as-grown SiNW channels, as illustrated schematically in **Figure** 4a, which has been testified upon a purposely designed sidewall grooves with a varied SiO_2 trench width in each layer, increasing from 10 nm at the top to 30 nm at the bottom level, as seen in the sideview SEM image in Figure 4b. With the same the a-Si:H coating layer thickness and In layer evaporation condition, SiNWs of different diameters were grown within the different sidewall grooves. However, it is also noteworthy that, with the same a-Si:H coating condition, an optimal *matched* growth condition cannot be met simultaneously for all these guiding grooves with different widths, which will cause unstable or discontinued growth of SiNWs in some of the grooves, leaving unoccupied/empty grooves (without SiNWs) in the 3rd and 5th layers. Cross-sectional TEM analysis in Figure 4c further reveals that the aspect ratio of the SiNWs can be effectively adjusted by varying the trench oxide layer thickness. For example, a high aspect-ratio SiNW was grown within the 1st layer with the widest trench layer of 30 nm (Figure 4d), while a flat channel was obtained within the 4th layer with much thinner trench width of 15 nm (see Figure 4e). It is worthy to note that, though these SiNWs were not grown with optimal parameter conditions (due to the varied groove width), they represent the first experimental proof of the possibility to tailor the c-Si channels continuously from fin-like to sheet-like geometries, via a rather simple and convenient layer-deposition or groove-etching control.

2.5. Prototype Field Effect Transistor

To testify the electronic transport property of the ultrathin sidewall SiNW channels, a simple FET device was fabricated.

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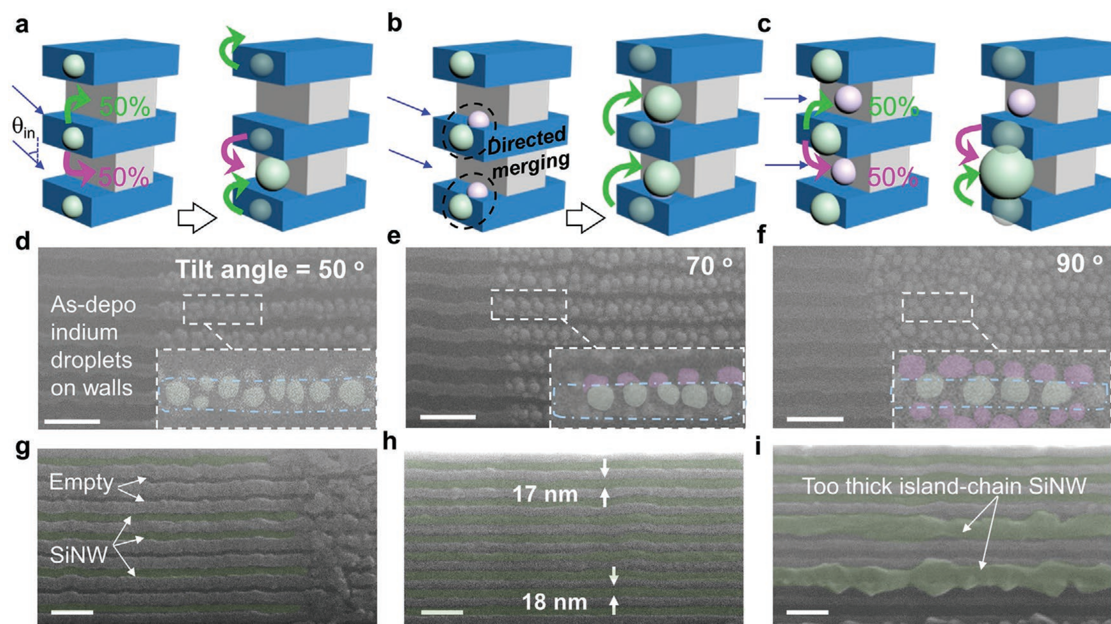

Figure 3. Tilted-angle-controlled catalyst formation. a-c) schematic illustrations of the evolution and merging of the In catalyst droplets, formed on the corrugated SiN_x (wall)/SiO_2 (trench) sidewall grooves, under an increased incident angle of 50°, 70°, and 90°, respectively, with the corresponding the SEM images of the as-formed catalyst droplets provided in d–f) and the as-grown SiNWs on the sidewall grooves in g–i). Scale bars in d-i are all for 100 nm.

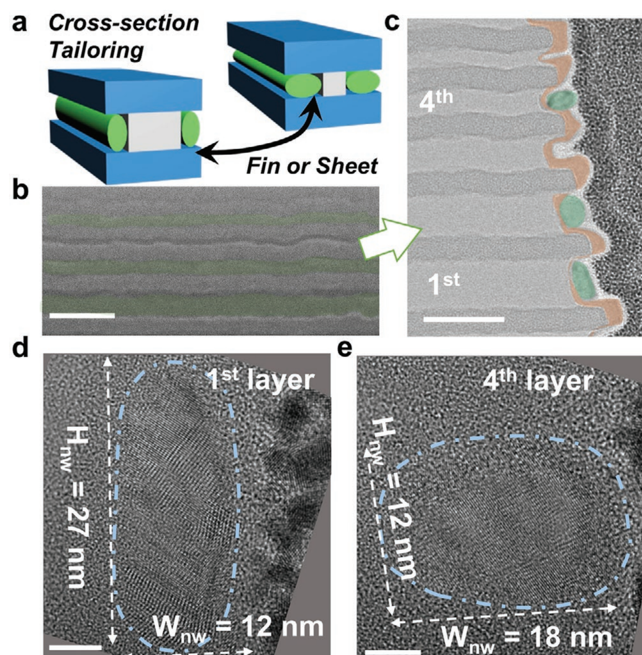

Figure 4. Tailored cross-sectional geometry controlled by groove profile. a) Schematic for the channel geometry control via different profile designs, while (b,c) show the SEM and TEM images of the SiNWs grown upon a specially designed sidewall grooves with continuously varied trench widths. d,e) TEM characterizations of the fin-shaped and sheet-shaped SiNW channels grown at different levels tailored by the grooves with different aspect-ratio profiles. Scale bar in (b) is 100 nm, in (c) is 50 nm, in (d,e) are 5 nm.

A column of 5-layer-stacked SiNWs, with an average height of 18.8 nm, was chosen and connected by a pair of composite Pt (5 nm)/Al (55 nm) Source/Drain (S/D)electrodes, defined by conventional lithography as diagrammed in **Figure 5**a, with a channel length of 2 µm. Note that prior to the S/D electrode fabrication, the remnant a-Si layers were first etched off by using reactive ion etching (RIE) etching, which can easily remove most of the a-Si left on the protrusive SiN_x walls, except the small amount of hidden a-Si rest in between the SiNW channels and the groove bottom surfaces (as seen in Figure 2e), which is intrinsic and high-resistive as no dopant gas was used. After that, a thin Al_2O_3 dielectric layer of 30 nm thick was deposited by using atomic layer deposition (ALD), followed by the preparation of a 60 nm Al side-gate electrode. This thus formed a single-side-gated configuration as depicted in the right inset of Figure 5a, with a photograph of the final device layout presented in Figure 5b. It has been known that the dissolution of In atoms into the SiNWs gives rise to a p-type doping with an equivalent B-doping of ≈ 10^{18} cm^{-3}.[32] The I_{ds}-V_{ds} characterization shown in Figure S2, Supporting Information indicates that the Pt/Al electrode contacts to the as-grown p-type SiNWs formed typical Schottky barrier (SB) junctions, with a band gap alignment profile as depicted schematically in Figure 5c (under V_{gs} = 0 V). Therefore, a pair of such SB junctions connected back-to-back in serial blocked the transport of hole carriers under positive $V_{gs} \geq 0$ V gating biases. In contrast, when a negative gating voltage is applied, a significant amount of holes are accumulated in the p-type SiNW channels, causing a thinning of the SB that will allow the holes to easily tunnel through the triangle barriers, to turn ON the channel current. The initial transfer and output characteristics of the as-fabricated FET are provided in Figure S3, Supporting Information, showing

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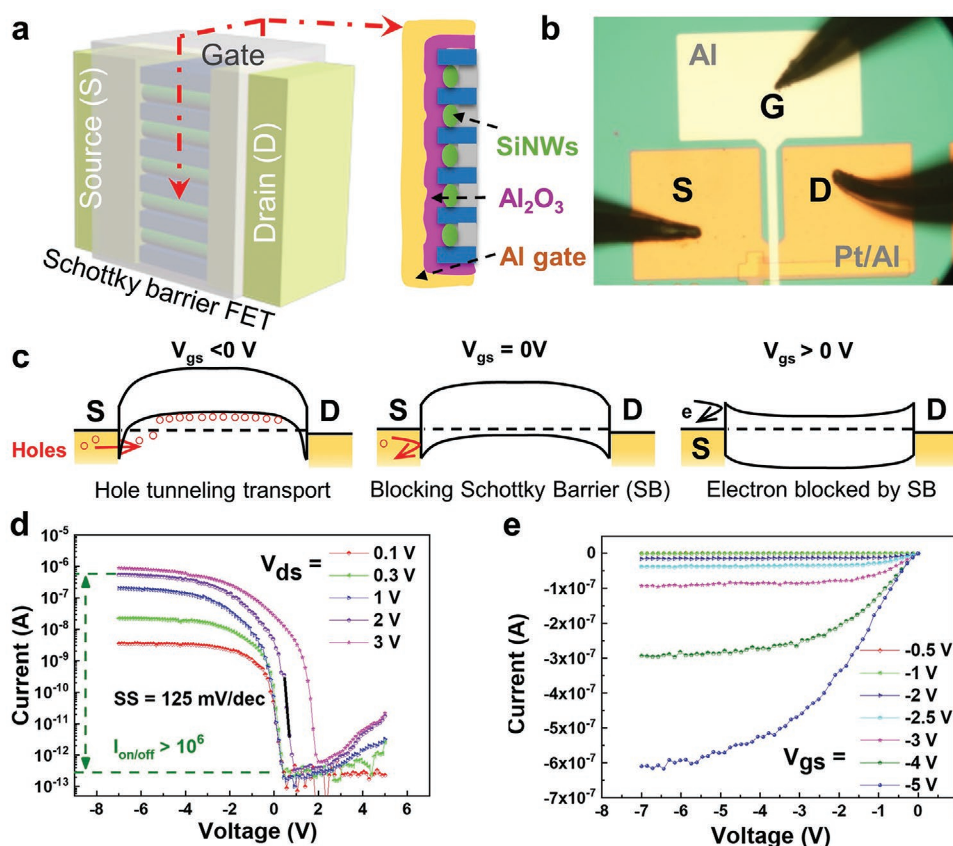

Figure 5. Electrical transport properties of the FET. a) Schematic diagram of the device with cross-section view of the channel region depicted right. b) The photography of a device testing layout. c) Band gap alignment profiles under different gating bias conditions. d) The typical transfer curves under different V_{ds}. e) The output curves of the device.

a high $I_{on/off}$ ratio $>10^6$ and SS of 242 mV dec^{-1}. The device performance can be further improved to $I_{on/off} > 2 \times 10^6$ and SS = 125 mV dec^{-1} as seen in Figure 5d,e, by forming a roughly 2 nm thick SiO_2 layer on the SiNW channels via an 850 °C oxidation for 1 min.

3. Discussion

Compared to the existing technologies that have been used to fabricate ultrathin c-Si nanowire, narrow fin or nanosheet channels,[1,12,21] with CD control down to tens of nanometers, as summarized in **Table 1**, the ultra-confined sidewall growth represents indeed a new strategy to batch-manufacture ultrathin, orderly and vertically stacked SiNW channels with CD that can really approach to that in 10 nm node, but without the need of using sophisticated SAQP, electron beam lithography (EBL) or EUV lithography technologies. Also, a low temperature (350 °C) bottom-up growth of the uniform ultrathin SiNW channels has a unique potential to enable a monolithic 3D integration of various back-end-of-line logics or memory functionalities, considered as the most promising strategy to push the evolution of Moore's law further,[25,41,42] directly upon the front-end electronic circuit layer, and does not require the preexistence of high-quality c-Si wafer substrate, as necessary for all the top-down lithography and etching technologies.

4. Conclusion

In summary, a catalytic low-temperature growth integration of ultrathin 3D stacked SiNW channels has been demonstrated, with rather uniform width and height of $W_{nw} = 9.9 \pm 1.2$ nm and $H_{nw} = 18.8 \pm 1.8$ nm, approaching to the CD in 10 nm node. This has been enabled via a new self-delimited catalyst formation and growth control strategy, with yet a unique capability to engineer the SiNW cross-section from fin-like to sheet-like geometries. Prototype FET devices are also successfully fabricated based on the ultrathin channels, demonstrating a high $I_{on/off}$ ratio and a small sub-threshold swing of $>10^6$ and 125 mV dec^{-1}, respectively. These results indicate that a well-controlled *bottom-up* growth can also reliably fabricate ultrathin and high-density c-Si channels with CD control down to <10 nm, comparable to the cutting-edge top-down technology, while there are still plenty of room for further device performance improvement, given better parameter controls, such as, but not limited to, the use of thinner high-k dielectric layer and optimized S/D electrodes, more importantly in a truly GAA-gating configuration. In short, the successful demonstration of such an ultraconfined catalytic growth integration of ultrathin and uniform SiNWs opens up a promising new route to establish more advanced 3D monolithic integration architecture, as well as the novel logic-in-memory and neuromorphic functionalities.

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Table 1. Comparison to the fabrication strategies for ultrathin SiNW or channels in literature.

Channel fabrication	CD [nm]	Spacing [nm]	Size/Uniformity controlled by	Growth/forming temperature [°C]	Challenges for monolithic 3D integration	Ref.
VLS growth	6.4 ± 1.2	Random array	Catalyst droplets	440	Difficult to align and stack as orderly 3D array	[12]
Solid-Phase Crystallization	9 ± 1.1	16	Corner spacer	1050	High temperature & poly-Si quality	[19]
5 nm GAA-Node by SAQP patterning	8 ± 0.7	12	193 nm Lithography + spacer layer width	750	Rely on preexisting C-Si wafer	[1]
10 nm Fin-Node by SAQP patterning	7~14	30	193 nm Lithography + spacer layer width	< 400	Rely on preexisting C-Si wafer	[21]
SiNW channels by EBL lithography	22 ± 3.8	70	Electron Beam Lithography	625	Rely on preexisting C-Si wafer	[7]
SiNW channels by EUV lithography	14 ± 0.6	14	Electron Ultraviolet Lithography	250	Rely on preexisting C-Si wafer	[8]
IPSLS gowth	28 ± 2.4	40	Droplet formation in wider channels	350	Large SiNW diameter low integration density	[28]
Ultra-confined IPSLS growth	9.9 ± 1.2	20	Ultrathin channels + self-delimited droplet	350	Suitable for 3D monolithic integration	This work

5. Experimental Section

Sidewall Grooves Formation: First, multiple layers of SiO_2 and SiN_x film were deposited alternatively upon 400 nm oxide-coated Si wafer substrate, within a PECVD system, where the thicknesses of each sublayer can be precisely controlled by tuning the deposition durations. Typically, the deposition of the SiO_2 layer was accomplished by using a gas mixture of 80 sccm SiH_4, 120 sccm N_2O, and 40 sccm N_2 at 300 °C, with a chamber pressure of 100 Pa, radio frequency (RF) power of 10 W, while for the SiNx layer a gas mixture of 100 sccm SiH_4, 6 sccm NH_3, and 100 sccm N_2 was used with a chamber pressure of 80 Pa and RF power of 40 W. After that, the positions of the guiding sidewalls were defined by using standard lithography or electron beam lithography, followed by a vertical inductive coupled plasma etching of the SiN_x/SO_2 superlattice to expose the vertical sidewalls, by using C_4F_8 plasma etchant gas and patterned photoresist (P.R.) or aluminum (Al) films as masks. Finally, a selective erosion of the oxide layers was carried out by using BOE solution, with precisely controlled dipping times, ranging from 5s to 20s, prior to rinse off the masks in acetone (for P.R.) or dilute HCl (for Al) solutions.

Self-Delimited Catalyst Deposition: The position of the In catalyst stripes was first defined by conventional lithography, lying crossing the end of the guiding sidewalls. Then, the samples were fixed onto an adjustable holder that can keep the sample at different tilted angles, varying from 50°, 70° to 90° (normal incident to the vertical sidewalls), when being placed on the platform of an electron beam evaporation (EBE) system. Note that the tilted angle was defined as the intersect angle between the incident In evaporation flux and the vertical SiN_x/SiO_2 stacking direction. Finally, a nominally 5–10 nm thick In catalyst layer was evaporated onto the sample surface, followed by a standard lift-off procedure of the remnant In.

Guided Growth of SiNWs on the Sidewall Grooves: The samples were first loaded into a PECVD system for H_2 plasma treatment at 250 °C (higher than the melting point of In, T_{in} = 157 °C) to reduce the surface oxide layer of the In droplets, allowing for the diffusion of In atoms and merging of the neighbored In droplets. The typical values for H_2 flow rate, chamber pressure, and RF power were 10 sccm, 140 Pa, and 10 W, respectively. Then, the samples were cooled to 100 °C, to frozen In droplets back into solid, before depositing a thin film of a-Si:H precursor layer by using silane plasma, with flow rate, chamber pressure, and RF power of 5 sccm, 20 Pa and 2 W, respectively. Upon annealing at 350 °C in vacuum, the solid In particles became molten again and started to absorb the nearby a-Si:H to move along the grooves, while producing c-SiNWs lying within the sidewall grooves. At the end of the SiNW growth, the remnant a-Si:H layer was removed by using CF_4 plasma etching in RIE system, followed by an O_2 plasma to remove the produced carbon-compound resultant.

FETs Fabrication and Characterizations: In the next step, the SiNWs channels were either directly contacted by S/D electrodes, or first treated in dry O_2 ambient at 850 °C for 1 min to form a roughly 2 nm thin SiO_2 layer prior to the S/D electrode preparation. After the S/D lithography and 4% HF dipping to remove the oxide layer on the exposed SiNWs, the sample was loaded into an EBE system and received the deposition of a composite Pt/Al (5 nm/55 nm) layer at a tilted angle of 60° for a better sidewall coverage by the deposited electrodes. Then, a 30 nm Al_2O_3 dielectric layer was coated at 300 °C by using ALD system, followed by the preparation of 60 nm Al gate electrodes. The electrical transport properties were measured by using a double-channeled Keithley 2636B unit at room temperature.

Statistical Analysis: The SEM and TEM images were presented with pseudo colors for the ease of observation, where SiNWs were tinted to green, a-Si layer tinted to light-yellow, and In droplets tinted to light-green and pink. The statistics on the height and width of SiNWs were extracted from TEM images with Gaussian distribution fitting lines and the corresponding standard deviation generated in Origin software. The transfer curves and output curves were plotted in Origin using raw data without further processing.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest

The authors declare no conflict of interest.

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

Keywords

3D integration, catalytic growth, in-plane solid-liquid-solid, ultrathin Si nanowires

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