Applied Surface Science 635 (2023) 157635

Contents lists available at ScienceDirect

Applied Surface Science

journal homepage: www.elsevier.com/locate/apsusc

Full Length Article

High-fidelity moulding growth and cross-section shaping of ultrathin monocrystalline silicon nanowires

Yifei Liang [a], Wentao Qian [a], Ruijin Hu [b], Xin Gan [a], Shuqi Shi [a], Yating Li [a], Junzhuan Wang [a,*], Zongguang Liu [a], Daowei He [a], Yi Shi [a], Jun Xu [a], Kunji Chen [a], Linwei Yu [a,*]

[a] School of Electronic Science and Engineering/National Laboratory of Solid-State Microstructures, Nanjing University, 210093 Nanjing, China
[b] School of Physical Science and Technology/Microelectronics Industry Research Institute, Yangzhou University, 225002 Yangzhou, China

ARTICLE INFO

Keywords:
Silicon nanowire
Uniform growth
Shape transition
Monocrystal

ABSTRACT

Catalytic growth of ultrathin silicon nanowires (SiNWs) provides ideal 1D channel materials for the construction of high-performance field effect transistors, where the diameter, uniformity and crystalline qualities are of utmost importance. In this work, a high-fidelity moulding growth of orderly ultrathin monocrystalline SiNWs, with diameter of 17 ± 2 nm, has been accomplished within tightly confined nanogrooves. A continuous and deterministic groove-width-transition or squeezing strategy has also been developed to accomplish an effective cross-section tailoring of the as-grown SiNW channels, while enabling a close-to-unity growth filling rate within the guiding grooves. Finally, a size-dependent adatom-searching model is proposed to explain how a monocrystalline SiNWs can be obtained even at such a low growth temperature of < 350 ℃. These results indicate a feasible catalytic growth fabrication route to implement monolithic 3D integration of advanced in-memory-computing and neuromorphic electronics.

1. Introduction

In pursuit of stronger electrostatic control, faster operation speed and less power consumption, the mainstream crystalline silicon (c-Si) field effect transistors (FETs) have evolved, over the last decades, from planar to fin-gate [1,2], and to the latest gate-all-around (GAA) channel configurations. The last one features horizontally stacked quasi-1D channels of ultrathin Si nanowires (NWs) or nanosheets [3–7]. In parallel, monolithic 3D (M3D) integration has been widely explored as the most promising paradigm to boost the integration density, or push forward the Moore's law further [8–11]. As illustrated schematically in Fig. 1a, multilayers of logics/memory units can be vertically stacked, and interconnected with direct unit-to-unit via, which is crucial to minimize the interlayer resistance and RC delay [12,13]. However, the conventional top-down etching fabrication of orderly array of ultrathin NW channels is difficult to implement in the stacked logic layers due to the lack of c-Si wafer. Also, the highest processing temperature allowed for the top, or the so-called back-end-of-line (BEOL), Si logic layer is ~ 450 ℃ [14,15], to avoid thermal damage of the bottom front-end-of-line (FEOL) logics. So, it is highly desirable to seek a reliable low-temperature fabrication strategy of ultrathin and monocrystalline c-SiNW channels, as a key basis to extend the mature c-Si technology in the M3D integration architecture.

Instead of subtractive etching patterning into c-Si wafer for NW channel formation, high-quality c-Si NWs can also be obtained via additive catalytic growth approaches, mediated by nanoscale metal droplets [16–19]. Though many high-performance prototype logics [20–22], sensors [23,24] and memory devices [25,26] have been demonstrated based on the catalytic SiNW channels, via the famous vapor–liquid-solid (VLS) mechanism [26–29], a bottleneck challenge remains as to how to position and integrate them precisely on planar substrate, ready for reliable electronic device integration. A feasible approach is to marry the surface-pattern formed by top-down lithography to the low-temperature catalytic growth, where the former provides a deterministic mould as growth guidance, while the latter can produce ultrathin monocrystalline c-Si channels at prescribed locations.

In our previous works, an in-plane solid–liquid-solid (IPSLS) mechanism has been established to grow planar SiNWs at a rather low temperature of ~ 350 ℃, where low-melting-point metal of indium (In) droplet was employed to absorb surface-coating amorphous Si (a-Si) thin film as precursor [30,31]. Compared to the VLS growth, the IPSLS SiNWs are particularly suitable to serve as 1D channels, as the SiNW

* Corresponding authors.
E-mail addresses: wangjz@nju.edu.cn (J. Wang), yulinwei@nju.edu.cn (L. Yu).

https://doi.org/10.1016/j.apsusc.2023.157635
Received 29 March 2023; Received in revised form 16 May 2023; Accepted 27 May 2023
Available online 29 May 2023
0169-4332/© 2023 Elsevier B.V. All rights reserved.

growth can be well guided by single-sided step edges to grow into desired locations [32–34]. However, the single-sided guided growth has a relatively weak control over the diameter or profile of the as-grown SiNWs, and a high-density integration (pitch $\leq$ 50 nm) of orderly SiNW array on planar surface has not been possible so far. It is also desirable that the SiNW can be grown into a rather dense array with readily tunable channel cross-section geometry, which is a critical dimension for the fin or GAA-gated FETs, as indicated in Fig. 1b.

So, the goal of this work is to explore a high-fidelity catalytic moulding growth of ultrathin monocrystalline SiNWs, within tightly confined high-density grooves with aggressively reduced width $<$ 25 nm. A parametric investigation has been carried out to understand the influences of guiding groove profiles on the growth filling rate, uniformity and channel geometry profile of the as-grown SiNWs. In addition, the width of groove will be adopted as a new dimension to tailor the aspect ratio of the SiNW channels. And a size-dependent adatom-researching model will be proposed to explain the growth formation of monocrystalline SiNWs at such a low growth temperature.

2. Experimental methods

The major fabrication steps for the double-confined growth of IPSLS SiNWs are schematically diagrammed in Fig. 1c-f, which involve, first, the formation of SiO_2 guiding grooves of 27 nm wide and 23 nm high, with a spacing of 23 nm on top of a Si substrate coated with a 90 nm SiO2 layer, by using electron beam lithography (EBL), where the SiO_2 sidewalls were produced by using negative resist of hydrogen silsesquioxane (HSQ) under electron beam exposure. Second, indium (In) catalyst stripes of 6 nm thick were deposited crossing the ends of the nanogrooves, via EBL patterning and subsequent thermal evaporation. The sample was then loaded into a plasma-enhanced chemical vapor deposition (PECVD) system and treated by H_2 plasma at 350 ℃ for 3 min, during which the surface oxide layer of In stripes were reduced, allowing them to diffuse and merge into separated droplets. The flow rate of H_2, chamber pressure and RF power were 15 sccm, 140 Pa and 10 W. After that, the substrate was coated with an a-Si layer as precursor at 150 ℃, for 2 min30 s by introducing silane into the chamber with flow rate, chamber pressure and RF power of 5 sccm, 20 Pa and 2 W, which was followed by an *in-situ* annealing in a high vacuum (10^{-4} Pa) at 290 ℃ to activate the In droplets to absorb a-Si and produce c-Si NWs when moving along the grooves. Similar to our previous works [16,30–32,35], the a-Si precursor layer thickness has to be matched with the size of In catalyst droplets, which can be controlled by tuning the initial In layer thickness and the H_2 plasma treatment conditions, to ensure a stable growth of relatively straight SiNWs. In this work, a suitable balance growth condition, with 10 nm thick a-Si layer and 6 nm thick initial In layer, has been adopted and fixed for all the following experiments. Finally, the remnant a-Si layer after the IPSLS growth can be removed by an in-situ H plasma etching at 180 ℃ or via a CF_4 reactive ion etching (RIE) at room temperature [36,37], while the exposed nanogrooves can be etched off later by dipping into a diluted Hydrofluoric acid (dHF) solution for further device fabrication. However, in this work, the remnant a-Si layer and the nanogrooves were preserved to facilitate analysis of the growth dynamics of the IPSLS SiNWs within the tightly confined guiding grooves.

3. Results and discussion

The double-confined (DC) guiding nanogrooves were designed to impose a stronger size confinement of the IPSLS SiNWs, compared to the single-step-guided (SG) growth of SiNWs, as in the latter case the In droplet is attracted by the guiding edge, but still free to move or vibrate in the lateral direction, as depicted in Fig. 1g, which will lead to random diameter variation. This is indeed that case, as witnessed in the Scanning Electron Microscopy (SEM) image of the typical SiNWs in Fig. 1i and schematized diagrammed in Fig. 1h, where the DC and SG SiNWs are pseudo-colored into green and purple, respectively. According to the extracted diameter/width variations of the DC and SG SiNWs plotted in Fig. 1j, the uniformity of the SiNWs can be substantially improved within the double-confined grooves, to achieve a diameter of $D_{nw}^{DC} = 23 \pm 1.8$ nm, slightly narrower than the patterned groove width of 27 nm.

Interestingly, the groove width of W_g has a significant impact on the growth behaviors and uniformity of the SiNWs within the grooves. For a constant In stripe thickness of 6 nm, as seen for example in Fig. 2a, three groove widths of 50 nm, 30 nm and 20 nm, were fabricated with a constant wall width of 30 nm, as seen in Fig. 2b-2d. It was found that if the grooves are too wide, as in the case of Fig. 2b with W_g = 50 nm, though all the grooves are filled with at least one SiNW, the In droplet seems to be too small to fulfil the groove, resulting in SiNWs highlighted

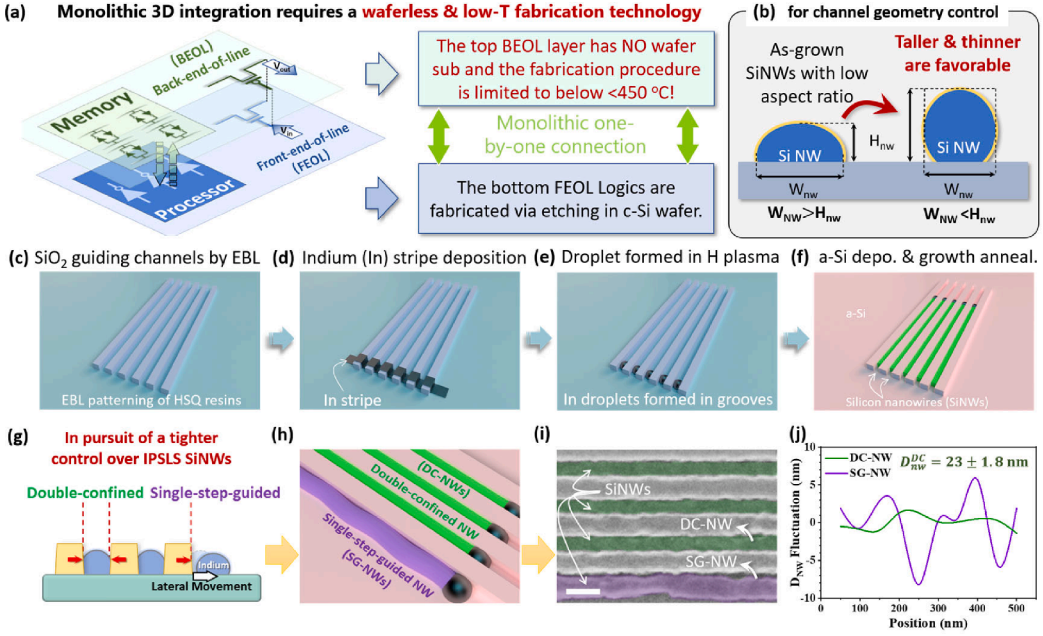


Fig. 1. (a), schematic illustration of the M3D integration of logic and memory units where the BEOL layer needs to be fabricated via a low temperature processing and without c-Si wafer. (b), depicts the desired cross-section tailoring of SiNWs into taller and thinner channels. (c)-(f), diagrams the major fabrication steps for the double-confined IPSLS growth of planar SiNWs within nanogrooves. (g), illustrates that double-confined SiNW growth imposes a stronger size control than that of single-step-guided droplet. (h)-(i), illustration and SEM images of the double-confined NWs (green) compared to the single-step-guided NWs (purple). Scale bar in (i) stands for 50 nm. (j), plots the extracted diameter/width variations of the double-confined and single-step-guided NWs for the bottom two SiNWs found in (i).

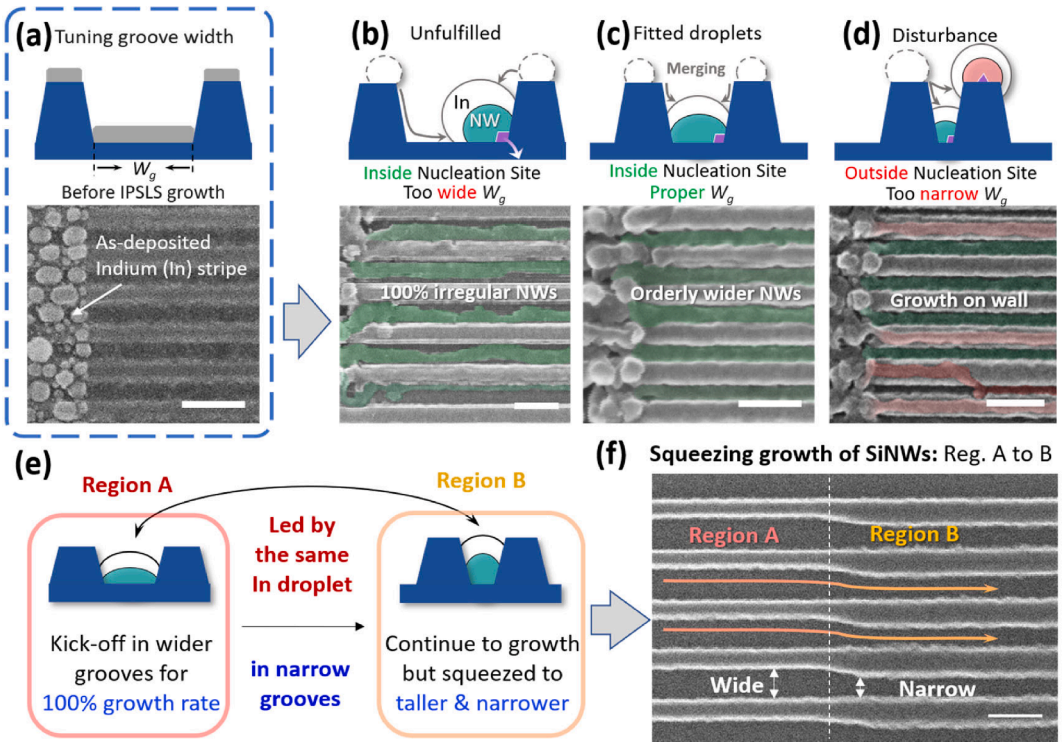


Fig. 2. (a), the schematic illustration and SEM image of the double-confined (DC) grooves with evaporated In stripe at one end, before the IPSLS growth. Scale bar stands for 100 nm. (b)-(d), depict the 3 typical situations for the DC growth of SiNWs, with too wide, proper and too narrow groove widths W_g, respectively, with corresponding SEM images shown in the lower panels. (e), illustrates a special groove width transition or squeezing design, to achieve first a high growth filling rate in wider grooves prior to being squeezed to become thinner in narrower grooves, with a typical SEM image of the groove width transition region shown in (f), where the W_g = 30 nm in Region A is reduced to to 20 nm in Region B. Scale bars in (b)-(d) and (f) stand for 100 nm and 30 nm, respectively.

by pseudo-green loosely grown within the grooves, with random and huge diameter fluctuations. To the opposite extreme, the In droplets were too large to be fully confined within the narrow grooves with W_g = 20 nm, and thus there was a chance for the initial nucleation of c-Si seed to take place directly upon the top of the walls, in strong contrast to the desired nucleation site within the grooves, as depicted schematically in Fig. 2d. When this happened, surplus growth of continuous SiNWs can be found along the wall lines, or crossing from walls to grooves, undermining the basis for achieving a stable groove-confined guided growth. Only for the proper choice of groove width set to 30 nm, as showcased in Fig. 2c, a rather stable and uniform growth of SiNW have been obtained, fulfilling the width of all the grooves, with a rather uniform diameter of the SiNWs.

However, a taller and narrower c-Si channel is always preferred for the construction of fin or GAA-gated FETs [38]. Unfortunately, this can't be accomplished by simply reducing the groove width as seen already in Fig. 2d, due to the formation of surplus nucleation site upon the top of walls. Though reducing In catalyst thickness could help to alleviate this challenge to some extent, it will also reduce the chance for the discrete In droplets (initially sitting on the walls and the grooves) to merge into a bigger ones settled down only at the bottom of grooves. As a consequence, the In droplets left on top of the walls will lead to non-groove or wall-riding guided growth of SiNWs. Also, it is still attractive if one could enforce the growth of SiNW channels with higher aspect-ratio, such as the one diagrammed in the right panel of Fig. 2e. So, a new type of width-transition groove has been conceived and fabricated, where wider grooves in Region A, as labeled in Fig. 2e and 2f, were fabricated and crossed by the In stripe, and then switched into Region B with narrower grooves. In this way, we hope to combine the high growth filling rate (approaching 100%) achieved within the wider grooves, as witnessed in Fig. 2b, with the strong size confinement imposed by the narrower grooves, as in Fig. 2d. It is important to note that, as the SiNW growth through the transit position will be continuous, there is no need of forming extra nucleation centers around, thus completely suppressing the surplus growth of SiNW over the top of the walls.

Impressively, as seen in the SEM image shown in Fig. 3a, the SiNW growth starting from Region A, with a groove width of 30 nm, into narrow grooves of 20 nm wide in Region B, is indeed continuous and rather stable. Atomic force microscopy (AFM) scanning in vertical direction across the segments of #1 SiNW in Region A and B, extracted and shown in Fig. 3b, reveals that the height of the SiNW increases by ΔH = 4.7 nm when grown into the narrower region, despite of the fact that the spatial resolution of could be degraded by the size of the AFM probe, ~25 nm in radius. In order to verify this height increment, AFM scans were also carried out along axial direction for #1 and #6 SiNWs found in the grooves. As shown in Fig. 3c and 3d, the average heights of the SiNW segments before and after groove-squeezing transition all increase by an amount of ΔH = 4.1–4.5 nm, which are consistent with the value determined in cross section scan.

In order to examine the final cross-section profile and crystalline quality, the as-grown SiNWs in the final narrow Region B were characterized by high-resolution transmission electron microscopy (HR-TEM), where a focused ion beam (FIB) milling was first applied to cut a slice of the grooves in Region B roughly at position X_2 as indicated in Fig. 3a. As shown in Fig. 4a, 7 SiNWs can be clearly found in the grooves, corresponding to numbering in the SEM image in Fig. 3a, with diameter of 17 ± 2 nm, as well as heights and aspect-ratio displayed in Fig. 4d. Note that the heights of the SiNWs in Region A were deduced from those found in Region B, with the known height disparity determined via AFM characterization in Fig. 3. Though there is no TEM data for the cross-section profile of SiNWs in Region A for this specific sample, a typical TEM profile examination of a similar sample, with the same groove width of 30 nm, is shown Fig. 4b, where it is found that the NW grown in wider grooves are usually flat and thinner with an aspect ratio

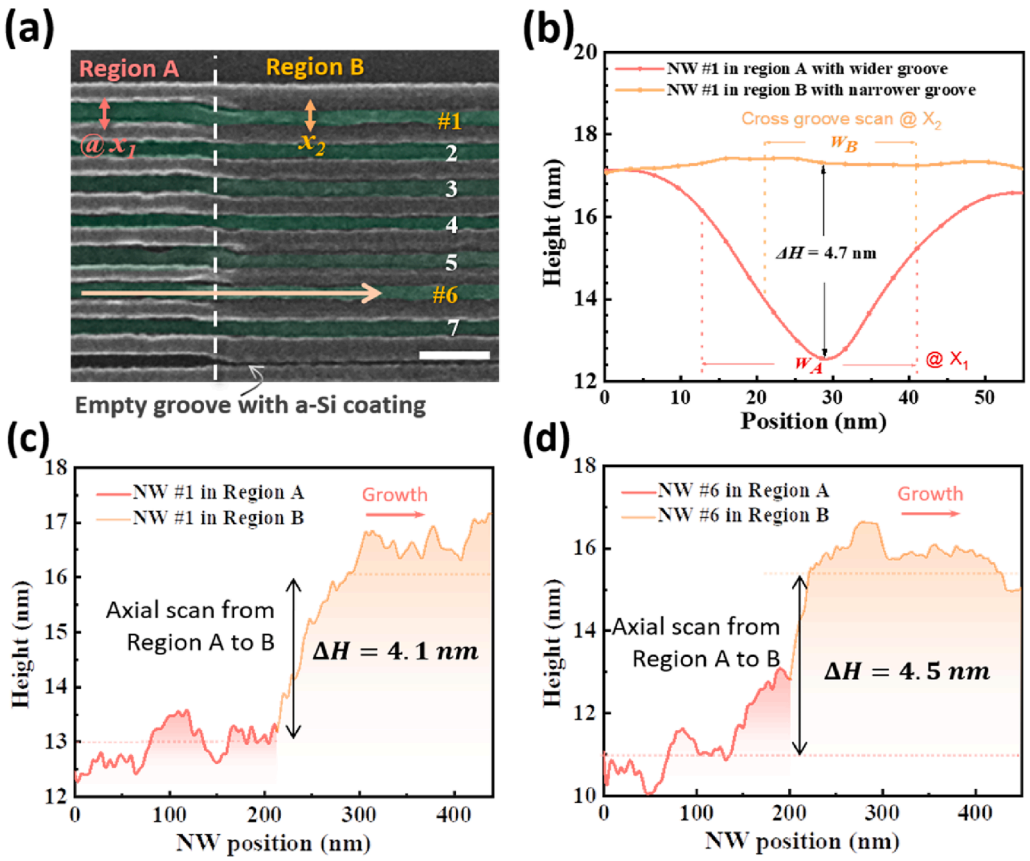


Fig. 3. (a), SEM image of NW grown from region A ($W_g = 30$ nm) into region B ($W_g = 20$ nm). Scale bar stands for 100 nm. (b), plots the extracted height distribution of #1 SiNW at position x_1 and x_2, obtained by AFM scanning in vertical direction across #1 NW. (c)-(d), the extracted height increments of #1 and #6 SiNWs by groove-squeezing transition, obtained by AFM scanning from region A to B along the grooves.

of$H_{nw}/W_{nw} \sim 0.5$. Apparently, the groove squeezing does have significant impact on the profile of SiNWs, increasing their aspect ratio from 0.5 to 1.0, as shown in Fig. 4d, indicating a new and rather effective dimension of control to reshape the channel of geometry of IPSLS SiNWs, without degrading their growth filling rate.

More importantly, after characterizing each cross section of 14 different ultrathin SiNWs with HR-TEM, it is found that all these SiNWs with diameters of ~ 20 nm are monocrystalline, despite of a rather low growth temperature at only 290 ℃, with 78% Si ⟨1 0 0⟩, 7% Si ⟨1 1 0⟩ and 15% Si ⟨1 1 1⟩ as determined by the HR-TEM and electron diffraction patterns, as shown for example in Fig. 4b and 4c. While the underlying mechanism still need to be better understood via more systematical investigation, we propose here a qualitative Si-adatom searching model that could help to explain why a monocrystalline growth can be expected even at such a low temperature.

Considering a typical layer-by-layer growth scenario, which is indeed the case according to the real time TEM observation in VLS growth of SiNWs [39], when a Si adatom is landed on the liquid (In)/solid (SiNW) deposition interface, as sketched in Fig. 4e, it will diffuse around seeking for the most energetically favorable, that's the most stable, site to attach and settle down at the edges of 2D nucleation sites [40,41]. If each Si adatom can be given a long enough time of τ_d, without the interference of other adatoms, to diffuse and search for the full deposition interface for the most energetically stable sites, the growing system can arrive at the lowest energy state, that is forming monocrystalline SiNWs. To guarantee this criterion, for a given diameter of the SiNW D_{nw}, the minimum diffusion time τ_{dm} required to search the full deposition interface can be estimated to be

$$D_{nw} < l_{Si} = \sqrt{D_{Si} \bullet \tau_d} \rightarrow \tau_{dm} > D_{nw}^2/D_{Si} \quad (1)$$

where $D_{Si} \approx 2 \times 10^{-9}$ m^2/s and l_{Si} are the binary diffusion coefficient of Si atoms in liquid indium and the mean diffusion distance of Si adatoms, respectively. Assuming all Si adatoms are added sequentially into the SiNWs, this corresponds to a critical growth rate of

$$v_{nw}^* \sim \frac{a^3}{D_{nw}^2 \tau_{dm}} \quad (2)$$

For the SiNW growth proceeding at a growth rate of $v_{nw} > v_{nw}^*$, the adatoms will be given insufficient time to search the full deposition interface for the most stable attaching site, but instead bonded to other sites with a local lattice configuration inconsistent with the already formed 2D nucleation seeds, that's, the formation of structural defects. So, a monocrystalline growth should be obtained most likely for the relatively slow growth with $v_{nw} < v_{nw}^*$, which is also dependent on the diameter of SiNW.

For the IPSLS growth of SiNWs, the growth rate is typically of $v_{nw} \sim 80\ nm/s$under 290 ℃, for the growth condition adopted in this work, which translates into a critical diameter of

$$D_{nw} < D_{nw}^* = \left(\frac{D_{Si} \bullet a^3}{v_{nw}}\right)^{1/4} \sim 29 \text{ nm} \quad (3)$$

According to this largely simplified but heuristic formulation of Eq. (3), for the ultrathin SiNW with a diameter below 29 nm, the addition of Si adatoms at the growing SiNW ends could still arrive at the most energetically favorable sites, in other word achieving a mono-crystalline growth as indeed observed in this work. Note that, this critical diameter of D_{nw}^* should be considered as an upper bound for the monocrystalline growth, as there could be other kinetic growth factors not considered in this model. Nevertheless, this model helps to emphasize an important

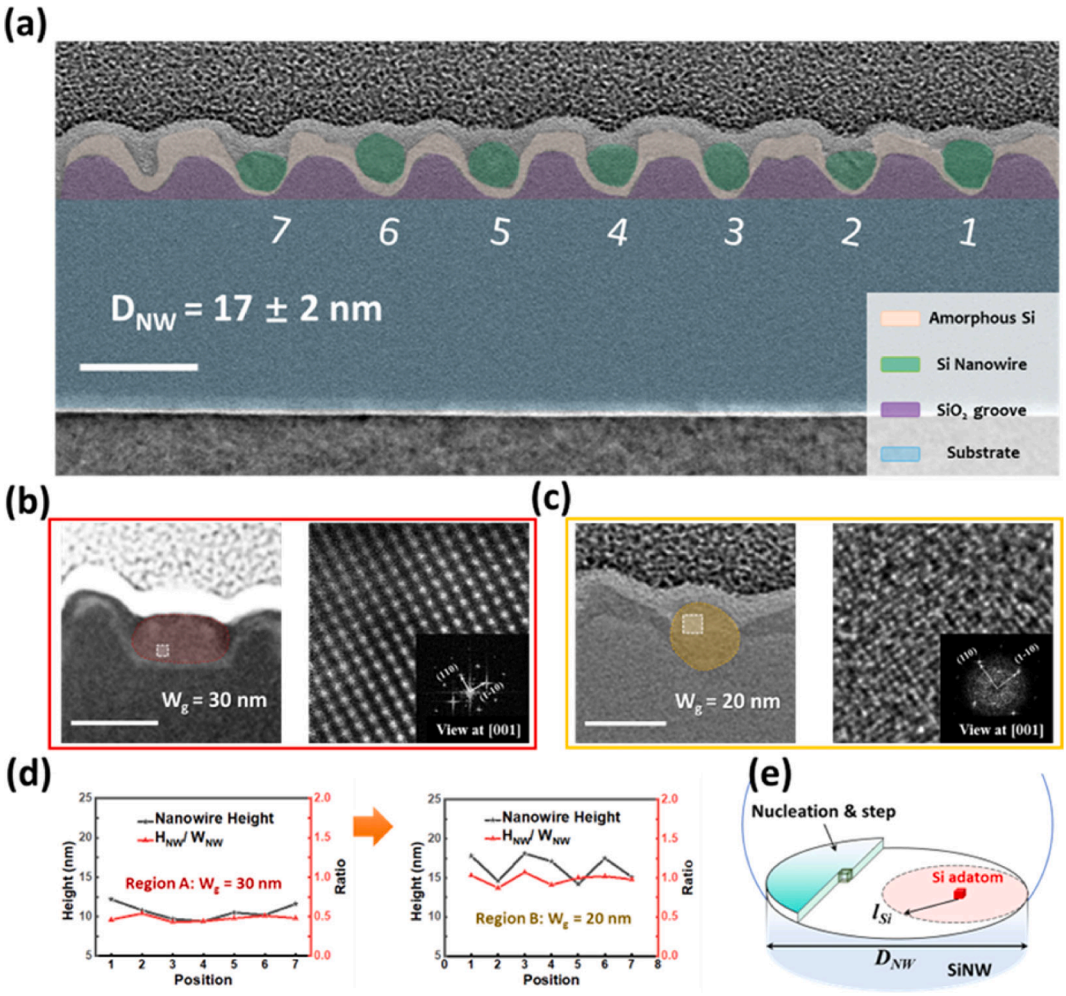


Fig. 4. (a), the cross-section of nanogrooves and SiNWs characterized by HR-TEM, which is obtained roughly from position x_2 in region B in Fig. 3**a**. Scale bar stands for 50 nm. (b)-(c), the TEM images showing the profiles of SiNWs in groove with W_g = 30/20 nm respectively, followed by zoom-in images of the marked areas and corresponding electron diffraction patterns as insets. Scale bars in (b)-(c) stand for 30 nm. (d), the NW heights, and the ratios of height/width distribution in region A (left diagram) and B (right diagram). (e), the Si-adatom searching model in which Si adatom diffuses and seeks for the stable site on In/SiNW interface to form monocrystalline structure.

fact that a low temperature growth of monocrystalline SiNW channels is indeed possible via a catalytic growth at the nanoscale deposition interfaces.

4. Conclusions

In summary, we have successfully demonstrated a high-fidelity moulding growth of orderly array of ultrathin SiNWs at 290 ℃, tightly confined by dense grooves, with a mean diameter of 17 ± 2 nm. A new width-transition groove design has been adopted to enable a close-to-unity growth filling rate of the SiNWs, while providing also a unique cross-section shaping capability to squeeze and reshape the height/width ratio of SiNWs from 0.5 to 1.0, continuously and deterministically, which is favorable for SiNW device applications. Moreover, an adatom-searching model is proposed to explain the formation of monocrystalline SiNWs even at a low temperature catalytic growth at < 350 ℃. These results indicate that a well-controlled catalytic growth has a promising potential to fabricate and integrate high quality 1D channels for the implementation of monolithic 3D integration of more advanced nanoelectronics, without the need of pre-existing c-Si wafer layer as substrate.

CRediT authorship contribution statement

Yifei Liang: Methodology, Validation, Formal analysis, Investigation, Data curation, Writing – original draft, Visualization. **Wentao Qian:** Methodology, Software, Validation, Formal analysis. **Ruijin Hu:** Investigation. **Xin Gan:** Investigation. **Shuqi Shi:** Investigation. **Yating Li:** Investigation, Resources. **Junzhuan Wang:** Methodology, Formal analysis, Investigation, Resources, Data curation, Project administration, Funding acquisition. **Zongguang Liu:** Validation, Resources, Supervision. **Daowei He:** Resources. **Yi Shi:** Supervision, Funding acquisition. **Jun Xu:** Supervision, Funding acquisition. **Kunji Chen:** Supervision, Funding acquisition. **Linwei Yu:** Conceptualization, Methodology, Formal analysis, Investigation, Resources, Data curation, Writing – original draft, Supervision, Project administration, Funding acquisition.

Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Data availability

Data will be made available on request.

Acknowledgements

The authors acknowledged the financial supports from the National Key Research Program of China under granted No. 92164201 and 61921005, National Natural Science Foundation of China under No. 11874198 and 61974064.

References

[1] M. Daga, G.P. Mishra, Subthreshold performance improvement of underlapped FinFET using workfunction modulated dual-metal gate technique, SILICON 13 (2021) 1541–1548.
[2] R.K. Ratnesh, A. Goel, G. Kaushik, H. Garg, M. Chandan, B.P. Singh, Advancement and challenges in MOSFET scaling, Mater. Sci. Semicond. Process. 134 (2021), 106002.
[3] D. Jang, D. Yakimets, G. Eneman, P. Schuddinck, M.G. Bardon, P. Raghavan, A. Spessot, D. Verkest, A. Mocuta, Device exploration of NanoSheet transistors for sub-7-nm technology node, IEEE Trans. Electron Devices 64 (2017) 2707–2713.
[4] G. Bae, D.I. Bae, M. Kang, S.M. Hwang, S.S. Kim, B. Seo, T.Y. Kwon, T.J. Lee, C. Moon, Y.M. Choi, K. Oikawa, S. Masuoka, K.Y. Chun, S.H. Park, H.J. Shin, J.C. Kim, K.K. Bhuwalka, D.H. Kim, W.J. Kim, J. Yoo, H.Y. Jeon, M.S. Yang, S.J. Chung, D. Kim, B.H. Ham, K.J. Park, W.D. Kim, S.H. Park, G. Song, Y.H. Kim, M.S. Kang, K.H. Hwang, C.H. Park, J.H. Lee, D.W. Kim, S.M. Jung, H.K. Kang, 3nm GAA Technology featuring Multi-Bridge-Channel FET for Low Power and High Performance Applications, in: 2018 IEEE International Electron Devices Meeting (IEDM), 2018, pp. 28.27.21-28.27.24.
[5] S. Barraud, B. Previtali, C. Vizioz, J.M. Hartmann, J. Sturm, J. Lassarre, C. Perrot, P. Rodriguez, V. Loup, A. Magalhaes-Lucas, R. Kies, G. Romano, M. Cassé, N. Bernier, A. Jannaud, A. Grenier, F. Andrieu, 7-Levels-Stacked Nanosheet GAA Transistors for High Performance Computing, 2020 IEEE Symposium on VLSI Technology, (2020) pp. 1-2.
[6] H. Mertens, R. Ritzenthaler, A.Y. Hikavyy, M.S. Kim, Z. Tao, K. Wostyn, S.A. Chew, A. De Keersgieter, G. Mannaert, E. Rosseel, T. Schram, K. Devriendt, D. Tsvetanova, H. Dekkers, S. Demuynck, A.V. Chasin, E. Van Besien, A. Dangol, S. Godny, B. Douhard, N. Bosman, O. Richard, J. Geypen, H. Bender, K. Barla, D. Mocuta, N. Horiguchi, A.V.-Y. Thean, Gate-all-around MOSFETs based on vertically stacked horizontal Si nanowires in a replacement metal gate process on bulk Si substrates, 2016 IEEE Symposium on VLSI Technology, (2016) pp. 1-2.
[7] J.P. Colinge, C.W. Lee, A. Afzalian, N.D. Akhavan, R. Yan, I. Ferain, P. Razavi, B. O'Neill, A. Blake, M. White, A.M. Kelleher, B. McCarthy, R. Murphy, Nanowire transistors without junctions, Nat. Nanotechnol. 5 (2010) 225–229.
[8] C.Y. Huang, G.H. Dewey, E.M. Mannebach, A. Phan, P. Morrow, W. Rachmady, I.-C. Tung, N. Thomas, U.S. Alaan, R. Paul, N.A. Kabir, B. Krist, A. Oni, M. Mehta, M. K. Harper, P. Nguyen, R. Keech, S. Vishwanath, K.L. Cheong, J. Kang, A.D. Lilak, M. Metz, S.B. Clendenning, B. Turkot, R. Schenker, H.J. Yoo, M. Radosavljevic, J.T. Kavalieros, 3-D Self-aligned Stacked NMOS-on-PMOS Nanoribbon Transistors for Continued Moore's Law Scaling, 2020 IEEE International Electron Devices Meeting (IEDM), (2020) pp. 20.26.21-20.26.24.
[9] V. Deshpande, V. Djara, E. O'Connor, P. Hashemi, T. Morf, K. Balakrishnan, D. Caimi, M. Sousa, J. Fompeyrine, L. Czornomaz, Three-dimensional monolithic integration of III–V and Si(Ge) FETs for hybrid CMOS and beyond, Jpn. J. Appl. Phys. 56 (2017) 04CA05.
[10] M.M. Shulaker, G. Hills, R.S. Park, R.T. Howe, K. Saraswat, H.P. Wong, S. Mitra, Three-dimensional integration of nanotechnologies for computing and data storage on a single chip, Nature 547 (2017) 74–78.
[11] J. Jeong, S.K. Kim, J. Kim, D.M. Geum, D. Kim, E. Jo, H. Jeong, J. Park, J.H. Jang, S. Choi, I. Kwon, S. Kim, Heterogeneous and monolithic 3D integration of III-V-based radio frequency devices on Si CMOS circuits, ACS Nano 16 (2022) 9031–9040.
[12] T. Sakurai, Closed-form expressions for interconnection delay, coupling, and crosstalk in VLSI's, IEEE Trans. Electron Devices 40 (1993) 118–124.
[13] M.T. Bohr, Ieee, Interconnect scaling - The real limiter to high performance ULSI, in: 1995 International Electron Devices Meeting, I E E E, Washington, Dc, 1995, pp. 241-244.
[14] L. Brunet, P. Batude, C. Fenouillet-Beranger, M. Vinet, (Invited) 3D monolithic integration, ECS Trans. 85 (2018) 125.
[15] C. Fenouillet-Beranger, B. Previtali, P. Batude, F. Nemouchi, M. Cassé, X. Garros, L. Tosti, N. Rambal, D. Lafond, H. Dansas, L. Pasini, L. Brunet, F. Deprat, M. Grégoire, M. Mellier, M. Vinet, FDSOI bottom MOSFETs stability versus top transistor thermal budget featuring 3D monolithic integration, Solid-State Electron. 113 (2015) 2–8.
[16] R. Hu, S. Xu, J. Wang, Y. Shi, J. Xu, K. Chen, L. Yu, Unprecedented uniform 3D growth integration of 10-layer stacked Si nanowires on tightly confined sidewall grooves, Nano Lett 20 (2020) 7489–7497.
[17] P. Livi, M. Kwiat, A. Shadmani, A. Pevzner, G. Navarra, J. Rothe, A. Stettler, Y. Chen, F. Patolsky, A. Hierlemann, Monolithic integration of a silicon nanowire field-effect transistors array on a complementary metal-oxide semiconductor chip for biochemical sensor applications, Anal. Chem. 87 (2015) 9982–9990.
[18] N.P. Dasgupta, J. Sun, C. Liu, S. Brittman, S.C. Andrews, J. Lim, H. Gao, R. Yan, P. Yang, 25th anniversary article: semiconductor nanowires–synthesis, characterization, and applications, Adv. Mater. 26 (2014) 2137–2184.
[19] S. Akhtar, K. Usami, Y. Tsuchiya, H. Mizuta, S. Oda, Vapor-liquid-solid growth of small- and uniform-diameter silicon nanowires at low temperature from Si2H6, Appl. Phys. Express 1 (2008), 014003.
[20] G.F. Zheng, W. Lu, S. Jin, C.M. Lieber, Synthesis and fabrication of high-performance n-type silicon nanowire transistors, Adv. Mater. 16 (2004) 1890-+.
[21] Y. Sun, W. Qian, S. Liu, T. Dong, J. Wang, J. Xu, K. Chen, L. Yu, Unexpected phosphorus doping routine of planar silicon nanowires for integrating CMOS logics, Nanoscale 13 (2021) 15031–15037.
[22] S. Pregl, A. Heinzig, L. Baraban, G. Cuniberti, T. Mikolajick, W.M. Weber, Printable parallel arrays of Si nanowire Schottky-barrier-FETs with tunable polarity for complementary logic, IEEE Trans. Nanotechnol. 15 (2016) 549–556.
[23] J.M. Halpern, B. Wang, H. Haick, Controlling the sensing properties of silicon nanowires via the bonds nearest to the silicon nanowire surface, ACS Appl. Mater. Interfaces 7 (2015) 11315–11321.
[24] A.P. Cao, E.J.R. Sudholter, L. de Smet, Silicon nanowire-based devices for gas-phase sensing, Sensors 14 (2014) 245–271.
[25] Q. Li, S.-M. Koo, M.D. Edelstein, J.S. Suehle, C.A. Richter, Silicon nanowire electromechanical switches for logic device application, Nanotechnology 18 (2007), 315202.
[26] H. Zhu, J.E. Bonevich, H. Li, C.A. Richter, H. Yuan, O. Kirillov, Q. Li, Discrete charge states in nanowire flash memory with multiple Ta2O5 charge-trapping stacks, Appl. Phys. Lett. 104 (2014), 233504.
[27] R.A. Puglisi, C. Bongiorno, S. Caccamo, E. Fazio, G. Mannino, F. Neri, S. Scalese, D. Spucches, A. La Magna, Chemical vapor deposition growth of silicon nanowires with diameter smaller than 5 nm, ACS Omega 4 (2019) 17967–17971.
[28] Y. Wang, V. Schmidt, S. Senz, U. Gosele, Epitaxial growth of silicon nanowires using an aluminium catalyst, Nat. Nano 1 (2006) 186–189.
[29] J. Westwater, D.P. Gosain, S. Tomiya, S. Usui, H. Ruda, Growth of silicon nanowires via gold/silane vapor-liquid-solid reaction, J. Vac. Sci. Technol. B 15 (1997) 554–557.
[30] L. Yu, P.-J. Alet, G. Picardi, P. Roca i Cabarrocas, An in-plane solid-liquid-solid growth mode for self-avoiding lateral silicon nanowires, Phys. Rev. Lett. 102 (2009), 125501.
[31] L. Yu, P.R. i Cabarrocas, Growth mechanism and dynamics of in-plane solid-liquid-solid silicon nanowires, Phys. Rev. B 81 (2010), 085323.
[32] L. Yu, M. Oudwan, O. Moustapha, F. Fortuna, P.R.i. Cabarrocas, Guided growth of in-plane silicon nanowires, Applied Physics Letters, vol. 95 (2009) p. 113106.
[33] M. Xu, Z. Xue, L. Yu, S. Qian, Z. Fan, J. Wang, J. Xu, Y. Shi, K. Chen, P. Roca i Cabarrocas, Operating principles of in-plane silicon nanowires at simple step-edges, Nanoscale, vol. 7 (2015) pp. 5197-5202.
[34] M. Xu, J. Wang, Z. Xue, J. Wang, P. Feng, L. Yu, J. Xu, Y. Shi, K. Chen, P. Roca i Cabarrocas, High performance transparent in-plane silicon nanowire Fin-TFTs via a robust nano-droplet-scanning crystallization dynamics, Nanoscale, vol. 9 (2017) pp. 10350-10357.
[35] T.G. Dong, Y. Sun, Z.M. Zhu, X.X. Wu, J.Z. Wang, Y. Shi, J. Xu, K.J. Chen, L.W. Yu, Monolithic integration of silicon nanowire networks as a soft wafer for highly stretchable and transparent electronics, Nano Lett. 19 (2019) 6235–6243.
[36] X. Song, T. Zhang, L. Wu, R. Hu, W. Qian, Z. Liu, J. Wang, Y. Shi, J. Xu, K. Chen, L. Yu, Highly stretchable high-performance silicon nanowire field effect transistors integrated on elastomer substrates, Adv. Sci. 9 (2022) 2105623.
[37] R. Hu, Y. Liang, W. Qian, X. Gan, L. Liang, J. Wang, Z. Liu, Y. Shi, J. Xu, K. Chen, L. Yu, Ultra-confined catalytic growth integration of sub-10 nm 3D stacked silicon nanowires via a self-delimited droplet formation strategy, Small 18 (2022) 2204390.
[38] D. Nagy, G. Espiñeira, G. Indalecio, A.J. García-Loureiro, K. Kalna, N. Seoane, Benchmarking of FinFET, nanosheet, and nanowire FET architectures for future technology nodes, IEEE Access 8 (2020) 53196–53202.
[39] C.B. Maliakkal, D. Jacobsson, M. Tornberg, A.R. Persson, J. Johansson, R. Wallenberg, K.A. Dick, In situ analysis of catalyst composition during gold catalyzed GaAs nanowire growth, Nat. Commun. 10 (2019) 4577.
[40] V.A. Nebol'sin, A.A. Shchetinin, Role of surface energy in the vapor–liquid–solid growth of silicon, Inorg. Mater. 39 (2003) 899–903.
[41] B.A. Wacaser, K.A. Dick, J. Johansson, M.T. Borgstrom, K. Deppert, L. Samuelson, Preferential interface nucleation: An expansion of the VLS growth mechanism for nanowires, Adv. Mater. 21 (2009) 153–165.