

High-Performance Transparent Silicon Nanowire Thin Film Transistors Integrated on Glass Substrates via a Room Temperature Solution Passivation

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Catalytic synthesized ultrathin silicon nanowires (SiNWs) are ideal 1D channel materials to fabricate high-performance transparent and low-cost thin film transistors (TFTs) that are widely needed for flexible electronics and displays. In this work, a scalable integration of orderly array of SiNW array, with a uniform diameter of only 52 ± 4 nm, grown directly upon glass/wafer substrates, via a guided in-plane solid–liquid–solid (IPSLs) process, and passivated by a new solution oxidizing/etching cycling technique is demonstrated. This has enabled an all-low-temperature (<350 °C) fabrication of high-performance SiNW-TFTs, achieving $I_{\text{on}}/I_{\text{off}}$ current ratio and subthreshold swing (SS) of $>10^6$ and 120 mV dec^{-1} respectively, with excellent negative and positive bias stabilities. Importantly, the SiNW-TFTs fabricated on glasses with ITO/or metal electrodes demonstrate a high transparency of 90% or 73% respectively, making them ideal candidates for building the next generation of high aperture displays, transparent electronics, and augmented reality applications.

1. Introduction


High-performance transparent electronics are now finding widely and rapidly expanding applications that include flexible light-emitting diode,^[1–3] displays,^[4–6] and electronic skin,^[7–9] augmented reality (AR) displays,^[10–12] which all demand high-performance transparent thin film transistors (TFTs) to drive the liquid crystal display (LCD), active matrix organic light-emitting diode (AMOLED) or micro LED units.^[13–17] To meet

the needs of high-definition and high-frequency displays, the mature large-area amorphous silicon (a-Si)^[18–19] TFTs are limited by their low mobility, while the low-temperature poly-silicon (LTPS) TFTs, with a much higher mobility,^[20–21] suffer from a high leakage current due to the randomly distributed grain boundaries.^[22–23] Though the indium-gallium-zinc-oxide (IGZO) TFTs^[24–26] represent a good compromise between mobility and scalability, they are derived from a much complex 4-element-compound-material system with still moderate mobility.

Recently, quasi-1D semiconducting metal oxide nanowire,^[27–28] carbon nanotube (CNT),^[29–30] and Si nanowires (SiNWs)^[31] have been intensively investigated for high-performance TFTs, thanks to their high surface-to-volume ratio, high crystallinity and excellent electrostatic

modulation capability in a fin-gate configuration.^[32–33] On the other hand, since the diameters of these 1D NWs/CNTs are much thinner than the visible wavelengths, a sparse array of such slim channels scatters only slightly the transmitted light, which is particularly attractive for transparent electronic applications. For these reasons, a variety of NWs/CNTs have been explored for TFT applications. For example, synthetic CNTs grown via chemical vapor deposition (CVD) at 900 °C were transferred by using thermal release tape or spin-coated onto a glass substrate to fabricate TFTs devices.^[29] SiNWs grown via vapor–liquid–solid (VLS) mechanism at 700 °C were collected and spin-coated upon the glass/flexible substrate to fabricate flexible SiNW TFT devices.^[34–35] Similarly, 1D NWs of ZnO, In₂O₃, or SnO₂ grown upon transparent glasses have been explored to serve as the active TFT channel layer.^[27–28,36] However, among all these grown-and-transferred NWs/CNTs, a precise position and ordering control of these 1D channels is still lacking, and the NW-channels are actually composed of randomly oriented and mutual crossed percolative network of NWs/CNTs. These unstable and random NW-crossing connection can greatly degrade the overall electronic transport performance of the TFTs,^[37] when compared to their high device performance verified in the single-NW or CNT TFT prototypes.^[9,38–39] To fulfill the potential of these 1D semiconducting channels, it is imperative to accomplish a rather

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precise integration of these tiny NWs, into orderly array with pre-known locations, channel numbers, and uniform diameter, as well as a sufficient length of all the individual NWs to span the full Source/Drain electrode gaps, without any random NW-to-NW crossing. Ideally, these 1D NW channels should be fabricated or grown directly upon transparent glass substrates, via an all-low temperature process, that's <450 °C to be compatible for large area electronics fabrication on glass substrates, without the need of the any sophisticated post-growth transferring or arrangements.

In our previous works, an in-plane solid liquid-solid (IPSLs) growth mechanism^[40–42] has been proposed to address these challenges, where indium (In) catalyst droplets were employed to produce self-aligned SiNW array upon planar substrates at a rather low temperature of <350 °C, by consuming precoated amorphous Si (a-Si) precursor layer deposited by plasma enhanced chemical vapor deposition (PECVD). However, in order to remove the remnant a-Si layer, a H₂ plasma was usually used to etch off selectively the remnant a-Si, which causes frequently surface damage on the exposed sidewalls of crystalline SiNWs.^[43] Though this damaged layer can be passivated by a simple oxidation at 850 °C for 15 min to demonstrate a series of high-performance SiNW TFTs,^[32,37,44–45] this high

temperature passivation is not compatible with the large area TFT fabrication on glass or polymer substrates. So, in this work, we develop a room temperature (RT) solution oxidation-etching cycling technology to passivate the orderly ultrathin SiNW with a diameter of $D_{\text{NW}} \approx 50$ nm. It is found that the RT solution passivation can help to achieve a high $I_{\text{on}}/I_{\text{off}}$ current ratio and subthreshold swing (SS) of >10⁶ and 120 mV dec⁻¹, respectively, with excellent negative and positive bias stabilities, while the SiNW-TFTs with ITO/or metal electrodes fabricated on glasses demonstrate a high transparency of 90%/or 73%, which particularly suitable for the high aperture, transparent displays or augmented reality applications.

2. Results and Discussion

As illustrated schematically in Figure 1a, AR and virtual reality (VR) glasses are emerging as next-generation interactive displays with the ability to provide vivid 3D visual experiences, which require TFTs to drive display units. For large-area AR/VR display, the scalable low temperature is critical. On the other hand, SiNWs are ideal channel for a fin-gate configuration, as shown in Figure 1b, where SiNWs has very efficient

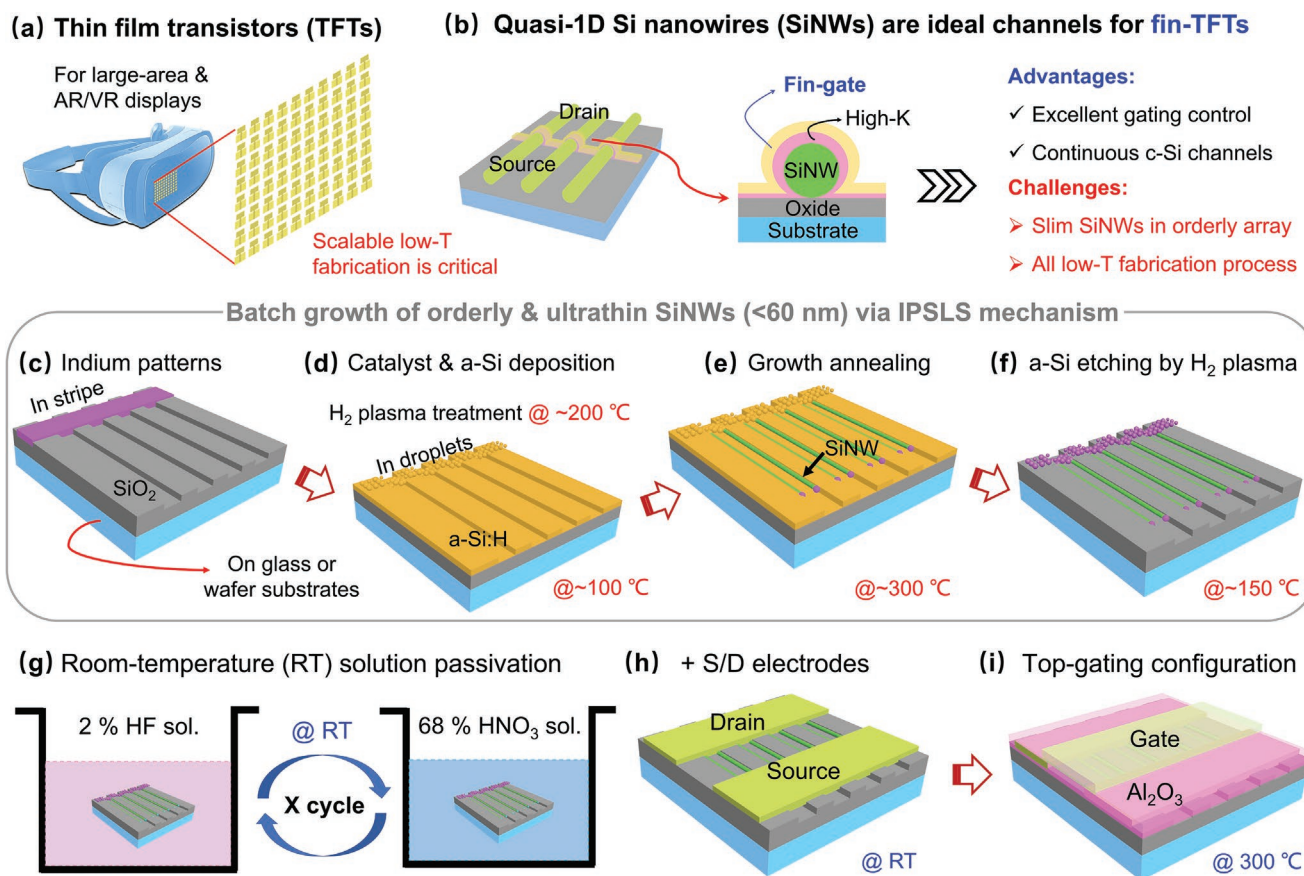


Figure 1. a) Schematic illustrations of the transparent TFTs directly fabricated and integrated upon curved or flexible glass substrates for AR/VR applications, with an advantageous fin-gate configuration and SiNW channels, as depicted in (b). c–f) Diagram the typical IPSLS guided growth of orderly and ultrathin SiNW array upon glass or wafer substrate, while g) illustrates the solution oxidation-etching cycling passivation of the as-grown SiNWs, after the H₂ plasma etching of the remnant a-Si layer (f), followed by h–i) the deposition of source/drain electrodes, dielectric layer and the top-gate electrode formation.

gating control and high crystallinity 1D channels, will enable reliable batch-manufacturing of high-performance Fin-TFTs. However, how to grow even thinner SiNW 1D channels to accomplish all low temperature fabrication is the key challenge. Figure 1c–f shows the catalytical growth of orderly and ultrathin SiNW arrays via IPSLS mechanism, upon the SiO₂ buffer layer (≈300 nm) upon a glass or wafer substrate. Briefly, the guiding edges with a depth of ≈100 nm were first prepared on the buffer layer by using photolithography and inductively coupled plasma (ICP) etching. Then, In stripes of 6 nm thick fabricated by photolithography, thermal evaporation, and standard lift-off procedure, as indicated in Figure 1c. After that, the sample was loaded into a PECVD system for a H₂ plasma treatment at 200 °C, which reduces the thin oxide layer of In and allows them to aggregate into discrete droplets, followed by the coating of ≈10 nm a-Si:H thin film at 100 °C (Figure 1d). In the next step, the samples were annealed at 300 °C for 1 h in a high vacuum for SiNW growth, where the catalyst droplets move along the guiding edges and absorbed the nearby a-Si:H to produce crystalline SiNWs behind (see Figure 1e). At the end, the remnant a-Si layer was selectively etched off by H₂ plasma at 150 °C (Figure 1f).

The room-temperature solution passivation of the as-grown SiNWs is diagrammed in Figure 1g. Briefly, the samples were first immersed into a 2% HF solution to remove the oxide layer on SiNW surface. After washing with deionized water, the samples were transferred into 68% HNO₃ solution to form a thin layer of SiO₂ on SiNW surface. The solution oxidation-etching cycling was repeatedly operated in one or two cycles. Note that, the passivation procedure should be ended at the HNO₃ solution treatment to form a SiO₂ layer as a buffer layer to contact the following Al₂O₃ dielectric. Then, the source and drain electrodes (Pt/Au or ITO) were prepared via electron beam evaporation (EBE) and lift-off procedure (Figure 1h), followed by the deposition of Al₂O₃ gate dielectric layer by using PECVD and the preparation of the top gate (Al or ITO) electrodes (Figure 1i). Note that, when a group of parallel SiNWs was taken as the channels in a single TFT device, the individual SiNWs are gated in a fin-like configuration, as diagrammed in Figure 1b. Finally, the SiNWs TFTs were loaded into a furnace and treated at 350 °C. More experimental details and explanations were provided in the Experimental Section.

A field-emission scanning electron microscopy (SEM, Zeiss Sigma) characterization of the typical SiNWs, grown along the guiding edges patterned on a wafer substrate, is shown in Figure 2a. It's found that the SiNW array, tinted to green for the ease of observation, is rather orderly and uniform with a mean diameter of only $D_{\text{nw}} = 52 \pm 4$ nm (see the statistics in Figure 2b). Meanwhile, the IPSLS SiNWs can also be grown directly upon glass substrate, as witnessed in Figure 2c, where a 300 nm SiO₂ buffer layer was pre-coated on the Corning glass surface. However, the SiNWs grown on a glass substrate manifest somehow larger diameter variation with $D_{\text{nw}} = 56 \pm 8$ nm, as shown in Figure S1 (Supporting Information). Further on, Figure 2d provides the SEM image of a single unit of the as-fabricated SiNW-TFT upon the glass substrate, where the marked regions of Source, Drain, and Gate electrodes are of Pt/Au (5/55 nm) and Al (60 nm), respectively. To zoom in and

show more details of the SiNW channel region, with a length of $L_{\text{ch}} \approx 3 \mu\text{m}$ long, magnified SEM views are also provided in Figure 2e,f for the regions delineated by the dashed blue and yellow rectangles, respectively.

The as-fabricated SiNW-TFTs on glass substrate, for example, those seen in Figure 2g, look rather transparent, particularly when the metal electrodes are replaced by ITO pads. According to the transmission characterization in Figure 2h, the glass sample with only SiNW arrays on surface has a transparency close to 90% over the full visible light wavelength spectrum ranging from 400 to 1200 nm. For the SiNW TFT samples with ITO electrodes on glass substrate, the whole samples look even more transparent (see Figure 2i), and even for the sample with opaque metal electrodes, the overall transparency is ≈73% (as witnessed in Figure S2, Supporting Information), which is sufficient for most transparent electronics and AR/VR display applications.^[46]

The typical transfer and output characteristics of the SiNW-TFTs fabricated on the wafer substrates, via an all-low-temperature (<350 °C) growth and solution passivation process (for two cycles) at RT, are first presented in Figure 3a,b, where the p-type transfer property arises from the incorporation of In atoms into the c-SiNW channels during the IPSLS growth.^[42,47] Under $V_{\text{ds}} = 0.5$ V bias, a high On/Off current ratio of $\approx 4 \times 10^6$ and a steep SS of 120 mV dec⁻¹ have been achieved. In parallel, the electrical characterizations of the SiNW-TFTs, fabricated directly on the glass substrates, are shown in Figure 3c–f. In order to assess the repeatability of the SiNWs-TFTs, 50 transfer curves of different SiNW-TFT devices are collected and presented together in Figure 3e, while a typical one with an $I_{\text{on}}/I_{\text{off}}$ ratio of $\approx 10^5$, SS of 175 mV dec⁻¹ and with little hysteresis in forward and backward scans, is singled out in Figure 3f. It is noteworthy that, according to the nonlinear $I_{\text{ds}}-V_{\text{ds}}$ curves measured under $V_{\text{gs}} = 0$ V on both the wafer and the glass substrates (see Figure S3, Supporting Information), the S/D Pt/Au contacts to the p-type SiNW channels form a pair of typical Schottky barrier (SB) junctions, with a bandgap alignment profile depicted schematically in Figure 3g. In this situation, the hole current transport through the p-type SiNW channels is basically blocked by such a pair of back-to-back connected SB junctions, under zero or positive ($V_{\text{gs}} \geq 0$ V) gating biases. But when a negative gating voltage is applied ($V_{\text{gs}} < 0$), the triangle SB is dragged upward in the band profile and thus becomes thinner, while more and more holes are accumulated in the p-type SiNW channels. This greatly thinner SB thus allows the holes to easily tunnel through the triangle barriers and travel through the p-type SiNW channels, leading to an abrupt On current status.

Furthermore, the stabilities of such SB-contacted SiNW TFTs were testified under positive bias stress (PBS) and negative bias stress (NBS) and presented in Figure 4a,b. It is found that under stress duration up to 1500 s under $V_{\text{ds}} = 0.1$ V and $V_{\text{gs}} = \pm 5$ V, for PBS and NBS respectively, the threshold voltage shifting (ΔV_{th}) under positive bias is only $\Delta V_{\text{th}}^{\text{PBS}} = 0.4$ V (Figure 4a), while the NBS shifting is negligible as seen in Figure 4b. In addition, the corresponding evolution trends of the current On/Off ratio and SS, extracted and shown in Figure 4c,d, respectively, also indicate that the electronic performances of the SiNW-TFTs fabricated via the all-low-temperature growth and

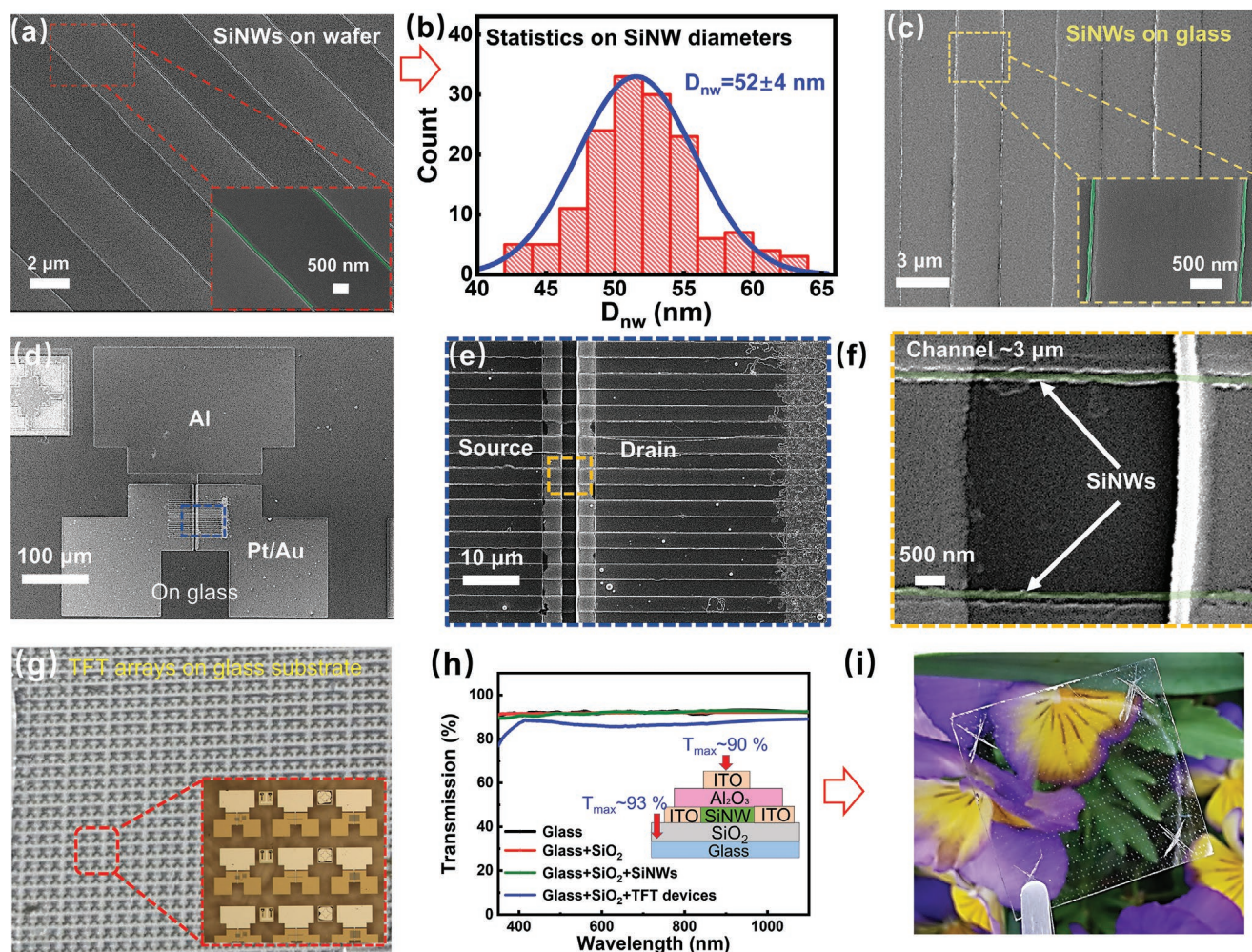


Figure 2. a) A typical SEM image of the edge-guided SiNWs on a wafer substrate, with a close examination and diameter statistics provided in the inset and (b), respectively. The SEM image of the SiNWs on glass substrate, with an enlarged view provided in (c). d–f) Provide enlarged SEM characterizations of the TFT unit on glass substrate, where only the slim guided SiNWs, with two parallel SiNWs pseudo-colored in green, away from the In stripe edges are used as the channels. g) Optical image of the array of the SiNW devices onto transparent glass substrate, with an enlarged view microscope image of the device configuration provided in the inset. h) Optical transmission spectra of the SiNWs TFTs with ITO electrode, compared to those of the reference glass substrate, with SiO₂ coating and SiNWs. The inset shows the schematic illustrations of the TFT. The red arrow points to the area of reference (93% transparent in the range). f) Provides the optical image of transparent electronics.

solution passivation process are rather stable, and comparable to those fabricated in the same batch but passivated with 850 °C oxidation for 15 min (see Figure S4, Supporting Information for example).

It is very interesting to note that the solution passivation leads to a significant improvement in the electronic transport properties of the SiNW TFTs, which gradually manifests with increased passivation cycles, as witnessed in Figure 5a,b. Specifically, the SiNW TFTs fabricated directly on the initial SiNWs, obtained after H₂ plasma a-Si etching and without any passivation cycles, demonstrate little gate modulation. With the first and the second RT solution cycles, the $I_{ds}-V_{ds}$ curves change continuously from being linear to that of typical SB type, after 1–2 cycles treatment (see Figure 5a), accompanied by the emergence of significant channel current regulation, of $I_{on/off} > 3 \times 10^5$ (Figure 5b), indicating an effective passivation on the SiNW channels.

These observations implicate that, for the initial SiNWs, the H₂ plasma etching of the residual a-Si layer around the SiNWs caused indeed sidewall damage, as schematically depicted in Figure 5c, which could be related to the dangling bonds or surface defects that are highly conductive but difficult to modulate by gating biases. In the subsequent solution HNO₃ oxidation, a superficial layer of the damaged sidewall surfaces is oxidized/consumed, and then removed in the next HF etching step, which suppresses in turn the populations of the defective sites left on the SiNW sidewalls. While one cycle of solution passivation can handle only the outermost defects, adding one more cycle seems to completely remove this damaged layer and enable a good gate-modulation of the c-SiNW channels. Also note that, after two cycle passivations, the average diameter of the SiNWs also decreased from 52 to 45 nm, a total reduction of 7 nm (see Figure S5, Supporting Information), or an etching depth of ≈3.5 nm, which is consistent to two times of the typical

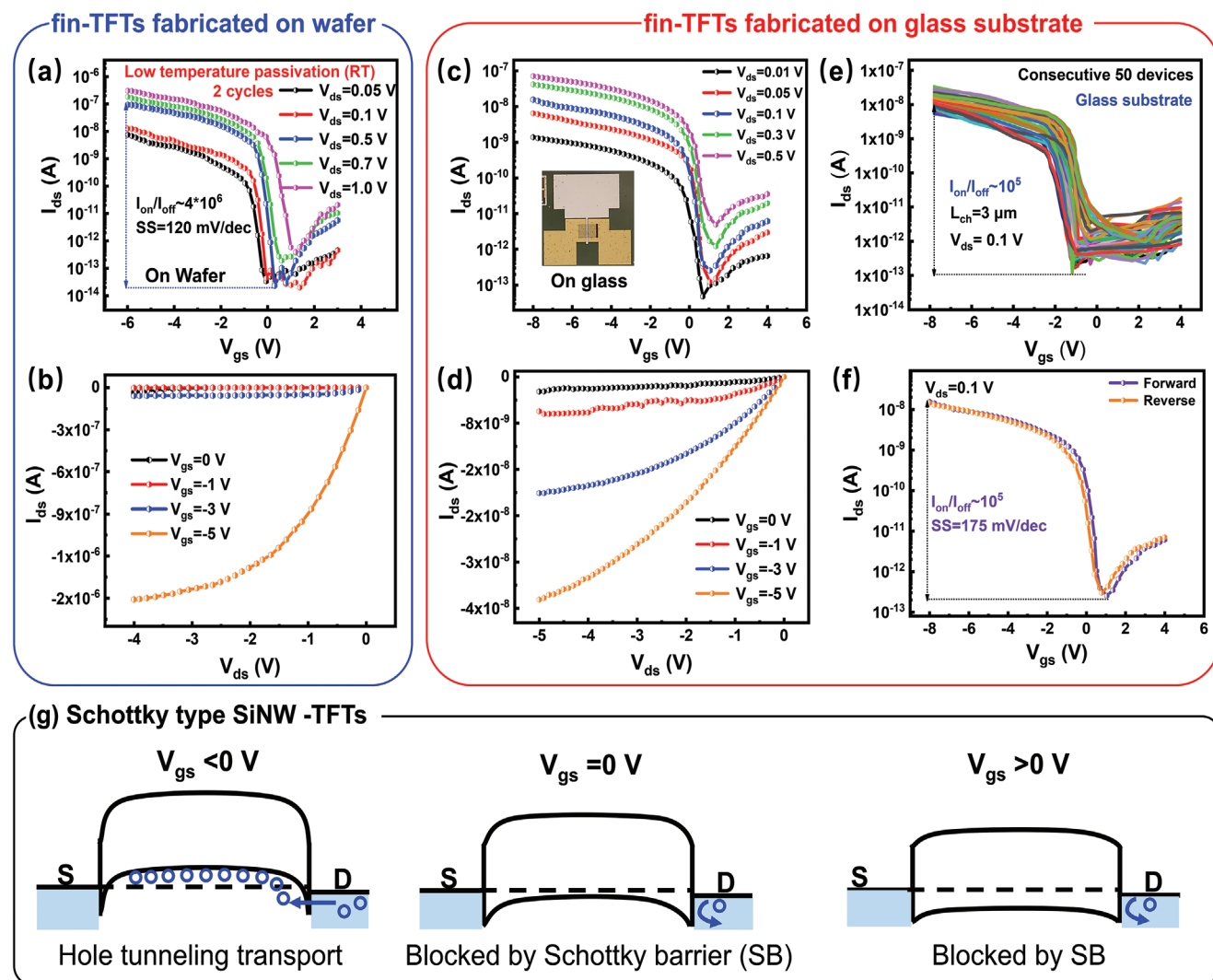


Figure 3. The electronic transport properties of the SiNW-TFTs fabricated with SiNW channels passivated by two cycles of oxidation-etching solution process on wafer a,b) or on glass c,f) substrates. e) Shows the transfer characteristics of 50 different SiNW-TFTs, while the hysteresis feature of the forward/backward scans is presented in f). g) Showcases the band gap alignment profiles under different gating bias conditions.

oxide layer thickness formed by HNO_3 oxidation of 1.5–3.5 nm reported in the literature.^[48–50] Note that, according to the transmission electron microscopy characterizations in our previous works,^[44,51] the as-grown SiNWs are polycrystalline with random twin defects in the lattice, while the low-temperature solution processing is not supposed to change the lattice quality of these SiNW channels. Importantly, the device performance of these low temperature solution-passivated SiNW-TFTs was comparable to the SiNW-TFTs passivated by using high-temperature dry oxygen oxidation process at 850 °C, as seen in Figure S4 (Supporting Information). This also implies that the as-grown crystalline SiNW channels at 350 °C have already good lattice and chemistry qualities that qualify for high performance TFT devices, without the need of post-growth high temperature annealing for crystallinity improvement or dopant activations.

Compared to the other large-area transparent TFTs reported in the literature, as summarized in Table S1 (Supporting Information), the high performance SiNW-TFTs reported here have

achieved a high transparency up to 90%, with a high $I_{\text{on}}/I_{\text{off}}$ current ratio of $>10^5$ and a small SS down to 120 mV dec^{-1} , plus that the SiNW-TFTs can be directly grown, self-positioned and batch-manufactured via a scalable all-low-temperature process that is fully compatible to the mainstream large area TFT technologies on glass or polymer substrates. In comparison, most of the CNT-TFTs are produced via VLS growth mode at much higher temperatures or require a pick-and-place manipulation or transferring processes on foreign substrates, where a precise position control of all the individual CNT has not been accomplished so far. Meanwhile, the oxide-semiconductor TFTs, particularly IGZO, have been widely investigated to serve as display driving and back end of the line (BEOL) logics,^[52–54] with high transparency, good uniformity, but moderate mobility and lacking of high-performance p-type FETs. In addition, the SiNW-TFTs represent a promising strategy to combine the high performance of LTPS TFTs with the large area and low cost a-Si TFT technology, as the growth of SiNWs demands

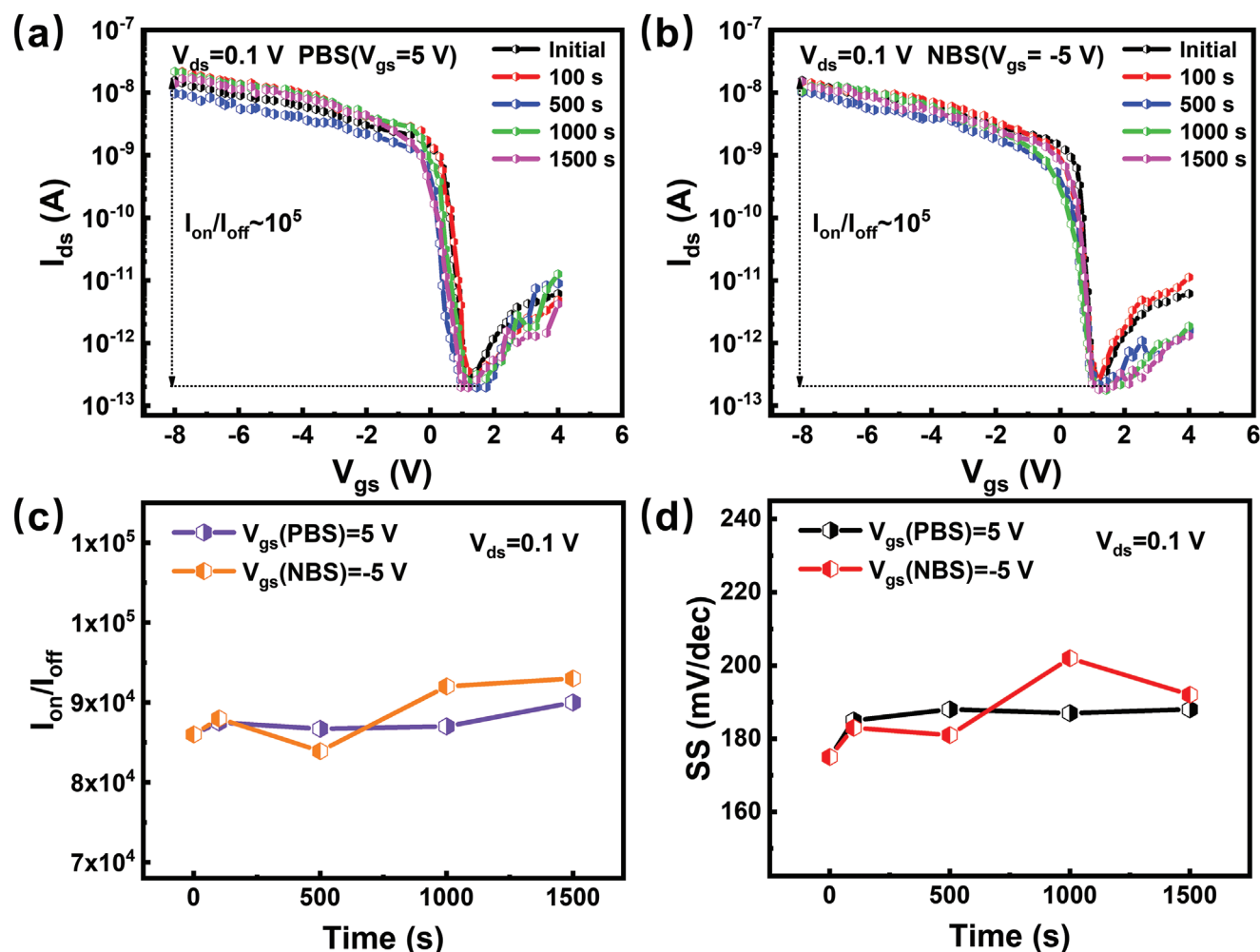


Figure 4. Temporal evolution of the transfer characteristics under a) positive bias stress (PBS) and b) negative bias stress (NBS), all measured under $V_{ds} = 0.1$ V and $|V_{gs}| = 5$ V, on glass substrates. c, d) extract and display the variation of the corresponding I_{on}/I_{off} and SS of the SiNWs TFT, respectively, under different bias stressing duration from 0–1500 s.

only conventional lithography patterning for guiding edges and rather low temperature for PECVD a-Si deposition and growth annealing, avoiding the needs of excimer laser beam scanning in LTPS that leads to challenging scan-line-stitching and limited panel sizes.^[55] For high I_{on} TFT device application, the areal density of SiNWs can be largely boosted by using multi-step terrace technology, as demonstrated in our previous work,^[32,56] which explored an alternative etching procedure to produce 12 mini-steps at the edge of a guiding step for SiNW growth, closely placed with NW-to-NW spacing of <120 nm, without the need of high-resolution lithography. Moreover, the slim SiNW channels with a diameter <50 nm are certainly advantageous building blocks for high performance fin-TFTs, which could enable eventually a new c-Si technological routine for various transparent/soft electronic applications.

3. Conclusion

In summary, a catalytic growth integration and all-low-temperature passivation of ultrathin SiNWs, with a uniform diameter of

only 52 ± 4 nm, have been demonstrated, which provide ideal 1D channels for building highly transparent and scalable high-performance TFTs. Prototype TFT devices are successfully fabricated based on the ultrathin SiNW channels, demonstrating a high I_{on}/I_{off} ratio and a small sub-threshold swing of $>10^6$ and 120 mV dec^{-1} , respectively, with excellent stabilities under negative and positive bias stresses, while the SiNW-TFTs with ITO or metal electrodes on glasses demonstrate a high transparency of 90% and 73%, respectively. These results could indicate a promising routine to integrate high performance SiNW-based nanoelectronics directly upon glass or polymer substrates for building future wearable/transparent AR/VR displays, electronics, and sensors.

4. Experimental Section

Growth of Self-Aligned SiNWs Array: The substrate was first cleaned with acetone, ethanol, and deionized water for 10 min each and then dried at 100 °C baking for 5 min. Then, a buffer layer of $\text{SiO}_2 \approx 300$ nm thick was deposited on the wafer/glass substrate for guiding edge fabrication. Typically, the deposition of the SiO_2 layer was accomplished

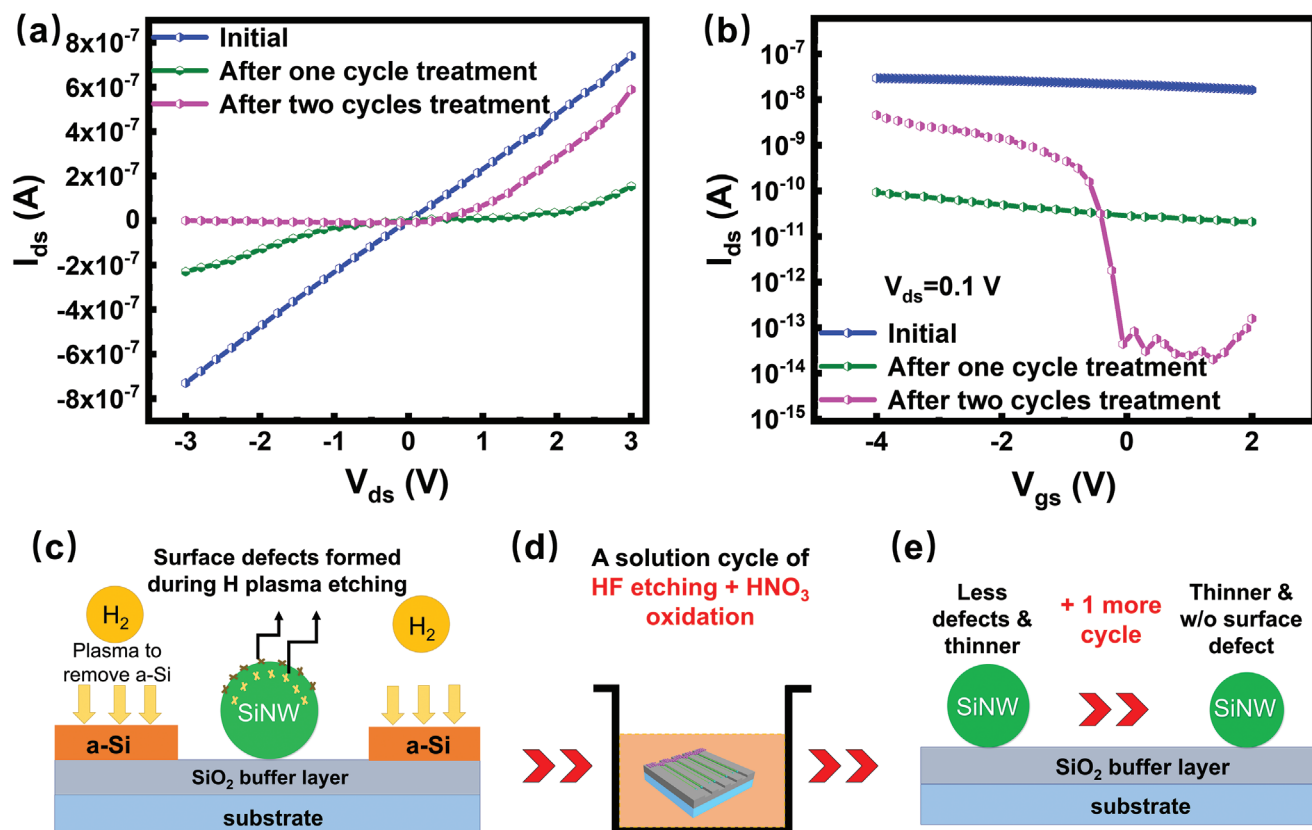


Figure 5. a,b) Show respectively the I_{ds} - V_{ds} curves and the transfer characteristics of the SiNW TFTs fabricated with initial or solution passivated SiNWs, with one or two cycles. c) Diagrams the sidewall surface damage caused by the H_2 plasma etching in the final a-Si cleaning step, which can be gradually oxidized and removed via d) a single solution cycle that consists of HNO_3 oxidation and HF etching steps at room temperature, e) while adding one more cycle is found to greatly improve the electronic transport properties in (a) and (b).

by using a gas mixture of 80 SCCM SiH_4 , 120 SCCM N_2O , and 40 SCCM N_2 at 300 °C, with a chamber pressure of 100 Pa, radio frequency (RF) power of 10 W. Second, the guiding edges with a depth of ≈ 100 nm were prepared on SiO_2 surface by photolithography and ICP etching techniques. After that, the Indium stripes with 7 μm width and 6 nm thickness were fabricated by photolithography, thermal evaporation, and lift-off procedure. In the next step, the sample was loaded into PECVD system, where a H_2 plasma treatment at 200 °C for 4 min to remove the native oxide layer on the surface of the Indium particles. The typical values for H_2 flow rate, chamber pressure, RF voltage, and RF power were 15 SCCM, 140 Pa, 15 V, and 10 W, respectively. Then, the 10 nm thick a-Si:H precursor layer was deposited at 100 °C for 3 min, with gas flow rate, chamber pressure, RF voltage, and RF power of 5 SCCM, 20 Pa, 14 V, and 2 W, respectively. In the following step, the samples were annealed at ≈ 300 °C for 1 h in a high vacuum for SiNW growth, where the catalyst droplets move along the guiding edges and absorbed the nearby a-Si:H to produce crystalline SiNWs behind. Finally, the remnant a-Si layer was removed on SiO_2 substrate by using H_2 plasma etching at 150 °C for 5 min, with typical gas flow rate, chamber pressure, RF voltage, and RF power of 15 SCCM, 140 Pa, 15 V, and 20 W, respectively. The detailed fabrication processes are shown in Figure 1c–f.

Solution Passivation of SiNWs in Solution at Room Temperature: The as-received SiNWs on SiO_2 -coated wafer/glass were alternately treated by HF and HNO_3 solution for surface passivation. First, the samples were immersed into a 2% HF solution for 10 s to remove the native oxide layer on the SiNW surface, followed by washing in deionized water and blow-drying. Then, the samples were transferred into 68% HNO_3 solution for 10 min to form a thin layer of SiO_2 at room temperature. The

solution oxidation-etching cycling passivation was repeatedly operated in one or two cycles, which was shown in Figure 1g.

Fabrication of Transparent SiNW TFTs on Glass Substrates: The source (S) and drain (D) electrode regions were first patterned by lithography, and then the exposed oxide layer on SiNW surface was removed by using 4.0% HF solution for 10 s. After that, the indium-tin oxide (ITO) electrodes (60 nm) or Pt/Au (5/55 nm) electrodes were deposited by using a magnetron sputtering or EBE system, followed by lift-off procedure. Then, the Al_2O_3 dielectric layer with a thickness of 25 nm was deposited at 300 °C by using atomic layer deposition (ALD) system, followed by the preparation of 60 nm ITO or Al gate electrodes by using magnetron sputtering or EBE system, respectively. The detailed fabrication procedures are shown in Figure 1i. Finally, the TFTs were loaded into furnace and treated at 350 °C for 30 s. The fabricated Si thin film transistors electronics were characterized with a high precision source-monitor unit (Keithley 2636B, SMU, USA). The optical measurements were made using a UV-3600 UV–vis–NIR spectrophotometer.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest

The authors declare no conflict of interest.

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

Keywords

low temperature passivation, silicon nanowire, thin film transistors, transparent electronics

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- [1] M. Choi, Y. J. Park, B. K. Sharma, S. R. Bae, S. Y. Kim, J. H. Ahn, *Sci. Adv.* **2018**, *4*, eaas8721.
- [2] J. Lewis, S. Grego, B. Chalamala, E. Vick, D. Temple, *Appl. Phys. Lett.* **2004**, *85*, 3450.
- [3] P. Gorrn, M. Sander, J. Meyer, M. Kroger, E. Becker, H. H. Johannes, W. Kowalsky, T. Riedl, *Adv. Mater.* **2006**, *18*, 738.
- [4] H. E. Lee, S. Kim, J. Ko, H. I. Yeom, C. W. Byun, S. H. Lee, D. J. Joe, T. H. Im, S. H. K. Park, K. J. Lee, *Adv. Funct. Mater.* **2016**, *26*, 6170.
- [5] J. H. Kwon, Y. Jeon, S. Choi, J. W. Park, H. Kim, K. C. Choi, *ACS Appl. Mater. Interfaces* **2017**, *9*, 43983.
- [6] T. J. Ha, *IEEE Electr. Device L.* **2016**, *37*, 1586.
- [7] M. Asadirad, Y. Gao, P. Dutta, S. Shervin, S. Sun, S. Ravipati, S. H. Kim, Y. Yao, K. H. Lee, A. P. Litvinchuk, V. Selvamanickam, J. H. Ryou, *Adv. Electron. Mater.* **2016**, *2*, 1600041.
- [8] D. W. Kim, S. Y. Min, Y. Lee, U. Jeong, *ACS Nano* **2020**, *14*, 907.
- [9] S. Y. Ju, A. Facchetti, Y. Xuan, J. Liu, F. Ishikawa, P. D. Ye, C. W. Zhou, T. J. Marks, D. B. Janes, *Nat. Nanotechnol.* **2007**, *2*, 378.
- [10] J. J. Kim, Y. Wang, H. Y. Wang, S. Lee, T. Yokota, T. Someya, *Adv. Funct. Mater.* **2021**, *31*, 2009602.
- [11] J. H. Xiong, E. L. Hsiang, Z. Q. He, T. Zhan, S. T. Wu, *Light Sci Appl* **2021**, *10*, 216.
- [12] H. Fang, J. J. Guo, H. Wu, *Nano Energy* **2022**, *96*, 107112.
- [13] T. Zhan, K. Yin, J. H. Xiong, Z. Q. He, S. T. Wu, *iScience* **2020**, *23*, 101397.
- [14] O. Cakmakci, J. Rolland, *J. Disp. Technol.* **2006**, *2*, 199.
- [15] G. A. Koulouris, K. Aksit, M. Stengel, R. K. Mantiuk, K. Mania, C. Richardt, *Comput Graph Forum* **2019**, *38*, 493.
- [16] Z. X. Pan, C. Guo, X. C. Wang, J. C. Liu, R. M. Cao, Y. F. Gong, J. T. Wang, N. Y. Liu, Z. T. Chen, L. H. Wang, M. Ishikawa, Z. Gong, *Adv Mater* **2020**, *5*, 2000549.
- [17] H. Kim, Y. T. Kwon, H. R. Lim, J. H. Kim, Y. S. Kim, W. H. Yeo, *Adv. Funct. Mater.* **2021**, *31*, 2005692.
- [18] J. J. Huang, M. H. Lee, C. J. Tsai, Y. H. Yeh, *Jpn. J. Appl. Phys.* **2007**, *46*, 1295.
- [19] M. J. Powell, C. Glasse, P. W. Green, I. D. French, I. J. Stemp, *IEEE Electr. Device L.* **2000**, *21*, 104.
- [20] C. C. Tsai, H. H. Chen, B. T. Chen, H. C. Cheng, *IEEE Electr. Device L.* **2007**, *28*, 599.
- [21] S. D. Brotherton, *Semicond. Sci. Technol.* **1995**, *10*, 721.
- [22] H. Y. Tu, Y. C. Tsao, M. C. Tai, T. C. Chang, Y. L. Tsai, S. P. Huang, Y. Z. Zheng, Y. X. Wang, H. C. Chen, T. M. Tsai, C. C. Wu, *IEEE Electr. Device L.* **2019**, *40*, 1768.
- [23] T. Goto, K. Saito, F. Imaizumi, M. Hatanaka, M. Takimoto, M. Mizumura, J. Gotoh, H. Ikenoue, S. Sugawa, *IEEE T. Electron. Dev* **2018**, *65*, 3250.
- [24] H. Yabuta, M. Sano, K. Abe, T. Aiba, T. Den, H. Kumomi, K. Nomura, T. Kamiya, H. Hosono, *Appl. Phys. Lett.* **2006**, *89*, 112123.
- [25] H. C. Wu, C. H. Chien, *IEEE Electr. Device L.* **2014**, *35*, 645.
- [26] M. Nag, F. De Roose, K. Myny, S. Steudel, J. Genoe, G. Groeseneken, P. Heremans, *J. Soc. Inf. Display* **2017**, *25*, 349.
- [27] E. N. Dattoli, Q. Wan, W. Guo, Y. B. Chen, X. Q. Pan, W. Lu, *Nano Lett.* **2007**, *7*, 2463.
- [28] G. Z. Shen, J. Xu, X. F. Wang, H. T. Huang, D. Chen, *Adv. Mater.* **2011**, *23*, 771.
- [29] F. N. Ishikawa, H. K. Chang, K. Ryu, P. C. Chen, A. Badmaev, L. G. De Arco, G. Z. Shen, C. W. Zhou, *ACS Nano* **2009**, *3*, 73.
- [30] J. L. Zhang, C. Wang, C. W. Zhou, *ACS Nano* **2012**, *6*, 7412.
- [31] Y. Cui, C. M. Lieber, *Science* **2001**, *291*, 851.
- [32] X. X. Wu, H. G. Ma, H. Yin, D. F. Pan, J. Z. Wang, L. W. Yu, J. Xu, Y. Shi, K. J. Chen, *Adv. Electron. Mater.* **2019**, *5*, 1800627.
- [33] S. Rollo, D. Rani, W. Olthuis, C. P. Garcia, *Sensor. Actuat. B-Chem.* **2020**, *303*, 127215.
- [34] S. H. Lee, T. L. Tae, M. H. Ham, S. J. Lee, J. H. Park, Y. C. Kim, P. Biswas, J. M. Myoung, *Adv. Funct. Mater.* **2015**, *25*, 6921.
- [35] M. C. McAlpine, R. S. Friedman, S. Jin, K. H. Lin, W. U. Wang, C. M. Lieber, *Nano Lett.* **2003**, *3*, 1531.
- [36] S. M. Peng, Y. K. Su, L. W. Ji, S. J. Young, C. N. Tsai, W. C. Chao, Z. S. Chen, C. Z. Wu, *IEEE Electr. Device L.* **2011**, *32*, 533.
- [37] X. P. Song, T. Zhang, L. Wu, R. J. Hu, W. T. Qian, Z. G. Liu, J. Z. Wang, Y. Shi, J. Xu, K. J. Chen, L. W. Yu, *Adv. Sci.* **2022**, *9*, 2105623.
- [38] A. Javey, J. Guo, Q. Wang, M. Lundstrom, H. J. Dai, *Nature* **2003**, *424*, 654.
- [39] Z. Y. Zhang, X. L. Liang, S. Wang, K. Yao, Y. F. Hu, Y. Z. Zhu, Q. Chen, W. W. Zhou, Y. Li, Y. G. Yao, J. Zhang, L. M. Peng, *Nano Lett.* **2007**, *7*, 3603.
- [40] L. W. Yu, P. R. I. Cabarrocas, *Phys. Rev. B* **2009**, *80*, 085313.
- [41] L. W. Yu, P. R. I. Cabarrocas, *Phys. Rev. B* **2010**, *81*, 085323.
- [42] L. W. Yu, W. H. Chen, B. O'Donnell, G. Patriarche, S. Bouchoule, P. Pareige, R. Rogel, A. C. Salaun, L. Pichon, P. R. I. Cabarrocas, *Appl. Phys. Lett.* **2011**, *99*, 203104.
- [43] M. Bauer, S. G. Thomas, *Thin Solid Films* **2012**, *520*, 3139.
- [44] M. K. Xu, J. Wang, Z. G. Xue, J. Z. Wang, P. Feng, L. W. Yu, J. Xu, Y. Shi, K. J. Chen, P. R. I. Cabarrocas, *Nanoscale* **2017**, *9*, 10350.
- [45] H. Yin, H. F. Yang, S. Xu, D. F. Pan, J. Xu, K. J. Chen, L. W. Yu, *IEEE Electr. Device L.* **2020**, *41*, 46.
- [46] C. Walko, M. J. Maibach, *Opt. Eng.* **2021**, *60*, 103103.
- [47] W. H. Chen, L. W. Yu, S. Misra, Z. Fan, P. Pareige, G. Patriarche, S. Bouchoule, P. R. I. Cabarrocas, *Nat. Commun.* **2014**, *5*, 4134.
- [48] H. Kobayashi, Asuha, O. M. , M. Takahashi, H. Iwasa, *J. Appl. Phys.* **2003**, *94*, 7328.
- [49] Asuha, S. I. , M. Takahashi, H. Kobayashi, *Appl. Phys. Lett.* **2004**, *85*, 3783.
- [50] Asuha, T. K. , O. Maida, M. Inoue, M. Takahashi, Y. Todokoro, H. Kobayashi, *Appl. Phys. Lett.* **2002**, *81*, 3410.

- [51] Z. Xue, M. Sun, T. Dong, Z. Tang, Y. Zhao, J. Wang, X. Wei, L. Yu, Q. Chen, J. Xu, Y. Shi, K. Chen, P. R. I. Cabarrocas, *Nano Lett.* **2017**, *17*, 7638.
- [52] Y. H. Sun, J. K. Kim, N. Chatterjee, S. L. Swisher, *Adv. Electron. Mater.* **2021**, *7*, 2001037.
- [53] A. Zeumault, V. Subramanian, *Adv. Funct. Mater.* **2016**, *26*, 955.
- [54] J. Z. Sheng, E. J. Park, B. G. Shong, J. S. Park, *ACS Appl. Mater. Interfaces* **2017**, *9*, 23934.
- [55] H. Zhu, E. S. Shin, A. Liu, D. Ji, Y. Xu, Y. Y. Noh, *Adv. Funct. Mater.* **2020**, *30*, 1904588.
- [56] S. Xu, R. Hu, J. Wang, Z. Li, J. Xu, K. Chen, L. Yu, *Nanotechnology* **2021**, *32*, 265602.