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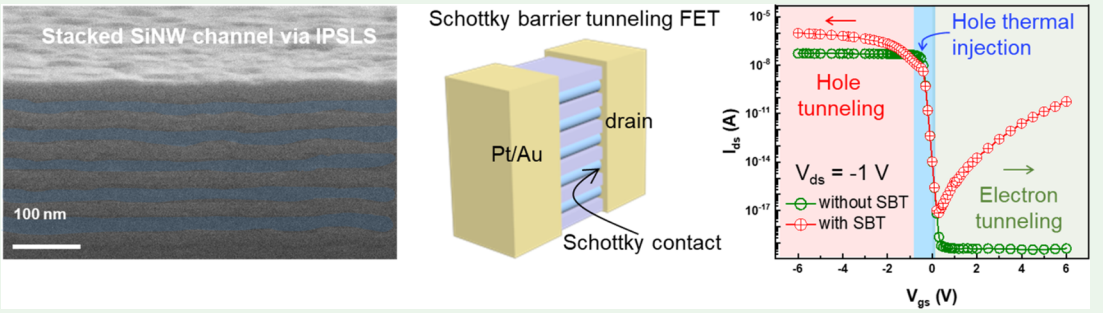
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Comprehensive Understanding of Schottky Barrier Tunneling FET Built upon Ultrathin Silicon Nanowire for Monolithic 3D Integration

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Cite This: *ACS Appl. Nano Mater.* 2024, 7, 20138−20144 Read Online

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ABSTRACT: A Schottky barrier tunneling field-effect transistor (SBT FET) built upon catalytically grown ultrathin silicon nanowires (SiNWs) offers a preferable low-temperature routine to construct top device layers for monolithic three-dimensional (3D) integration technology, but there still remain several peculiar electronic transport behaviors that need to be better understood. In this work, a high-performance SBT FET was fabricated based on orderly SiNWs grown via the in-plane solid−liquid−solid (IPSLSL) mechanism, achieving an I_{on}/I_{off} ratio of 10^6 and a SS of 150 mV/dec. The as-fabricated device, with SBT contacts between SiNWs and Pt/Au source-drain electrodes, was analyzed and compared to a three-dimensional numerical model built via the TCAD simulator to extract the actual energy band profile and the bias distribution in the SBT FET, as well as the hole carrier mobility in the catalytic SiNW channels. This comparative investigation also reveals the limiting factors for the SBT transport and explains well the observed peculiar channel-bias-dependent drain-induced barrier-lowering (DIBL) behavior. These results provide an in-depth understanding of SBT FET and lay a solid basis for its future applications in high-performance logic and in-memory computing in advanced 3D architecture.

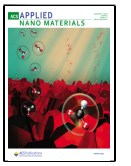
KEYWORDS: *monolithic 3D integration, silicon nanowires, Schottky barrier tunneling FET, numerical model, in-plane solid−liquid−solid*

INTRODUCTION

Monolithic three-dimensional integration,[1−3] vertically stacking multiple device layers tie by tie in a sequential fabrication process, offers a promising opportunity to increase the device density and incorporate more diverse functionalities into a given area. To ensure the integrity of the bottom front-end-of-line (FEOL) devices, the thermal budget for the top back-end-of-line (BEOL) device layers must be below 500 °C.[3−5] Thus, conventional source-drain (SD) electrode formation strategies, such as dopant activation for heavily doped SD region (>1000 °C)[5] and the selective epitaxy (700 °C)[6] methods become incompatible with top BEOL devices as diagrammed in Figure 1a. Compared with the complex process, contacting channel materials directly with metal films, composing the Schottky barrier tunneling field-effect transistors (SBT FETs), represents a low temperature and rather facile methodology to realize SD connections. Though high-performance SBT FETs have been fabricated by using carbon nanotubes,[7] transition metal dichalcogenides (TMDC),[8] and metal oxide thin film[9] as channel materials, the reliable batch transfer process or the moderate mobility has yet to be further explored and improved. To this end, it is highly desirable to seek a low-temperature strategy to obtain high-mobility channels in situ on the amorphous top layer to construct SBT FETs.

Recently, a relatively new in-plane solid−liquid−liquid (IPSLS) mechanism[10−12] has been developed, demonstrating the capability of growing planar crystalline silicon nanowires at precise locations under a low temperature of 350 °C. This is achieved by using a low-melting-point metal indium (In) as catalysts and a solid amorphous silicon (a-Si) film as the precursor, thus In droplets can be activated at a low temperature and absorb a-Si coating on the surface to produce orderly SiNWs along the guiding steps.[13−15] Remarkably, this

Received: May 21, 2024
Revised: August 7, 2024
Accepted: August 11, 2024
Published: August 22, 2024



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https://doi.org/10.1021/acsanm.4c02942
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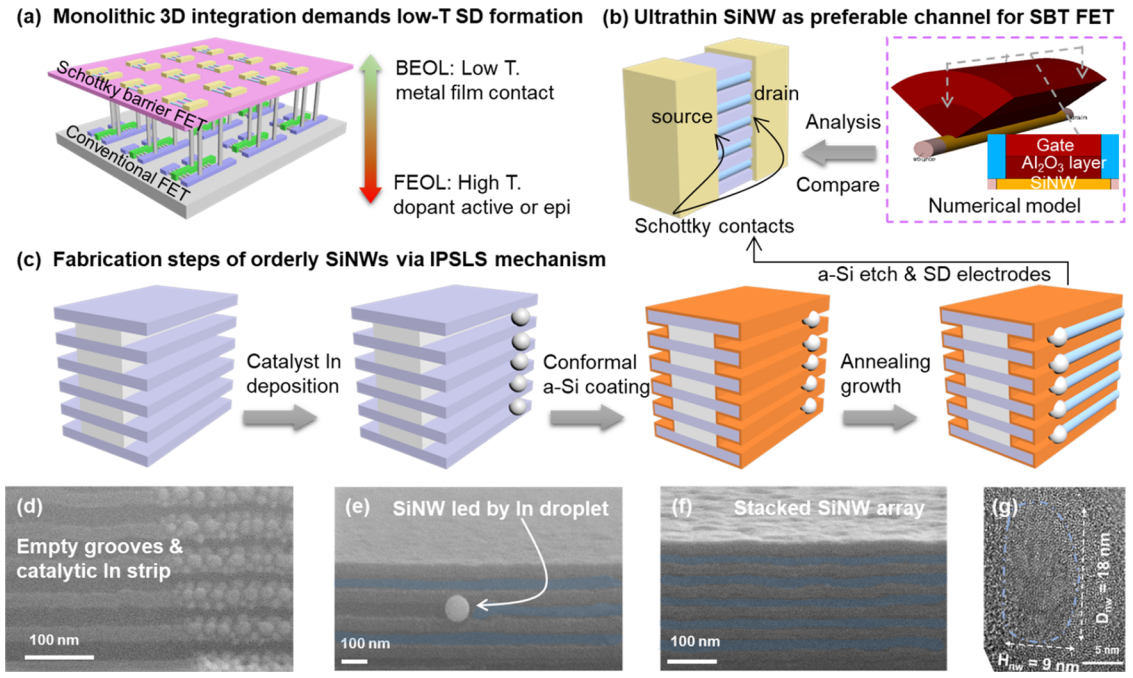


Figure 1. (a) Schematic illustration of the monolithic 3D integration technology where the low-temperature SD formation is needed for the top BEOL devices. (b) Illustration of SBT FET built upon ultrathin SiNWs with Schottky contact between channel and source-drain electrodes, where the electrical behaviors are analyzed and compared by the TCAD numerical model. (c) Major fabrication steps of stacked SiNWs grown via IPSLS mechanism. (d)−(f) Typical SEM images of the In catalyst strip and the SiNWs. (g) TEM image of the as-grown SiNW.

strategy can be extended into three-dimensional space. Vertically stacked SiNWs with diameters down to 10 nm, aiming for the gate-all-around (GAA) architecture, have been produced with excellent uniformity.[16−18] The ultrathin body would be beneficial for boosting the on current (I_{on}) of SBT FET by enhancing the carrier tunneling probability due to the formation of a thin triangular Schottky barrier, as well as decreasing the off current (I_{off}) owing to the complete depletion. Though prototype SiNWs SBT FETs have been fabricated, an in-depth understanding of the working mechanism and peculiar electrical behavior is still lacking. More importantly, the accurate mobility extraction strategy for SBT FET is yet to be established since employing the conventional metal-oxide-semiconductor field-effect transistor (MOS FET) model to calculate the value will lead to an underestimation.[19−21]

In this work, a high-performance SBT FET was fabricated based on stacked SiNW channels grown via the IPSLS mechanism. To comprehensively understand the electrical properties of the device, a three-dimensional (3D) numerical model is built via TCAD simulation, indicating good consistency with experimental data. Then, the working mechanism and the peculiar channel-bias-dependent drain-induced barrier-lowering (DIBL) behaviors are analyzed by extracting actual energy band profiles from the model. Furthermore, after validation of the model against measured data, the hole carrier mobility of the catalytic-grown SiNW is successfully derived from the transfer curve considering the effective drain bias applied to the channel region.

RESULTS AND DISCUSSION

The SBT FET device is prepared by contacting ultrathin SiNWs with Pt/Au metal film SD electrodes, as seen in Figure 1b. Since, in reality, SiNWs are embedded into the sidewall grooves, resulting in the one-side electrostatic potential control of the channel, the numerical model is developed using the single-gated structure. The schematic diagram of the as-fabricated device is demonstrated in Figure S1(a), with the cross-sectional view of the channel region depicted on the right. The model has a channel doping concentration of 10^{17} cm^{-3} according to the equivalent boron-doping verified in our previous work,[11,22] a diameter of 10 nm, an Al_2O_3 dielectric layer of 20 nm, and a source-drain work function of 5.1 eV based on the adoption of Au film. The typical fabrication procedure of stacked SiNWs is illustrated in Figure 1c. First, the vertical sidewall grooves with controllable height and space are produced by selective etching SiO_2 sublayers of SiO_2/SiN_x multilayers, followed by catalyst In strip deposition at the designated location defined by lithography. Figure 1d shows a typical SEM image of the In catalyst formed on the sidewall grooves. Then, uniform In droplets confined within the narrow grooves are formed and reduced by H_2 plasma treatment in a plasma-enhanced chemical vapor deposition (PECVD) system. After coating the whole structure with a-Si film, the growth is activated upon the annealing temperature of 350 °C, where In droplets absorb a-Si film in the grooves to produce crystalline SiNWs. The SEM images of the as-grown SiNWs are provided in Figure 1e and f, where SiNWs are pseudocolored to blue for ease of observation. Generally, the diameters of SiNWs are proportional to the size of In droplets guiding the growth, which can be found at the end of SiNW. The diameter consistency of SiNWs is guaranteed by the uniformity of In droplets and grooves, indicating the great potential of integration in CMOS technology. In order to testify to the crystallinity, a slice of stacked SiNWs is cut off via the focused ion beam (FIB) and characterized by high-resolution transmission electron microscopy (TEM), as seen in Figure 1g. The SiNW presents a monocrystalline and an elliptic cross-section with a width down to 10 nm. Finally, the Pt/Au SD electrodes

https://doi.org/10.1021/acsanm.4c02942
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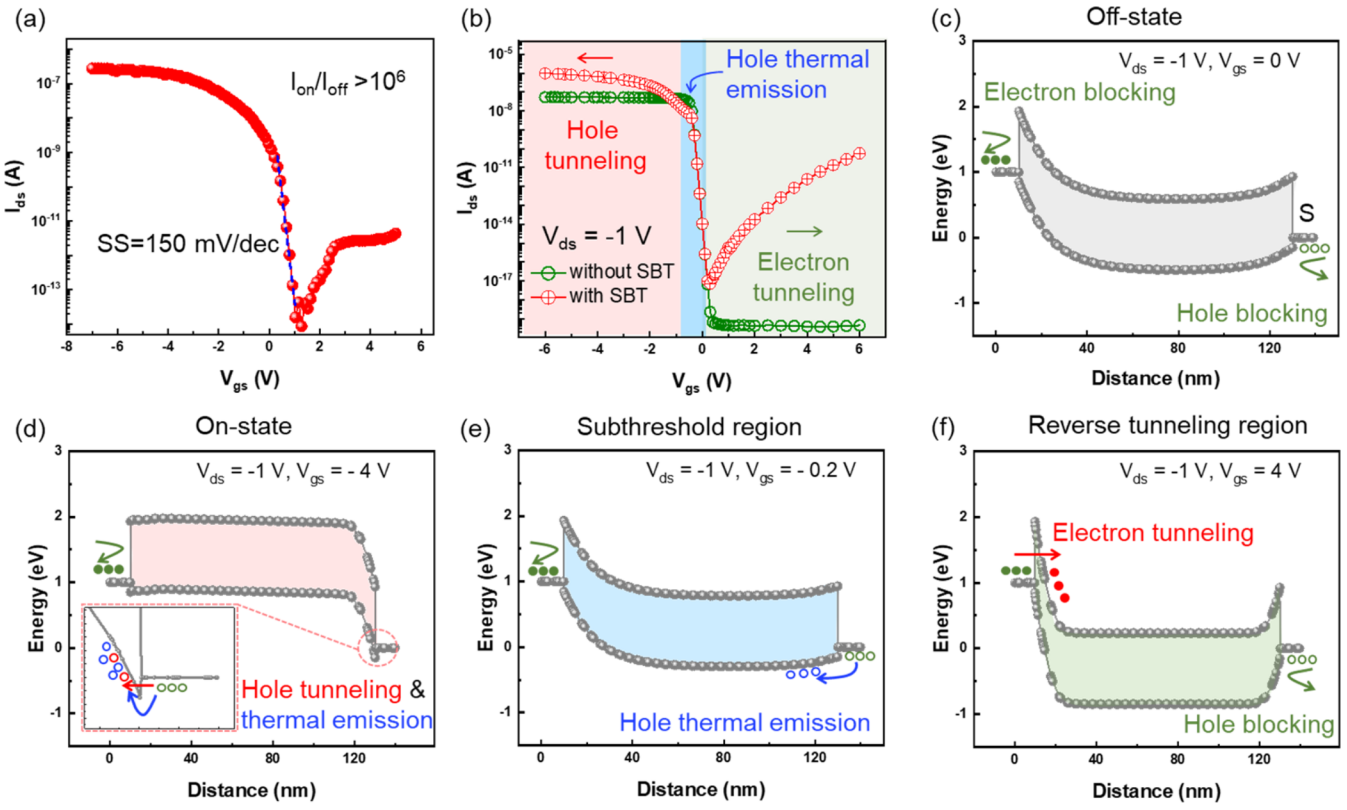


Figure 2. (a) Measured transfer curve. (b) Simulated transfer curve marked with different current domination. (c–f) Energy band profiles of SiNW SBT FET under different gate voltages extracted from the numerical model.

are patterned and evaporated after the removal of remnant a-Si film, followed by deposition of the Al_2O_3 dielectric layer and gate metal film.

Since In atoms as p-type dopants will incorporate into the SiNWs during the growth, the device shows a p-type property with an on/off ratio of 10^6 and a SS of 150 mV/dec, as demonstrated in Figure 2a. Notably, unlike the typical p-type FET, the current increases again under the positive gate voltage, suggesting a transportation mechanism different from conventional MOS FET. According to the $I_{ds} - V_{ds}$ curve inserted in Figure S1(b), the contacts between the SiNW channel and SD metal present a Schottky contact characteristic, implying a SBT FET device nature. For the numerical model, the total current flow through the Schottky junction is composed of two parts: thermal emission current determined by effective barrier height and tunneling current due to the formation of the thin triangular barrier.

The simulated transfer curve with and without considering the carrier tunneling is demonstrated in Figure 2b, showing a higher hole current at negative V_{gs} than the electron current at positive V_{gs}, coinciding with the experimental data. It is clear that carrier transportation can be divided into three stages: hole thermal emission under small negative V_{gs}, hole tunneling accompanied by constant thermal emission under large negative V_{gs}, and electron tunneling under positive V_{gs}. When negative drain bias is applied, holes are blocked by the high and wide Schottky barrier at the source end under zero gate voltage, similar to electrons at the drain end, as illustrated in Figure 2c. The energy band moves upward under the negative gate voltage, reducing the effective barrier height for holes and allowing them to step over the barrier while keeping the constant high barrier blocking the electrons, as seen in Figure 2e. The barrier height for holes decreases linearly with the negative V_{gs} until reaching the flat band voltage, indicating that the current increases exponentially at this stage. While the barrier height for holes remains constant upon the more negative gate voltage, the triangular barrier with width continually decreasing along with V_{gs}, thus enabling the hole carrier tunneling, as illustrated in Figure 2d. On the other hand, if a positive gate voltage is applied, a triangular barrier turns up at the drain end due to the bending down of the energy band, which makes it possible for the electron to tunnel through the barrier (Figure 2f). Nevertheless, the thermal emission for electrons is negligible owing to the high barrier at the drain end. Using the energy band profiles extracted from the numerical model, the working mechanism of the SiNW SBT FET is well understood.

One peculiar electrical behavior is observed when transfer curves are measured at multiple positive and negative drain biases, as shown in Figure 3a,b. The threshold voltages (V_{th}) hold constant for different negative drain biases while shifting under positive drain biases. Those unique properties of the SBT FET are different from the conventional MOS FET with Ohmic SD contacts. Consistent results are obtained for the simulated data in Figure 3c,d, implying a channel-bias-dependent DIBL characteristic. A DIBL-free behavior under negative drain biases and an obvious DIBL, here named Schottky DIBL, under positive drain biases is verified. To achieve a better understanding of this electrical mechanism for SBT FET, the energy band profiles at zero gate voltage under different negative/positive drain biases are extracted in Figure 3e and f. Besides, the Schottky barrier heights for holes and electrons are marked in Figure S2 as φ_p and φ_n, while the barrier widths are marked as W_p and W_n, respectively. Those

https://doi.org/10.1021/acsanm.4c02942
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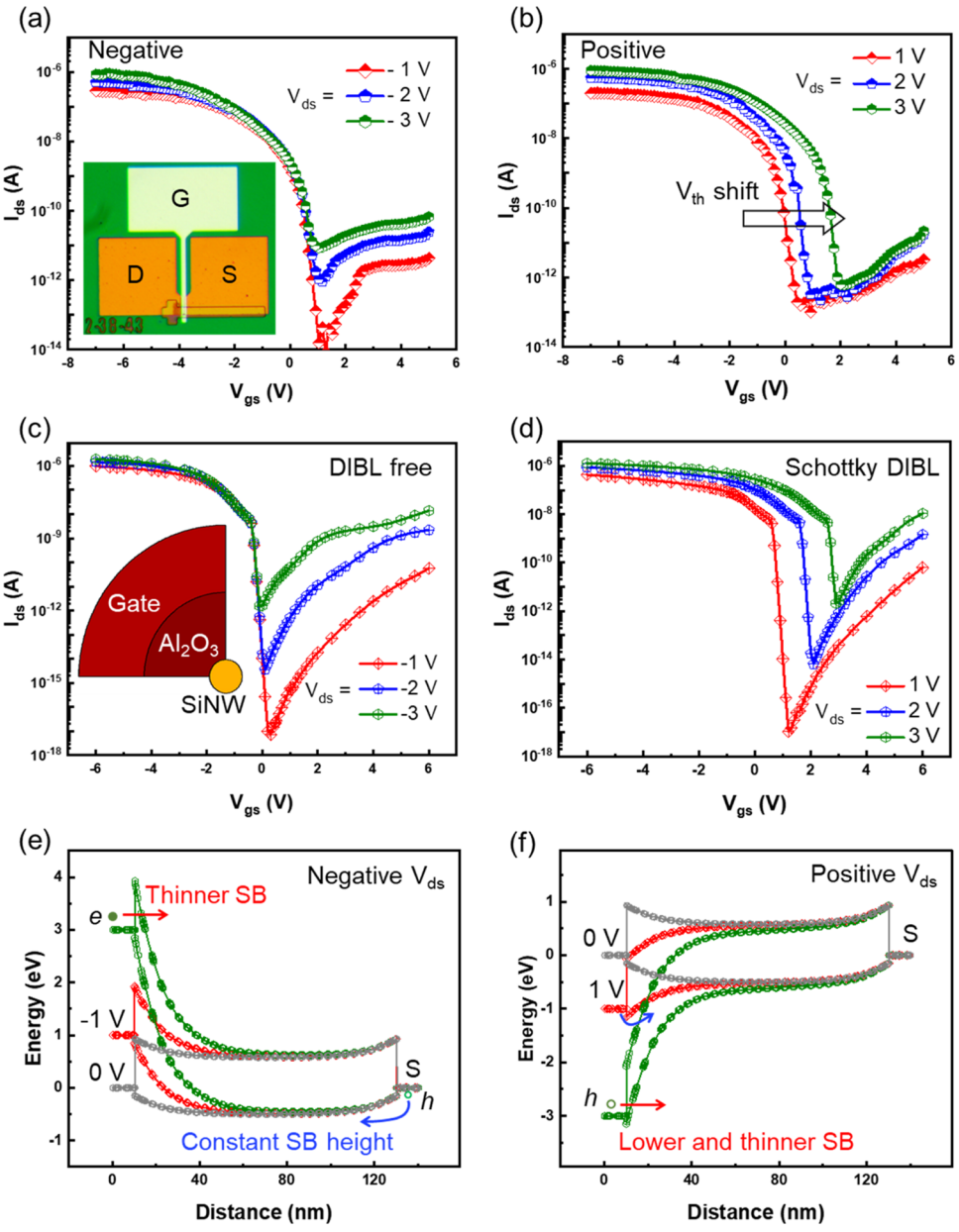


Figure 3. (a) and (b) Measured transfer properties under different negative drain biases and positive drain biases, respectively. (c, d) Simulated transfer curves. (e, f) Energy band profiles to analyze the peculiar channel-bias-dependent DIBL behavior.

four values are plotted in Figure S3, in which the red and blue values represent φ_p /W_p and φ_n /W_n, respectively. For negative drain biases, the holes are injected into the channel from the source junction while the electrons are injected from the drain junction. Since the V_{ds} drops almost completely across the drain junction at zero gate voltage verified by the potential distributions along the channel direction (Figure S4), the negative drain voltage has a negligible effect on the Schottky barrier at the source end. Therefore, the barrier height for holes remains nearly unchanged under different negative V_{ds}, resulting in the almost constant threshold voltage, as shown in Figure S3(a). But the shape of the triangular barrier on the drain end changes with V_{ds} as seen in Figure 3e. The Schottky barrier width for electrons becomes thinner for larger negative V_{ds} so that the electrons will have a better probability of tunneling, boosting the electron tunneling current, as seen in Figures 3c and S3(b). As for the positive drain biases, the holes are injected from the drain junction, instead of the source junction. Thus, the effective Schottky barrier height for holes is not only affected by the gate voltage but also by the V_{ds} drops on the drain junction. Under larger V_{ds}, the effective Schottky barrier height is decreased, accompanied by thinning of the width, as indicated in Figure S3(c) and (d). As a consequence, the thermal emission for holes, even tunneling, could occur under zero gate voltage, as seen in Figure 3f. To this end, smaller V_{gs} is required to flat the band for larger positive V_{ds}, leading to the shift of V_{th} upon different positive drain biases. Therefore, to reliably use the SBT FET as the top device for monolithic 3D integration, the p-type devices need to work under negative drain biases to avoid Schottky DIBL.

To evaluate the intrinsic properties of catalytically grown SiNW channels, the hole carrier mobility, one of the most important parameters for semiconductor materials, needs to be obtained. For a typical nanowire FET with Ohmic SD contacts,

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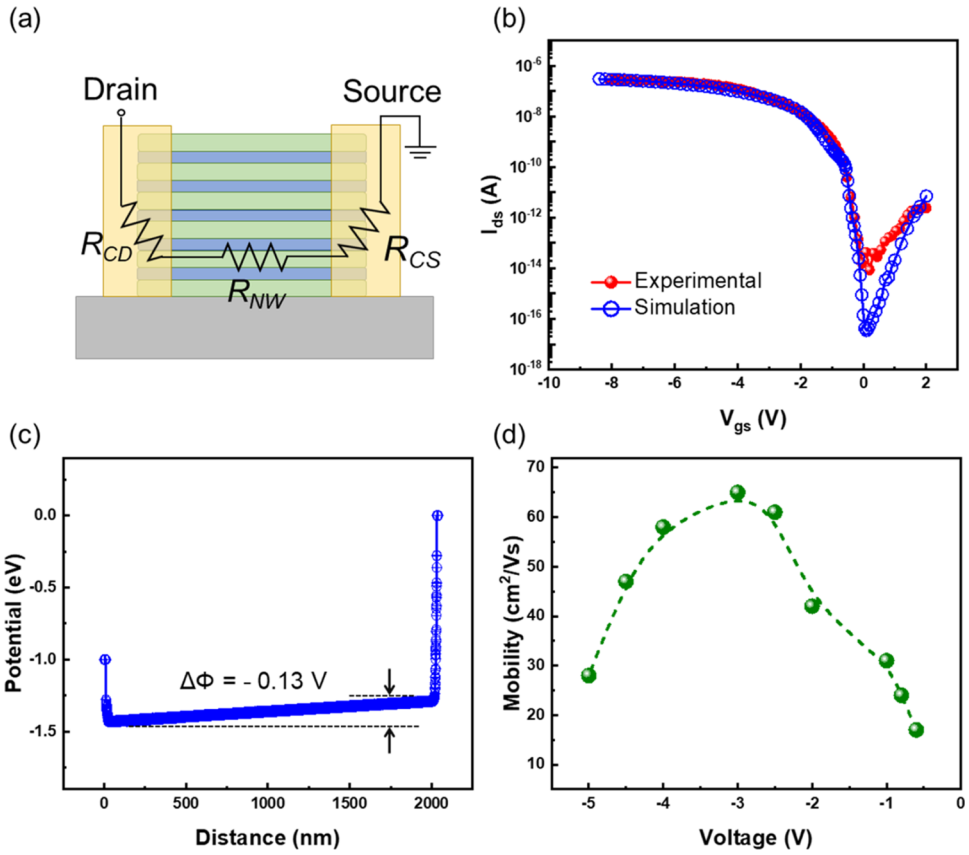


Figure 4. (a) Schematic diagram of SBT FET with the equivalent circuit, where drain bias is applied to both the channel region and contact resistance. (b) The simulated transfer curve fitting with the experimental result. (c) Potential distribution along the channel direction. (d) Calculated hole carrier mobility under different gate voltages.

the mobility of the channel can be extracted from the transfer curve using transconductance (g_m)[23,24]

$$\mu = \frac{g_m \times L^2}{C \times V_{ds}} \quad (1)$$

where μ is the mobility, C is the gate capacitance, and L is the channel length of the device.

However, for SBT FET, calculating the mobility using the equation above will underestimate the value due to the effective drain bias (V^*_{ds}) applied to the channel being much smaller than V_{ds}. Due to the existence of the Schottky barrier at the source and drain, most of the V_{ds} drops on the contact resistances, while only a small portion applies to the channel region, as illustrated in Figure 4a. To accurately obtain the V^*_{ds}, the numerical model is validated by the experimental data with a channel length of 2 μm to extract the potential distribution along the channel direction. An excellent agreement is observed, especially for the hole carrier transportation process, as shown in Figure 4b. For V_{ds} of −1 V, only −0.13 V drops across the channel upon gate voltage of −3.5 V, that is the V^*_{ds} is merely 13% of the applied value, as shown in Figure 4c. Using the corrected V^*_{ds} at different V_{gs}, hole carrier mobility is acquired by using eq 1. The mobility of SBT FET initially increases and then eventually decreases with $|V_{gs}|$, a behavior consistent with the observation in previous works.[25−27] At low $|V_{gs}|$, hole carriers may suffer from scattering due to unfilled traps and Coulomb interactions, leading to a low value of mobility. As $|V_{gs}|$ increases, the Schottky barrier is lowered, allowing more hole carriers to be injected into the channel, which fills traps and enhances Coulomb screening, thus suppressing scattering and increasing mobility. However, at higher gate biases, mobility may decrease due to enhanced surface roughness scattering and photonic scattering.[28−30] As depicted in Figure 4d, a peak value of 65 cm^2/(V·s) was achieved for IPSLS-grown SiNWs.

CONCLUSIONS

In summary, a 3D numerical model of the SiNW SBT FET has been developed and validated by the experimental data, with the electrical properties comprehensively analyzed using the band alignments, potential distribution, and extracted height and width of the Schottky barrier. The current of SBT FET is dominated by hole thermal emission at low negative gate voltage while hole tunneling plays a leading role upon more negative V_{gs}, accompanied by constant hole thermal emission current due to the fixed SB height. At positive V_{gs}, the electrons will tunnel through the thin triangular barrier from the drain end, inducing an n-branch current. Furthermore, the peculiar channel-bias-dependent DIBL behavior is understood, implying that the p-type SBT FETs need to work under negative drain biases to avoid Schottky DIBL. More importantly, a peak hole mobility of 65 cm^2/(V·s) is achieved for IPSLS-grown SiNWs, considering effective drain bias applied to the channel region. These results provide a detailed and applicable platform for understanding the characteristics of SBT FET devices and obtaining the intrinsic properties of SiNW channels with the potential of expanding to various one-dimensional and two-dimensional nanomaterials.

https://doi.org/10.1021/acsanm.4c02942
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■ ASSOCIATED CONTENT

Supporting Information

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Schematic diagram of the SBT FET device with the cross-sectional profile on the right and $I_{ds} - V_{ds}$ curve (Figure S1); band energy profiles marked with SB height and width under V_{ds} of −2 and 2 V (Figure S2); Schottky barrier height and width extracted from the simulation under negative drain biases and positive drain biases (Figure S3); the potential distribution along the channel direction under zero gate voltages with negative V_{ds} and positive V_{ds} (Figure S4); experimental methods; the parameters for SBT FET device simulation (Table S1) (PDF)

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Notes

The authors declare no competing financial interest.

■ ACKNOWLEDGMENTS

The authors acknowledged the financial support from the National Key Research Program of China under Grant No. 92164201, National Natural Science Foundation of China for Distinguished Young Scholars under No. 62325403, National Natural Science Foundation of China under No. 61974064 and No. 62304200, Natural Science Foundation of Jiangsu Province under No. BK20230562, and Innovation Technology platform project jointly built by Yangzhou City and Yangzhou University (No. YZ2020268).

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https://doi.org/10.1021/acsanm.4c02942
ACS Appl. Nano Mater. 2024, 7, 20138−20144