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Planar Growth, Integration, and Applications of Semiconducting Nanowires

Ying Sun, Taige Dong, Linwei Yu, Jun Xu,* and Kunji Chen*

Silicon and other inorganic semiconductor nanowires (NWs) have been extensively investigated in the last two decades for constructing high-performance nanoelectronics, sensors, and optoelectronics. For many of these applications, these tiny building blocks have to be integrated into the existing planar electronic platform, where precise location, orientation, and layout controls are indispensable. In the advent of More-than-Moore's era, there are also emerging demands for a programmable growth engineering of the geometry, composition, and line-shape of NWs on planar or out-of-plane 3D sidewall surfaces. Here, the critical technologies established for synthesis, transferring, and assembly of NWs upon planar surface are examined; then, the recent progress of in-plane growth of horizontal NWs directly upon crystalline or patterned substrates, constrained by using nanochannels, an epitaxial interface, or amorphous thin film precursors is discussed. Finally, the unique capabilities of planar growth of NWs in achieving precise guided growth control, programmable geometry, composition, and line-shape engineering are reviewed, followed by their latest device applications in building high-performance field-effect transistors, photodetectors, stretchable electronics, and 3D stacked-channel integration.

1. Introduction

While the miniaturization of integrated circuitry has followed the Moore's law, over the last decades, to 7 nm technology Node,[1] the highest performance/investment ratio has been left behind at the technological Node of 14 nm.[2] In face of the daunting technical challenges in top-down scaling further, seeking an efficient and natural approach to fabricate orderly nanochannels has become more urgent and relevant than ever. Actually, quasi-1D semiconductor nanowires (NWs) can be easily grown out of tiny metal catalyst droplets via a famous vapor–liquid–solid (VLS) mechanism,[3] in analogy to the seed sprouting in nature. The catalyst droplets, oversaturated with constituent atoms, mediate a layer-by-layer atomic piling deposition upon the NWs' tip, which can proceed rapidly at a rather low temperature with diameters controlled by the size of the leading droplets to even several nanometers.[4] This provides a solid basis for the construction of high performance field effect transistors (FETs), where advantageous fin-gate or gate-all-around configuration can be adopted to achieve a higher I_{on}/I_{off} current ratio, reduced leakage current and lower power dissipation. In addition, these NW-based FETs are also ideal building blocks to explore highly sensitive and responsive field effect biosensors and photodetectors.[5]

Though the VLS growth of Si or other semiconductor NWs has proven highly efficient and tunable in terms of their diameter, geometry and composition, there is still a huge technical challenge for integrating these self-assembly building blocks into the mainstream planar electronic architecture, which is and will continue to be, in a foreseeable future, the most convenient and reliable platform to prototype and deploy most of these advanced NW-based functionalities. At the root of this challenge is a fundamental incongruence between the 3D vertical growth of NWs, typically in a gas-feeding environment, and their planar (2D) alignment and integration on substrate surface. For example, Si NWs grown by using gold (Au) nanodroplets via VLS approach[3] usually stand on the substrates with somehow random orientations. Then, they have to be collected, transferred, and rearranged upon planar surface for subsequent electric connections and device fabrication.[6] However, most of these techniques are costly, sophisticated, and inefficient to apply for scalable device applications. Arranging self-assembly NWs into precise locations for integration, via an economically feasible approach, is now arguably the last technical hurdle in the way to bring the NW technologies into market place.

An in-plane or on-plane growth of NWs, constraint to substrate surface, brings not only the convenience for planar device fabrication, but also a set of unprecedented opportunities to tailor and engineer the geometry, line-shape, and growth routine of the planar NWs. For example, (1) a planar growth of NWs, with an epitaxial contact to underlying crystalline substrates, can be easily guided into specific orientations, directed by the substrate lattice ordering; (2) by adopting an amorphous thin film as precursor, the NW growth can be tightly confined to planar surface, with a series of new control strategies to modulate the diameter, doping and composition of the NWs; (3) in-plane growth of NWs

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can be better controlled with less boundary constraints, compared to that required in 3D growth, thus enabling a guided growth of NWs into predesigned locations and pathways for precise integration, or programmable line-shapes to achieve extra flexibility and stretchability; (4) a planar growth is indeed not limited to flat substrate surfaces, but also applicable to even out-of-plane and curved surfaces that are inaccessible by conventional lithography technology. These new capabilities, as well as their potentials to enable a set of new applications, such as NW-based logic gates, optoelectronics, sensors, and 3D integration circuitry, will be addressed in the following sections.

In recent years, more and more efforts have been drawn to the planar growth, arrangement, and integration of semiconducting NWs, which can be inferred from the evolution of published papers on the NW research over the last decade (**Figure 1**). These papers are searched with the key words of "semiconductor nanowires" with or without the adjective restraints of "in-plane or planar or horizontal" in Google Scholar. Note that, there are still a small portion of papers, which are published without those planar growth keywords in the title, but actually should be classified into the same group according to their reported research. It is estimated that these papers account for <5% of the total papers counted for in-plane/planar nanowires. Since the first report of Si NWs or nanowhiskers in the literature,[7] the number of research papers published every year on this topic augments steadily to more than 20 000 in 2015. In parallel, the number of papers dedicated to deploying/arranging NWs upon planar substrates or growing planar semiconducting NWs increases rapidly, with a larger and larger portion now accounting for 58% in 2018, reflecting a new focus on seeking precise growth control, arrangement, and integration of these tiny building blocks into planar architecture, particularly for the electronic, sensor and photodetector applications. So, if a reliable planar growth of NWs can be established, the transfer of accumulated knowledge and concepts of advanced NW technologies into practical applications can be greatly accelerated.

Herein, we will first examine the established key technologies for synthesis, transferring, and arrangement of vertical NWs, grown via a commonly used VLS mechanism with gas feeding, on planar substrate surface. Then, we will focus on the in-plane growth of planar or horizontal NWs, still with gas precursor feeding, but now the NWs are constraint to lateral growth by surface nanochannels or forming epitaxial interface with the underlying crystalline substrates. After that, a relatively new in-plane growth of NWs, with amorphous thin film as precursor, will be introduced, together with their unique potentials in achieving precise location, geometry, and composition controls, as well as line-shape engineering for enhanced mechanical elasticity. Finally, the latest device applications built on these planar NWs will be reviewed. As for the VLS growth mechanism of NWs by using different metal catalyst droplets, there are already several excellent reviews in the literature, and the interested readers can refer to ref. [8].

2. Planar Arrangement of VLS-Grown Nanowires

As one of the best known "bottom-up" self-assembly approaches, VLS growth mechanism was discovered in 1964 by Wagner and Ellis,[7b] but initially as an unfavorable phenomenon in Si wafer processing, where the remnant metal particles were identified as efficient catalyst to mediate the formation of elongated microwhiskers that could short-circuit neighboring electronic components. The potential of this micro- or nanoscale growth phenomenon was not fully appreciated until the advent of Nanotechnology at the end of 1990s,[8b] when researchers became fascinated with the potential of this self-assembly technology in mass-producing well-defined NW structures, with tunable diameter, ranging from several to hundred nanometers. Following the pioneering works of Charles Lieber's and his colleagues in Harvard University, a host of NW-based FET,[9] bioelectronic,[5a,b,10] sensors,[11] and even logic gate prototype devices[5c,f,12] have been demonstrated, as well as other NW-based applications in lithium ion battery,[13] photonic-crystal waveguide,[14] solar cells,[15] and nanoscale lasing.[16] However, the incorporation of these tiny NW building blocks for scalable electronic applications is not a trivial task, as the latter demands

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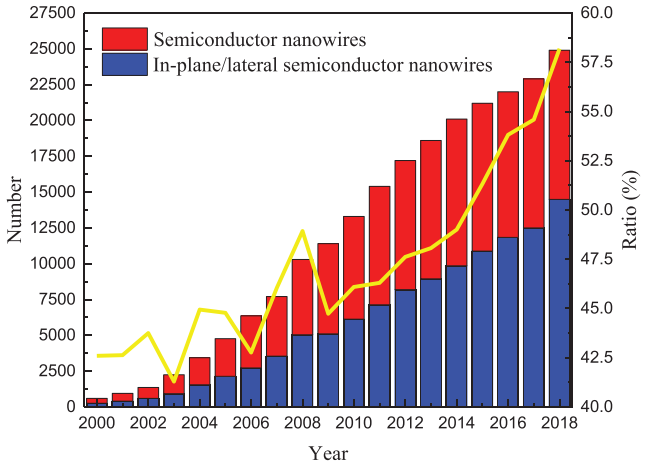


Figure 1. Evolution of the published research papers searched with the key words of "semiconducting or semiconductor nanowires" with (blue) or without (red) the adjective restraints of "in-plane or planar or horizontal" in Google Scholar, while the portion of the papers, dedicated to planar arrangement, growth or integration of semiconductor nanowires, is plotted as the yellow line. (Source: Google Scholar.)

a precise location control and the ability to deploy them in planar device architecture.

Usually, the major fabrication steps of a VLS growth procedure,[17] taking Au-catalyzed SiNW growth as example, involves: (1) first, the formation of nanodroplets of molten Au–Si alloy catalyst at a temperature above the eutectic point; (2) then, the introduction of silane (SiH_4) gas precursor that will be absorbed by the catalyst droplets to establish a supersaturation state; (3) the nucleation and precipitation of SiNW at the bottom solid/liquid interface that will kick off a unidirectional NW growth. As the precursor gas molecules are supplied from the top, a vertical growth of standing NWs is commonly observed, unless other constraints are imposed.[7b,17] This 3D vertical growth of VLS NWs brings in a fundamental challenge to integrate them in a 2D planar device architecture. In order to address this issue, the first transferring of VLS-grown SiNW to planar substrate was accomplished by using optical traps,[6o,p] contact printing,[6a–g,18] Langmuir–Blodgett,[6w,x] electric or magnetic field guidance,[6i–n,z] blown bubble film[6h,y] and microfluidic flow[6s] (see **Figure 2**). This synthesis-then-transferring technology can help to transfer and arrange SiNWs upon planar substrate, which have been widely used to prototype a variety of

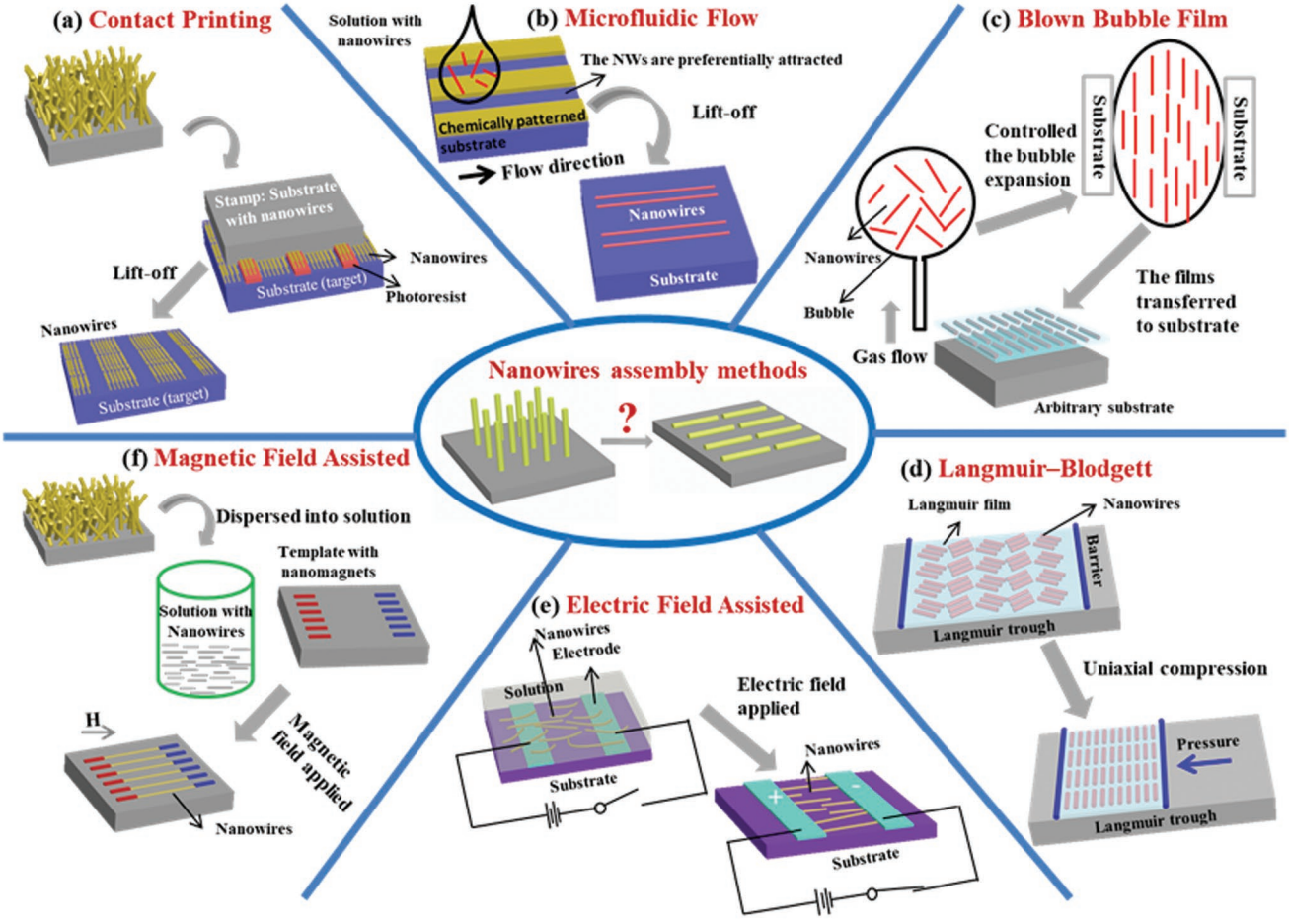


Figure 2. Various synthesis-then-assembly approaches to transfer NWs on planar substrate surfaces. a) NWs aligned by contact printing.[6f] b) Parallel NWs positioned by microfluidic flow with the aid of prepatterned microchannels.[6s] c) Transferring parallel NWs from blown bubble surface to target substrate.[6y] d) Langmuir–Blodgett assembly of NWs.[6x] e,f) Arranging polarized NWs by using electric field guidance (e)[6z] or magnetic field (f).[6j]

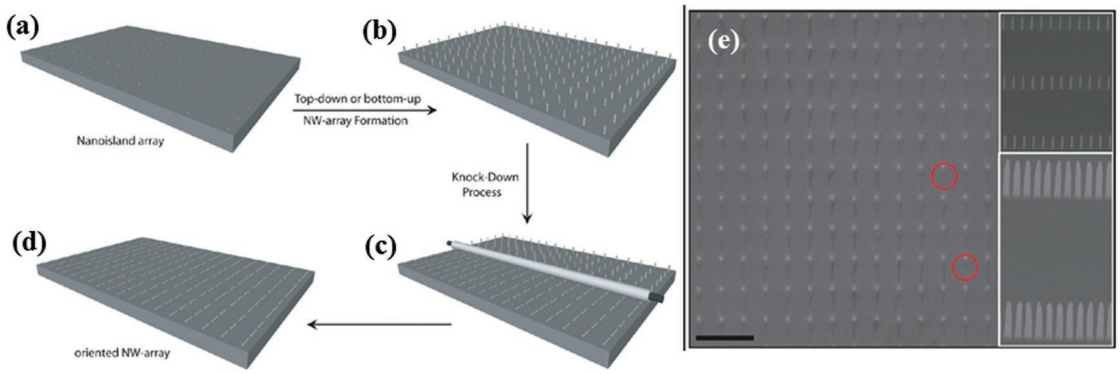


Figure 3. Schematic illustrations of the knock-down process for the fabrication of ordered NW arrays. a) Formation the ordered metal arrays that serve as masker for the top-down sculpting of nanowire arrays or as catalyst for bottom-up growth. b) Formed ordered vertical nanowires. c) Knock-down process and d) horizontal nanowires array. e) SEM images of the aligned NWs on surface. Insets: top and down are the NW array with pitch of 400 and 100 nm, respectively. The scale bar in (e) is 16 µm. a–e) Reproduced with permission.[18] Copyright 2010, American Chemical Society.

NW-based FET,[6d–f,h,l,q,s,w,y] sensor,[6a,b,g] and photodetector[6m,r] devices. However, most of them require the aids of elaborated electron beam lithography (EBL) lithography or nanomanipulators to select the specific NW and define the electrodes,[6s] which is indeed a formidable technical challenge for scalable device integration and applications.

In order to assemble the VLS-grown bottom-up NWs into specific orientations and locations, a combined fluidic alignment and surface-patterning technique was first demonstrated by Huang et al. in 2001,[6s] where VLS-grown Si, InP, and GaP NWs dispersed in solution can be deployed as self-oriented array on substrate surface, controlled by the flow direction. Further spacing control of the parallel NWs was accomplished via predefined surface patterns with NH_2-termination. This also enables a sequential layer-by-layer stacking assembly of the NWs to form crossed functional network. Interestingly, this fluidic guidance can also be extended to distribute aligned NW over large area (close to 1 cm^2) substrate, via a blown-bubble-film approach.[6h,y] This technique is applicable even to curved surfaces, with a tunable surface density of the transferred NWs controlled by the initial dispersed NW concentration in the bubble solution. Though self-alignment has been demonstrated via these flow-assisted approaches, it is still difficult to locate the NW channels precisely, in terms of their exact start-and-end places, which is however a critical requirement for reliable device integration. To address this issue, a high-yield dielectrophoresis method was developed by Freer in 2010,[6z] where balanced surface, hydrodynamic and dielectrophoresis forces can help to achieve a 98.5% yield of SiNW alignment between predefined electrode pairs under suitable bias voltage in solution. Notably, the ends of the NWs can now be precisely pinned to the opposed electrodes under the guidance of electric field, and the NW occupations on the electrode pairs are self-limiting, providing a key basis to control the exact number of NWs to serve as the semiconducting channels for reliable device fabrication. The remained challenges are the compatibility of this solution process to the standard CMOS fabrication, as well as the high fabrication cost and complexities associated with the high precision electrode pair prepatterning and delicate hydrodynamic force controls.

In pursuit of a dry transferring of the synthetic NWs, the NWs can be first grown via VLS process in a donor substrate, and then applied/transferred to the receiver substrate prepatterned with selected surface chemical treatment via a contact printing technique.[6a–g,18] (Figure 2a), the standing NWs were first detached from the donor substrates by their van der Waals interaction forces with the receiver substrate, and the alignment is primarily determined by the sliding direction. In order to minimize the NW–NW friction and protect the NWs from breakage damages during the hard-contact sliding, octane and mineral oil lubricant is needed during the transfer process. By this approach, wafer scale transferring of dense and parallel NWs can be realized with a 95% direction alignment, though the NW–NW spacing and their end-point positions are still hard to control, because of the initial random standing position of the VLS-grown NWs. Later, this problem was resolved by Pevzner et al. in 2010, via a gentle knocking-down process of orderly standing NW arrays.[18] The SiNWs were prepared via top-down etching or bottom-up growth by using an orderly array of metal droplets (**Figure 3**), which are prepatterned beforehand by using electron beam or nanoimprint lithography. After a polymer encapsulation over the SiNWs and the formation of points-of-easy-break at the ends, the NWs were knocked down by a rigid-roller to lie on the surface, with precisely controlled orientation, density, and NW dimensions. Obviously, a challenge for this dry transferring approach is to seek a trade-off between the scalability and the ordering of the transferred NWs, as the ordering of the transferred NWs is inherited from the initial vertical NW array, which has to be defined by using high cost and inefficient EBL lithography.

3. Planar-Guided Growth of VLS Nanowires

Instead of the growth-and-place deployment strategy, the NWs can also be directly grown in a planar configuration on a surface, via the same VLS mechanism. An obvious benefit is the exemption of postgrowth transferring, avoiding the solution process and the mechanical handling of the tiny and fragile building blocks. So, an in-plane growth of semiconducting NWs represents indeed a more convenient and practical approach toward integrating the self-assembled NWs into scalable electronics.

In order to confine the VLS growth of NWs to proceed on planar surface, instead of growing up in perpendicular direction to the substrate as in conventional VLS process,[7b,17] there are two principal strategies: first, the NW growth can be confined within narrow prepatterned channels lying on the substrate surface, at least during their initial growth stage; second, the NWs form a preferential bottom epitaxial interface with the underlying crystalline substrate, which can help to attract and direct the growth of NWs to proceed along specific crystallographic orientations on the substrate. Both of these strategies emphasize the key ability to direct the growth orientation of the VLS-grown NWs, which is indispensable for scalable device fabrication.

3.1. Planar VLS Growth Directed by Nanochannels

In order to confine the 1D growth of NW within a 3D space, the confinements have to be imposed in 3D−1D = 2D directions, that is by using nanochannels that allows only one direction to extend for the VLS growth of NWs. In this approach, the cross-section width of the channels has to be as thin as the NWs' diameter, which by itself is a technical challenge for nanoscale fabrication. Fortunately, the VLS growth of NWs is intrinsically unidirectional due to its crystalline nature, and the NWs will extend, once kick off, following a specific crystallographic orientation.[19] So, only the initial growth direction needs to be controlled by using surface patterned nanochannels. The first endeavor on this approach was reported by Shan and Fonash in 2008,[19b] where nanochannel templates were predefined by using EBL patterned Au nanostrips with diameter of 80 to 150 nm. Then, the Au strips were crossed and covered by a SiO_2 capping strip layer of 3 μm wide (**Figure 4**), leaving the space for the subsequent solution etching of the exposed Au strips to form empty channels inside the capping layer. A short Au segment was preserved in the middle of the channels to serve as the seeds for VLS growth of SiNWs. At last, straight SiNWs were grown out of the channels, led by Au catalyst particles, extruding from the open ends of the channels and along the initial channel directions. This approach thus enables a "growth-in-place" deployment of lateral VLS NWs with predesigned position and orientation, upon glass or wafer substrates surface, making them potentially useful channels to construct planar FET devices.

As EBL lithography and patterning of the nanochannels and catalyst stripes are expensive for large area processing, self-assembly nanopores, such as porous anodic alumina (PAA), have been explored to serve as the nanoguiding channels or molding system, where the diameter of the nanopores is readily tunable from several to hundred nanometers by adjusting the anodization parameters.[20] Xiang et al. demonstrated that high density nanopores can be formed within patterned Al electrodes deposited on planar substrate,[20c] where the pores' orientation is parallel to the substrate surface. One end of the

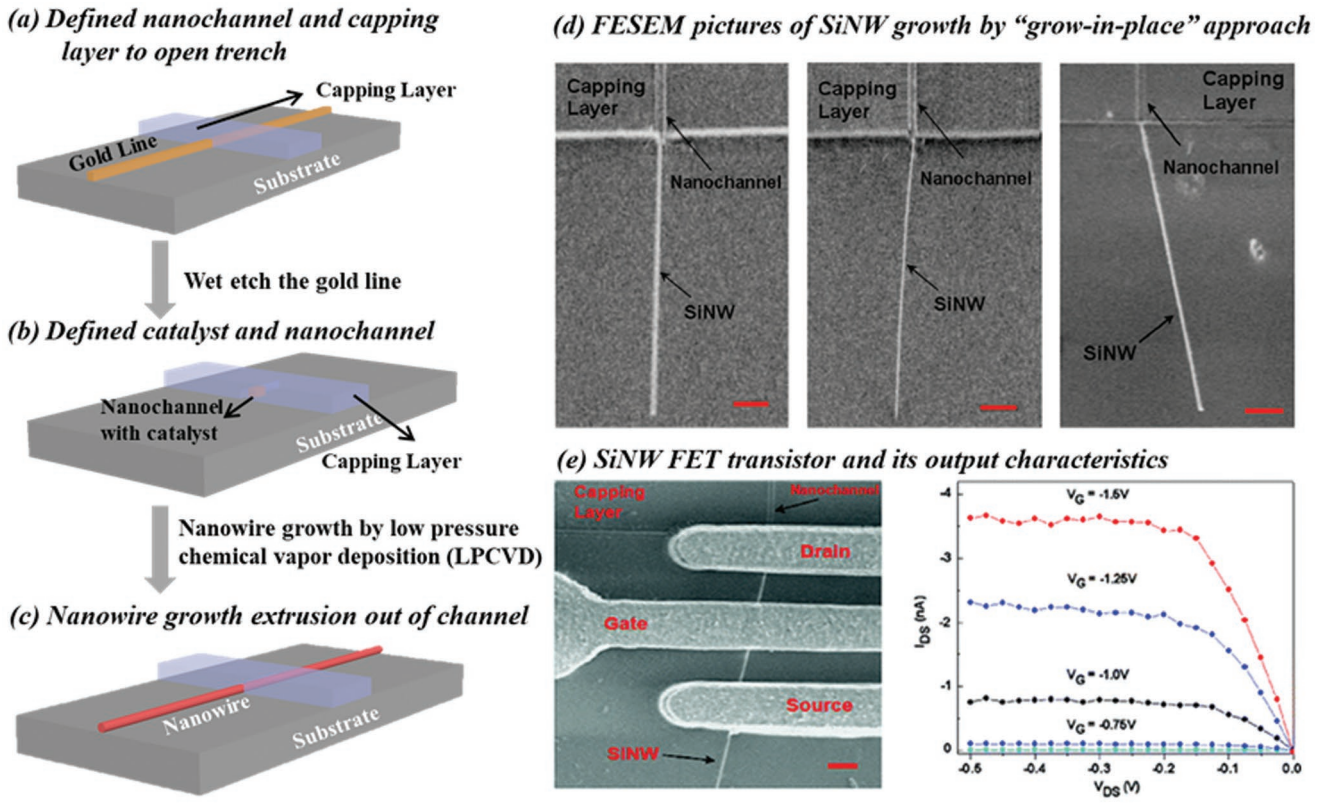


Figure 4. a–c) Fabrication procedure of the nanochannel-assisted "grow-in-place" deployment of SiNWs using guiding templates, while (d) shows the FESEM picture of the SiNWs grown out of the nanochannels. e) the configuration and output curves of a SiNW FET device. a–e) Reproduced with permission.[19b] Copyright 2008, American Chemical Society.

PAA pore array was connected to external circuitry to allow electrodeposition of short segments of metal (Au, Cu, or Ni), in different electrolyte solutions, to serve as the catalyst. Then, SiNWs were grown via conventional VLS procedure within the nanotemplates and extruded from the nanopores at the open ends. The authors also demonstrated the deposition of, as well as electric connection to, different groups of planar metal and semiconductor NWs upon the same substrate surface. Though the PAA nanopores can be small enough to serve as effective nanotemplates to confine the VLS growth of NWs, the NWs grown inside the pores are actually close-packed bundles buried within insulating Al_2O_3 dielectric, which are difficult to be selectively gated for FET applications. More recently, the PAA templates are also adopted to confine and direct the growth of lead-free perovskite NWs for high performance photodetector application.[21]

3.2. Horizontal Epitaxy-Guided VLS Growth of NWs

The challenges encountered in the synthesis and transferring of vertically grown VLS NWs to planar substrate stimulated more research efforts in search for a more straightforward approach to accomplish the growth and arrangement of NWs all in a single run operation. This has indeed become possible in 2011, when Tsivion et al. demonstrated, for the first time, an epitaxial guided growth of ultralong GaN NWs upon sapphire substrates.[22] The GaN NW growth was accomplished via a typical VLS mechanism in conventional CVD system, with Ni nanoparticles serving as the catalyst droplets and Ga_2O_3 vapor carried in N_2 and H_2 carrier gas flow as precursors. While typical vertical VLS GaN NWs were still found in the region covered with Ni catalyst pads, millimeter-long horizontal NWs were grown from the edges of Ni pads into the clean sapphire surfaces (**Figure 5**). Here, there is

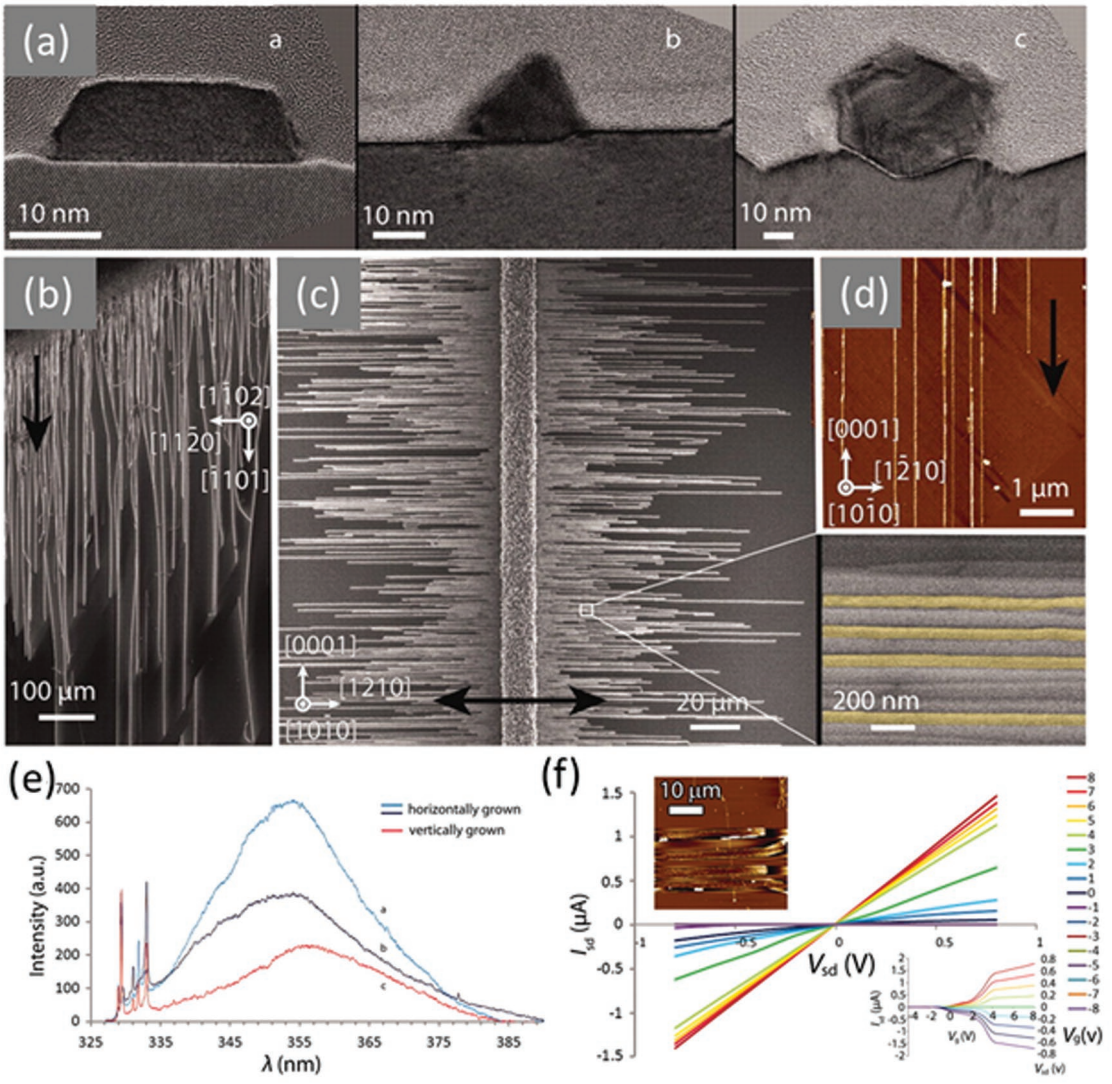


Figure 5. Epitaxial growth of horizontal GaN NWs on sapphire substrates. a) TEM cross-section analysis of the NWs epitaxially grown upon flat, L-shaped, and V-shaped nanogrooves of annealed miscut sapphire planes. b–d) The SEM and AFM characterizations of ultralong GaN NWs grown on C (0001) sapphire and annealed M (10-10) planes. e) The PL curves of horizontal GaN NWs grown on annealed M-plane (blue) and miscut C-plane (black) sapphire, and vertical GaN NWs grown on A-plane sapphire (red) under excitation wavelength $\lambda_{ex} = 325$ nm. f) Electronic transport properties of GaN NWs at room temperature. a–f) Reproduced with permission.[22] Copyright 2011, The American Association for the Advancement of Science.

no guiding channels prepatterned on the planar substrate, and the unidirectional growth of the GaN NWs is solely directed by the underlying preferential epitaxial interfaces, provided by the exposed crystalline substrate surfaces or the nanoscale corrugated facets formed upon annealing. A series of different sapphire substrates, including C (0001), miscut C-planes, M (10$\bar{1}$0), and R (1$\bar{1}$02) planes, have been explored for achieving a stable guided growth of GaN NWs, and it is found that the annealed M (10$\bar{1}$0) surface, with V-shaped nanofacets or grooves on the surface, delivered the best directional growth, thanks to a graphoepitaxial effect that encourages a maximization of the substrate/catalyst interface. This thus enables a stable planar movement of the Ni catalyst droplets and a self-aligned growth of parallel GaN NWs with little orientation deviation and few structural defects. Remarkably, the optical and electronic properties of the horizontal NWs are found to be comparable to those produced via typical vertical VLs growth, with gas precursor feeding, opening an exciting opportunity to mass-produce self-oriented semiconducting NWs for practical device applications.

Interestingly, this horizontal epitaxial growth approach has proven versatile enough to produce aligned NWs of different material systems. For instance, guided growth of horizontal ZnO NWs was successfully accomplished upon different planes of sapphire substrate in 2012,[23] followed by the reports of ZnSe,[5h] ZnTe,[24] CdSe,[25] CdS,[5g] GaN,[22,26] ZnSe,[5h,27] and SnO_2 NWs[23,28] on sapphire, InAs NWs on different substrate,[29] GaAs NWs on GaAs substrate.[29d,30] More recently, the surface-guided approach has been applied to produce parallel inorganic perovskite[31] on mica/sapphire or AuCN NWs[32] on graphene sheets, even though the growth of these planar NWs was not catalyzed by metal droplets. Note that, compared to the catalyzed epitaxial growth, the noncatalyzed growth of NWs, along the preferential axial directions, is usually accompanied with gradual sidewall expansion,[31a,b,33] making it difficult to control the NW diameter as in the case of catalyzed planar growth. On the other hand, the epitaxial growth of GaN NWs was also testified over a host of different crystal substrates, which include SiC[34] and Quartz.[35] The latter is particularly attractive as it allows for a reliable transferring of the oriented GaN or other NWs to Si wafer and glass substrates,[36] because the underlying Quartz substrate can be selectively etched off to release the epitaxially grown GaN NWs.[35] More importantly, a high yield guided growth of NWs, with nanoscale precision on the substrate, represents a crucial step toward massively deterministic assembly of the NW building blocks for electronic circuitry and logic gates. This capability has been demonstrated by Schvartzman et al. in 2013,[37] built on the guided growth of horizontal GaN NWs, where parallel NW FETs were fabricated with a high yield up to 85%.[37]

4. Planar Nanowire Growth with Thin Film Precursor

4.1. Amorphous Thin Film Precursor

As described above, a gas precursor feeding will naturally encourages a vertical growth of standing NWs, as the precursor molecules are mostly supplied from the top direction. For the epitaxial horizontal growth of VLS NWs,[3,5g,24b,25–27,28c,29a,c-e,30,34,36d,f,38] the formation of an energetically favorable bottom interface with the substrates helps to confine the leading catalyst droplets to proceed in-plane. This logic thus points to a more straightforward approach to enforce a planar growth of NWs by replacing the gas feeding with a thin film precursor on the substrate surface, as shown in **Figure 6**a, where the amorphous thin film has a higher Gibbs energy with respect to the crystalline phase of NWs, say $G^{a}_{tf} > G^{c}_{NW}$. An ideal model system is to adopt amorphous Si (a-Si) thin film as precursor to produce crystalline SiNWs, via an in-plane solid (a-Si)–liquid–solid (SiNW) (IPSLS) growth mechanism, first proposed and demonstrated by Yu et al. in 2009.[39] In this work, a low melting point metal of indium (In) was chosen as catalyst, which is considered as an alternative to the widely used Au catalyst, as the latter is known to introduce deep mid-bandgap level in c-Si that highly efficient recombination centers for minority carriers.[40]

Though this in-plane growth of SiNWs[39] adopts solid a-Si thin film as precursor, the IPSLS growth bears a similarity to the

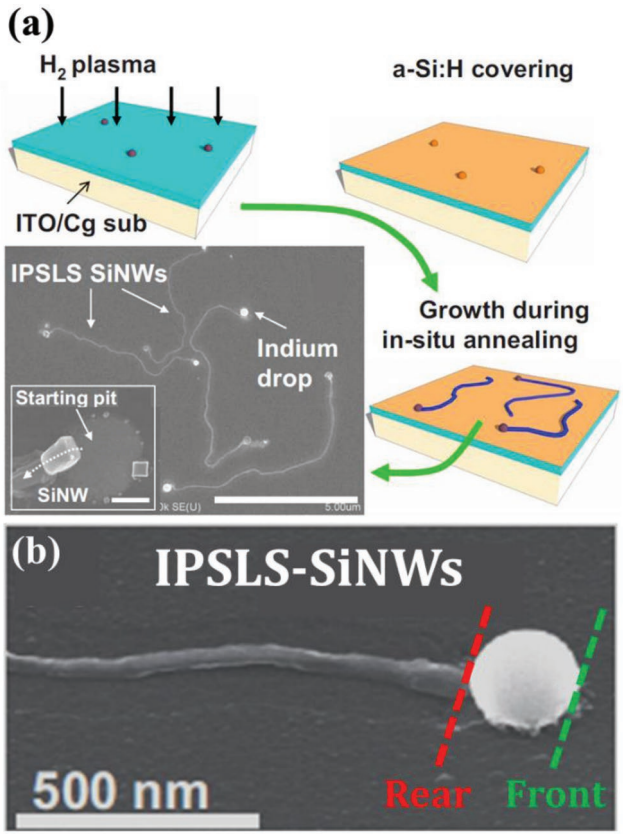


Figure 6. In-plane solid–liquid–solid growth of SiNWs with amorphous Si thin film as precursor. a) illustrates schematically the principal fabrication procedure for an IPSLS growth of SiNWs (scale bar, 5 µm) with an SEM image of the typical in-plane SiNWs shown in the inset (scale bar, 300 nm). b) A close examination of a SiNW led by a brighter In droplet. The scale bars in (a) and the inset of (a) are 5 µm and 300 nm, respectively. Reproduced with permission. a,b) Reproduced with permission.[41] Copyright 2010, American Physical Society.

VLS process: both of them are mediated by catalyst metal droplets, and the diameters of the as-grown SiNWs are both determined by the size of the leading catalyst droplets. Actually, In and tin (Sn) have been successfully used to mediate a gas-fed VLS growth of vertical SiNWs at a low temperature ≈300 °C for the construction of radial junction thin film solar cells.[42] For the IPSLS growth (Figure 6a), the first step of catalyst formation step is basically the same, where the wafer or glass substrates coated with a thin layer of In or ITO were first treated by H_2 plasma at a temperature higher than the melting point of the catalyst metal in a conventional PECVD system. This is to remove the native oxide layer on the thermally evaporated In layer, or to reduce the ITO layer to precipitate and form In droplets with relatively uniform size and distribution. The diameter of the In droplets can be readily adjusted by tuning the processing temperature, power density or the initial In/or ITO layer thickness, which are critical basses for controlling the diameter of the in-plane SiNWs.

In the next step, the substrate was cooled to a temperature below the melting point of catalyst droplets (for In it is T_m = 157 °C), followed by an a-Si coating to a thickness of t_{aSi}, by using silane plasma. The low deposition temperature guaranteed that no VLS growth of vertical SiNWs will happen, as the In catalyst droplets were frozen to solid state. After that, the substrate was heated to above 300 °C and annealed in vacuum or in H_2 ambient. During this course, the metal droplets became molten again and started to absorb the nearby a-Si to establish a supersaturation state in the In droplet. Eventually, c-Si seeds will form preferentially at the bottom edges, joint by the liquid droplet and the substrate surface, and continue to grow larger and larger to tilt the droplet to move into the opposite direction.[43] It is also found there exists a matching criteria for the a-Si layer thickness and the initial size of the catalyst droplet, in order to kick off successfully an in-plane movement of the SiNWs, otherwise the droplets could just end up with self-locked status. During an in-plane growth of SiNWs, the amorphous a-Si thin film is constantly absorbed at the front In/a-Si interface into the In droplet, while crystalline SiNW is produced at the rear SiNW/In deposition interface. Figure 6b shows a typical SEM image of the in-plane SiNW, led by a brighter In droplet ahead. Here, the driving force arises from the different Gibbs energy between the a-Si and SiNW, which is known to be around $\Delta G \approx 0.12$ to 0.15 eV,[41,43] depending on the disordering and defective states in the amorphous matrix.

Before going to the details of growth mechanism and control of the IPSLS NWs, it could be helpful, as well as necessary, for the readers to clarify two points.

First, this in-plane SLS mechanism should be distinguished from the other solid–liquid–solid growth mechanism of crystalline and amorphous SiNWs,[44] or even oxide NWs,[45] which are mostly catalyzed by using nickel (Ni) nanoparticles placed upon Si wafers at elevated temperature ranging from 900 to 1100 °C. Actually, the precursor source for the SLS growth is the c-Si substrates that were consumed by the Ni nanoparticles at the Ni/c-Si bottom interface, and then precipitated at the top Ni/NW interface, due to a sharp temperature gradient imposed by gas flow. More importantly, the NWs produced via the SLS mode are mostly vertical and random matrices, which are apparently different from the planar NWs addressed in this Review.

Second, the IPSLS growth process can be viewed as a nanoscale solid-phase-epitaxy (SPE) growth,[43] where molten In or Sn liquids are also used for depositing high quality crystalline Si thin films, except that the In liquid droplets are allowed to move on planar surface, so as to produce well-defined and continuous SiNWs, with a diameter proportional to the size of the catalyst droplets. Meanwhile, the IPSLS process also differs from the metal induced crystallization process, which has been heavily investigated in last decades to produce polycrystalline Si (poly-Si) from a-Si thin film for high performance electronics.[46] The fundamental difference lies that the metal used in MIC process forms atomic scale silicide layer, and the crystallization is rapid and even explosive, typically resulting in circular poly-Si zones, instead of well-defined SiNWs.

4.2. Growth Balance Condition and Geometry Engineering

Compared to the best-known VLS growth,[7b,17] a distinctive feature of the IPSLS growth is that the liquid droplet is now sandwiched by two solid/liquid interfaces (**Figure 7**), one is the front catalyst/a-Si interface, the other is the rear SiNW/catalyst interface. For a typical VLS growth, the liquid catalyst droplet is only propped up by the bottom catalyst/NW interface, as the top and the sidewall interfaces are all soft catalyst/gas boundary, which has little, if any, force to exert on the liquid droplet. Therefore, the droplet can preserve basically a spherical shape during the VLS growth in a gas feeding environment to produce relatively straight NWs, or bending ones due to the formation of twin or structural defects in the NWs or faceting on the sidewalls.[47] By contrast, having two stronger holds provided by the front a-Si/In and the rear In/SiNW solid/liquid interfaces, the liquid droplets can be significantly distorted, being squeezed (or stretched) if the front interface is moving relatively slower (or faster) than the rear one. This distortion can be significant enough to be exploited to engineer the geometry of the as-produced NWs to vary from bending zigzag springs,[48] to straight ones and even island-chains with self-oscillating diameter modulation.[49] This is because the relative moving speeds of the front and the rear interfaces is tunable by controlling the a-Si layer thickness h_{aSi}, or more precisely by adjusting the ratio of $\rho = h_{aSi}/D_c$, where D_c is the diameter of the catalyst droplet. That is, given the size of catalyst droplets, controlled by the initial In layer thickness, the hydrofluoride (HF) power and the temperature of H_2 plasma treatment in the catalyst formation step, the relative moving speeds of the front and the rear interfaces can be adjusted by the a-Si layer thickness, as a convenient parameter to engineer the geometry of the in-plane SiNWs.[50]

This unique capability derives from a stringent growth balance, or mass conservation, condition for the in-plane growth of NWs, which states that the Si atoms absorbed from the front absorption interface should be equal to the Si atoms precipitated out of the droplet to deposit as c-Si NWs at the rear interface. As a detailed discussion and derivation of the balance condition is provided in ref. [50], only a brief summary of this formulation is presented here. At the front absorption

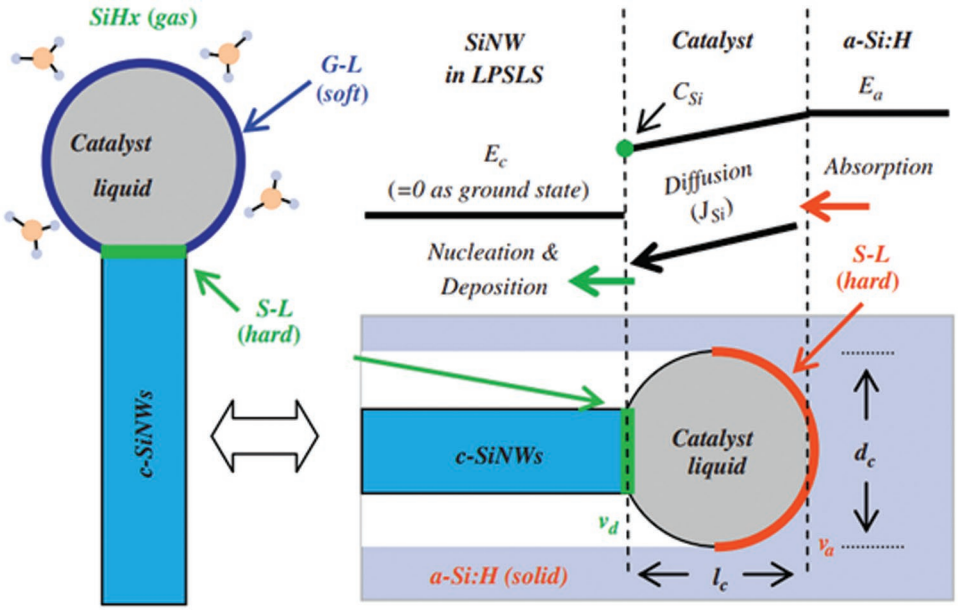


Figure 7. Schematic illustrations of the driving force and the absorption and deposition interfaces in an IPSLS growth with a-Si thin film as precursor, compared to the situation in a VLS growth process. Reproduced with permission.[50] Copyright 2010, Elsevier.

interface, advancing at a speed of v_{abs}, the incoming flux of Si atoms taken from a-Si thin film is written as

$$J_{in} = v_{abs}\, h_{aSi} D_c/\Omega_{Si} \quad (1)$$

where Ω_{Si} is the atomic volume of Si atom. For the rear deposition interface, the outgoing deposition flux of Si atoms to the end of SiNW is

$$J_{out} = v_{dep}\, D_{NW}^2/\Omega_{Si} = v_{dep}\, \alpha^2 D_c^2/\Omega_{Si} \quad (2)$$

with D_{NW} the diameter of the NW, which is roughly proportional to the diameter of the catalyst droplet via $D_{NW} = \alpha D_c$. $\alpha \approx 0.4$ to 0.6 is determined by the surface or interface tension balance at the triple phase line.[50] Equation (2) is established based on the assumption that the as-grown SiNW has a round cross-section. Apparently, the incoming absorption flux J_{in} and the outgoing deposition flux J_{out} scale with the size of catalyst droplet linearly and quadratically, respectively. For a stable in-plane growth, equalizing Equations (1) and (2) yields a balance condition that reads

$$J_{in} - J_{out} \rightarrow v_{abs} h_{aSi}\, D_c = v_{dep}\, D_{NW}^2 \rightarrow \eta = \frac{v_{abs}}{v_{dep}} = \frac{\alpha D_c}{h_{aSi}} = \alpha/\rho \quad (3)$$

Equation (3) tells that the relatively moving speed of the front absorption and the rear deposition interfaces can be readily controlled by a simple ratio of $\rho = h_{aSi}/D_c$, which is a parameter that can be precisely controlled in plasma deposition and catalyst formation.

As an example of this geometry engineering capability for the in-plane growth of NWs, Xue et al. demonstrated in 2016, a self-automated growth of zigzag SiNW springs, by using Sn as catalyst droplets.[48] The growth balance condition was adjusted to a slightly squeezing status, that is the rear interface always tends to move a little bit faster than the front absorption interface with $\eta < 1$. This situation can be obtained by choosing a relative thicker a-Si layer thickness, according to Equation (3), and the gradually squeezed droplet will develop a series of periodic self-turning dynamics (**Figure 8**a), to release the accumulated strain and restore energetically favorable spherical shape. Remarkably, this growth dynamic can be directly observed in situ in an SEM system equipped with a heating stage. This is because the in-plane growth of SiNW requires no gas feeding that will otherwise be a challenge for the electron beam imaging in high vacuum system. Thanks to this unique feature of the IPSLS growth, snapshots of the zigzag growth of SiNW led by brighter Sn catalyst droplets were captured and shown in Figure 8b, where periodic squeezing and turning growth details can be clearly observed in the SEM images. In addition, high resolution TEM analysis of the zigzag SiNW reveals a mono-like crystal structure in the zigzag SiNWs, which are composed of twin-reflected and interlaced crystalline domains, as a consequence of a cyclic crystallographic-index-lowering turning sequence. The twin planes are always found at the turning arms of the zigzag SiNW, corresponding to the change of turning direction at the end of each growth cycle. At the end, the mechanical properties of these self-assembly SiNW springs were testified by using nanoprobes in SEM system, and it is shown that the geometry engineered springs can sustain a tensile loading >12%, significantly larger than the fracture limit of rigid c-Si bulk. Note that, similar zigzag SiNWs are also observed for the In-catalyzed SiNWs,[50] with the basically same formation mechanism, indicating this is indeed a generic strategy for tailoring spring-shaped NWs.

To the opposite situation with $\eta > 1$, that is, the rear deposition interface is lagging behind the front absorption interface, straight SiNWs are usually produced, as a result of the pulling

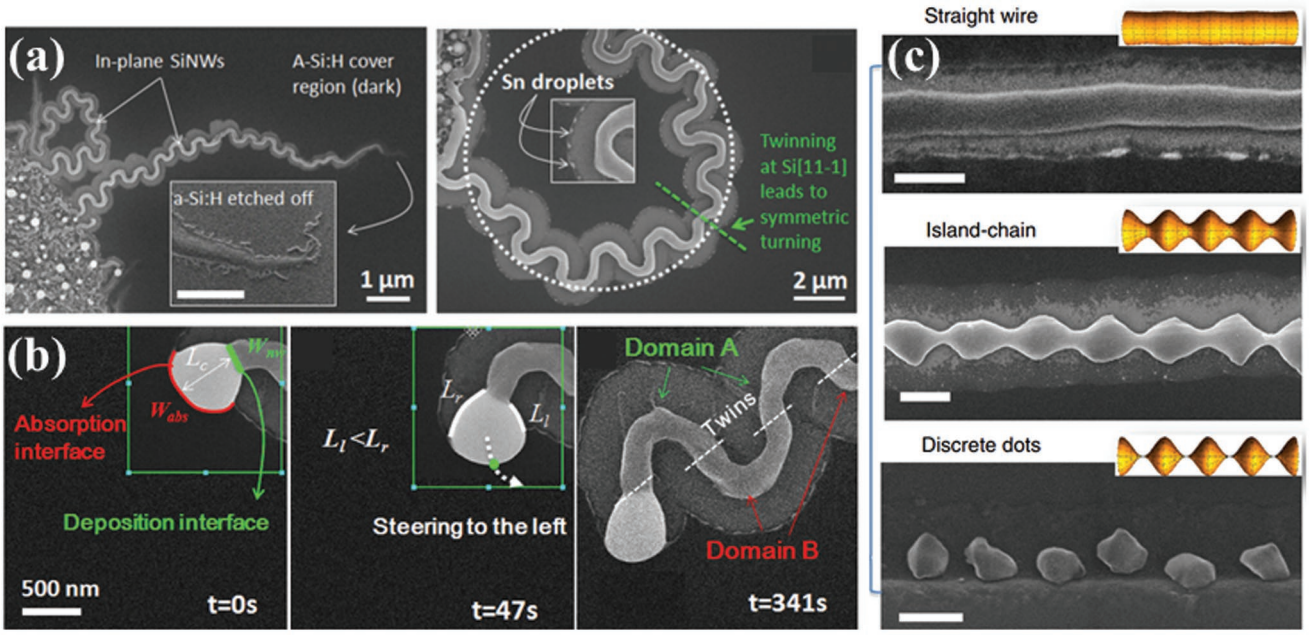


Figure 8. Geometry engineering of the in-plane SiNWs. a,c) The SEM images of zigzag, straight, and island-chain SiNWs grown with In droplets, engineered by significant interface squeezing and stretching forces, respectively. b) The in situ SEM snapshots of the zigzag growth of SiNW springs. The scale bars in the inset of (a) and in (c) are 50 and 200 nm, respectively. a,b) Reproduced with permission.[51] Copyright 2016, Wiley-VCH. c) Reproduced under the terms of the CC-BY Creative Commons Attribution 4.0 International License (http://creativecommons.org/licenses/by/4.0/).[52] Copyright 2016, The Authors, published by Springer Nature.

or stretching effect of the leading droplet on the produced SiNWs.[39,41,43,50] Interestingly, if the interface stretching effect becomes significant enough, a self-modulated and periodic diameter variation dynamic can be stimulated during the in-plane growth of SiNWs, transforming them into continuous or even broken island-chain NWs.[49] This island-chain transformation is quite similar to the breakage of a stream of water into discrete droplets, driven by the minimization of surface energy via a Plateau–Rayleigh (P–R) transformation,[53] despite that the island-chain SiNWs were grown at a temperature below < 350 °C, far below the melting point of c-Si of 1414 °C. Specifically, the island-chain SiNWs were grown via a Sn-catalyzed IPSLS process, where the a-Si layer was set to be relatively thinner than that required for a balanced growth.[49] Under a significant interface stretching on the liquid catalyst droplets, they will first deform into an elongated shape, which then leads to a shrinkage of the cross-section area (as the volume is constant) and a reduced diameter of the as-produced SiNW segment (Figure 8c), if every time the deposition rate at the narrower SiNW segment can pick up the speed to catch up the front absorption interface, a thicker island region will emerge, resulting in a continuous island-chain structure. Otherwise, the SiNW will decay into a chain of broken c-Si grains along the moving courses of Sn catalyst droplets. It is also noteworthy that this diameter-modulated island-chain NWs could serve as ideal fundamental structure to construct single electron devices.[54] Particularly, the nanoscale island-chain structure can be fabricated via a low temperature self-assembly process, and grown into precise locations (via a guided growth technique as will be explained later), which greatly facilitates the electric connection and device fabrications.

4.3. Epitaxial Growth with Thin Film Precursor

Epitaxial growth of high quality thin film or nanostructures upon crystalline substrates is a critical technology to construct a wide range of high performance electronic, optoelectronic, and photonic applications.[55] The underlying substrate lattice provides not only a perfect atomic reference for the subsequent epitaxial growth, but also a desirable guidance for the growth direction of nanostructure.[55,56] Compared to the epitaxial growth of vertical NWs[57] or horizontal NWs[3,5g,24b,25–27,29a,c,d,30,34,36d,f,38a–c,e–g] via VLS mechanism upon various wafer substrates, the IPSLS growth is intrinsically a planar growth, which is confined by the amorphous thin film precursor to form a close contact with the underlying substrate. In this sense, the IPSLS growth is more apt to carry out an epitaxial growth on crystalline substrate.

The first homoepitaxial growth of in-plane SiNWs was indeed demonstrated by Yu et al. in 2014,[56] where In were chosen as catalyst metal and deposited, by using electron beam or thermal evaporation, upon clean Si(100) wafer substrates. In order to guarantee an epitaxial growth, the native oxide on the wafer surface has been removed by HF dipping, prior to being loaded into PECVD system. Then, the samples were treated by H_2 plasma for catalyst droplet formation and coated with a-Si layer as precursor, as described above. Note that, the a-Si deposition was done at a low temperature of 180 °C (nominal temperature), so no SPE growth should be expected. Finally, upon annealing at 350 °C, the In droplets start to move on the surface, but now most of them are observed to follow exactly the crystallographic orientations of the underlying Si wafer substrates along Si⟨100⟩ directions (**Figure 9**a). Interestingly, even

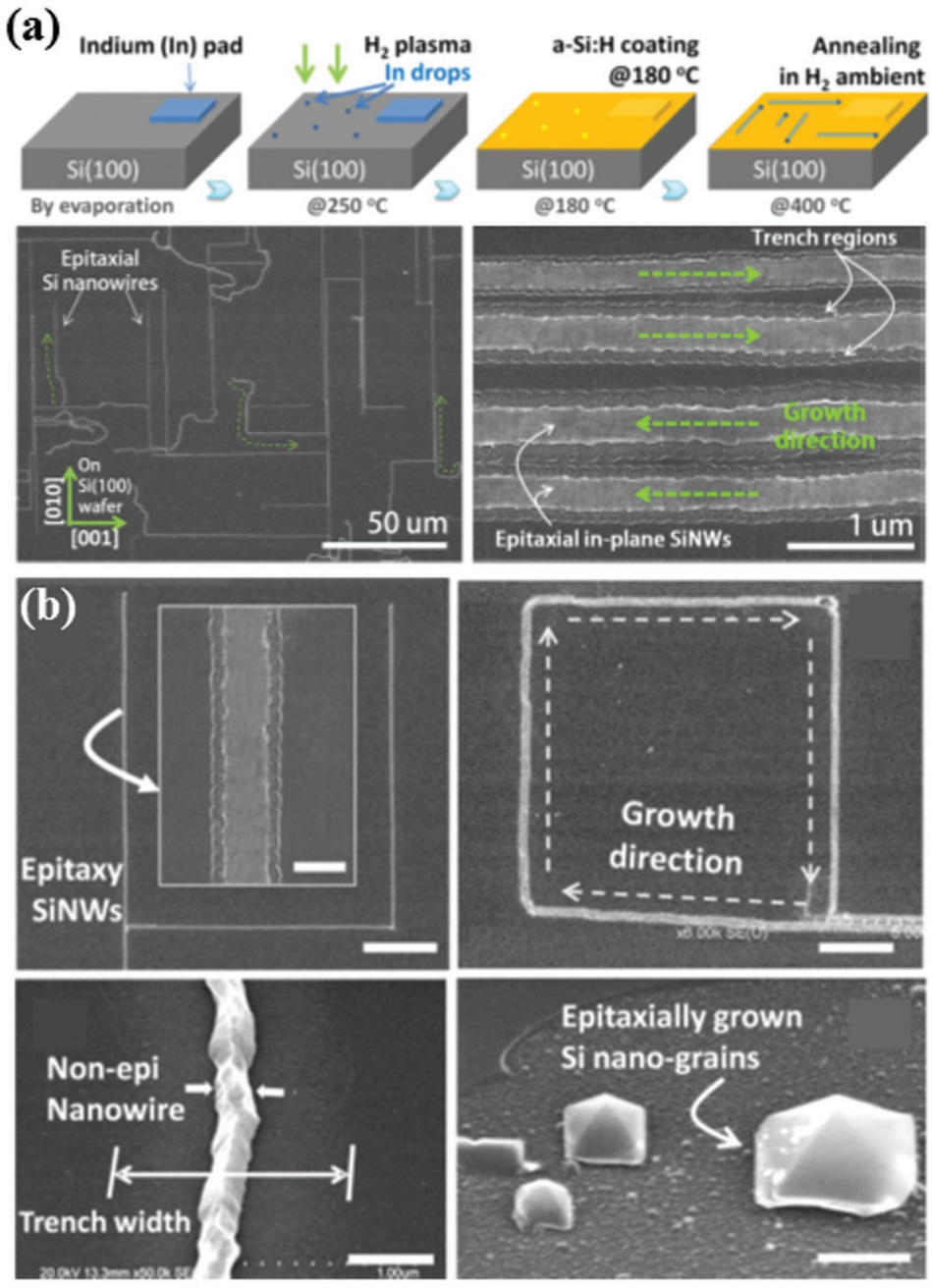


Figure 9. Homoepitaxial growth of SiNWs upon Si wafer substrate. a) depicts the fundamental steps involved in an epitaxial growth of self-aligned SiNWs on Si(100) substrate. b) More SEM details of the epitaxially grown SiNWs. The scale bars in (b) and the inset of (b) are 10 µm, 3 µm, and 300 nm, respectively. a,b) Reproduced with permission.[56] Copyright 2014, American Chemical Society.

the turning angles are always of regular 90 °C, which is exactly the intersection degree among the Si⟨100⟩ directions. Compared to the nonepitaxial SiNWs, which are usually random and irregular in geometry, the epitaxially grown SiNWs are mostly very straight, long, and regular wires, as witnessed in Figure 9b. Moreover, cross-section HR-TEM characterizations confirmed that the epitaxial SiNWs are flatter than the nonepitaxial ones, reflecting a clear tendency for the SiNWs to form a wider homoepitaxial interface with the underlying wafer substrate, where the interface energy is in principle close to zero. In addition, growing p-type SiNWs over n-type Si wafer substrate leads to the formation of a rectifying p–n junction, and the electronic transport property can be easily verified by using the probe of conductive AFM system in a vertical transport configuration.

While the homoepitaxial growth of SiNW upon c-Si wafer has been accomplished via a commensurate epitaxy process, that is no lattice mismatch, seeking incommensurate epitaxy growth of SiNWs directly upon insulating substrate is also highly valuable in view of establishing, for example, high

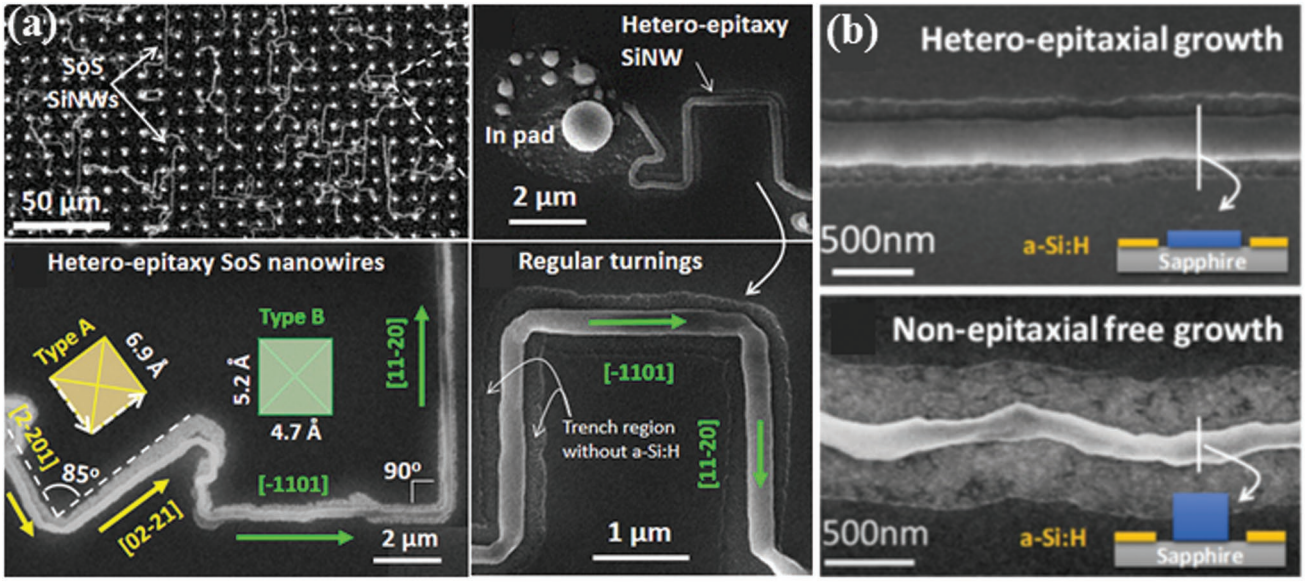


Figure 10. Epitaxial growth of the IPSLS nanowires on sapphire substrate. a) SEM image of the epitaxial IPSLS nanowires growth on sapphire substrate. The nanowire has a 90° turning angle. b) Comparison of the epitaxy nanowire and the nonepitaxy growth nanowire. The epitaxial nanowire is strait and regular while the nonepitaxy nanowire is irregular and smaller. a,b) Reproduced with permission.[55] Copyright 2016, American Chemical Society.

performance silicon-on-sapphire (SoS) electronics. SoS is considered as a special favor of silicon-on-insulator (SOI) technology,[58] where a large portion of parasitic capacitance can be shed off to enable a faster transistor operation, lower power consumption and potentially a higher integration density as the reverse-biased isolation zones required in bulk c-Si CMOS are no longer necessary for integration upon SoS substrate.[59] For this purpose, R-plane sapphire, featuring a similar atomic arrangement to Si(100) surface, are usually used as the substrate for heteroepitaxial growth of c-Si thin film. However, this usually requires a high temperature >900 °C processing, and the large thermal expansion coefficient mismatch between sapphire and c-Si thin film[58] will cause, during the final cooling step, a high density of defects in the as-grown Si thin film. For these reasons, a low temperature heteroepitaxial growth process is highly desirable. Growing in-plane SiNWs directly upon R-plane sapphire (SP) substrate was proposed by Xu et al. in 2016 to address these challenges.[55] It is shown that the in-plane SiNW growth can happen at a low temperature of 350 °C, with self-aligned directions following the SP[–1101] and SP[11–20] crystallographic orientations (**Figure 10**). Also, the nanoscale SiNW channels are formed in a single-run In droplet travel, exempting the need for later lithography for channel definition. More importantly, the SiNWs can also better dissipate the remnant lattice mismatch strain accumulated at the SiNW/SP interface, compared to a complete coverage of epitaxial thin film over the SP substrate surface. Based on the SiNW-on-insulator configuration, the authors also succeeded in demonstrating a fin-gate FET device, with reasonable I_{on}/I_{off} ratio >10^4 and mobility of 50 $cm^2\ V^{-1}\ s^{-1}$, through such a low temperature fabrication process.

It is also important to note that both the homoepitaxial and heteroepitaxial in-plane growths are subject to the constraint of growth balance criterion, as stated in Equation (3). For the in-plane growth with condition largely deviated from the balance parameters, a continuous epitaxial growth is not guaranteed. Specifically, if the a-Si layer is too thin, the SiNWs will decay into a chain of discrete islands, though most of them appeared as separate pyramids with clear facets,[56] implicating the existence of a coherent epitaxial interface at the bottom connected to the underlying wafer or R-plane sapphire substrates. On the other hand, the authors also point out that the epitaxial growth relies on the direct formation of discrete seeds directly on the bottom epitaxial interface, which inherit the orientation information from the crystalline substrate and are later merged into a continuous wire by the advancing SiNW/catalyst interface. This is indeed a critical requirement to guarantee a unidirectional growth of the NWs. For the growth with a too thick a-Si layer coating, the formation of crystalline seeds, directly contacting to the bottom substrate interface becomes more difficult, and as a consequence, an epitaxial growth is difficult to happen and most of the in-plane SiNWs will grow in a free and nonepitaxial manner.

4.4. Guided Growth of In-Plane NWs by Step Edges

As a prerequisite for scalable application of NWs-based electronics, the self-assembly NWs have to be positioned or grown into precise locations for a reliable device integration. Importantly, this has to be accomplished via an economically feasible and affordable approach, which is also supposed to be compatible to the standard planar Si technology and processing. Epitaxial growths of NWs via VLS[38f] and IPSLS[55,56] mechanisms have proven efficient and useful in producing self-aligned NW channels for FET device prototyping, which represent a critical step forward toward integrating the self-assembly building blocks for practical applications. In the next step, the NWs are

supposed to grow directly into precise locations in planar electronic architecture, so as to enable a deterministic and reliable integration of NWs, importantly via a scalable and affordable strategy. To this end, an in-plane growth of NW confined to 2D planar surface by adopting thin film precursor is advantageous, as now a precise guided growth requires only a 2D–1D = 1D confinement that can be defined on surface, reduced from the 2D confinements provided by nanopores or nanochannels in directing 3D VLS growth of NWs.

Fortunately, for the in-plane NWs grown via IPSLS mode, this 1D confinement can be provided by simple step edges, as depicted schematically in **Figure 11**a, which can be easily patterned upon planar substrate by using low resolution lithography and etching process, or even by sliding sandpaper over the substrates. The first report of a guided growth phenomenon of in-plane SiNWs was published in 2009,[61] where the edges of ITO pads predefined on wafer substrates were found to be able to attract the movement of In droplets, and thus producing self-aligned SiNWs along the step edge lines (Figure 11b). This ability derives from the fact that the a-Si coated on the vertical or oblique sidewalls of step edges forms an extra absorption interface (Figure 11c) with the liquid catalyst droplets, which can thus attract and guide the droplets to move along the edges. The stability of this guided growth strategy is indeed quite remarkable, as it has been observed that the in-plane SiNWs can be guided to grow over bending corner edges with largely varied local curvatures. And the guided growth control can be applied to SiNWs with different diameter ranging from tens to hundreds of nanometers, given a proper step height and growth balance condition.

In addition, according to Jeon et al.,[101] a precise guided growth can also be accomplished via an a-Si channel guiding approach, where narrow a-Si stripes were predefined by etching and used to enforce the growth of in-plane SiNW into and along the channels covered by a-Si stripes. Note that, in order to impose a stringent guidance for the catalyst movement, the width of the a-Si channels should be comparable to or thinner than the diameter of the leading catalyst droplet, which is indeed a challenge for conventional lithography technology (usually with spatial resolution > 1 µm). However, the a-Si channel guiding technology has a unique capability, that is it can control the diameter of the SiNWs by adjusting the a-Si channel widths,[61] which could be useful for seeking further geometry control over the SiNW channels. Furthermore,

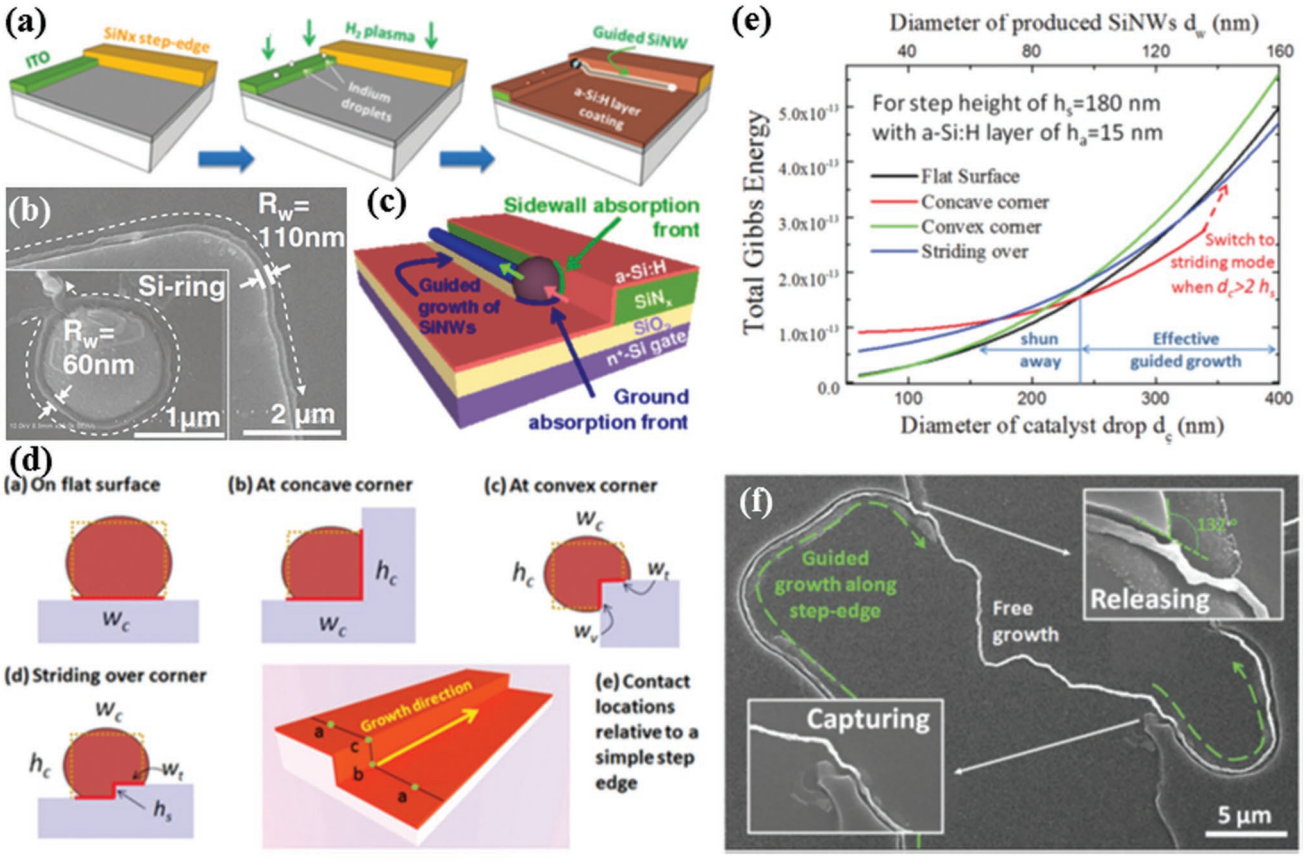


Figure 11. Guided growth of in-plane SiNWs along step edge lines. a) Schematics of the fabrication procedure of guiding edge for directing an in-plane growth of SiNWs. b) SEM images of the in-plane SiNWs guided over a corner and the periphery of a sphere. c) Schematically the absorption fronts of an In droplet contacted to and thus attracted by a guiding edge. d) The four possible contact situations between the droplet and a step edge, while their corresponding total Gibbs energies are calculated and plotted in e) against different initial diameters of the leading catalyst. f) An SEM image of an ultralong SiNW that was guided, released, and captured by step edges with varied local curvatures. a–f) Reproduced with permission.[60] Copyright 2015, Royal Society of Chemistry.

as an extension of the a-Si channel guiding technology, the in-plane SiNWs can also be guided along the edges of a-Si coated regions. But this has to be carried out with a growth balance condition that deviates toward $\eta < 1$ (with thicker a-Si according to Equation (3), where the droplets will tend to grow along the a-Si edges as a mechanism to release the accumulated strains in the catalyst droplets due to interface squeezing.

Though the guided growth of in-plane NWs has been successfully applied to deploy an orderly array of SiNWs for FET applications in 2011,[62] a comprehensive understanding of the key control parameters in achieving a stable guided growth was not established until 2015.[60] In this work, the authors focused on the growth balance conditions encountered by a running catalyst droplet that contacts to a simple step edge, with four distinct principal situations of flat, concave corner, convex corner, and striding over configuration, as illustrated in Figure 11d. In contrast to the relatively simple planar growth scenario, the addition of an extra absorption front on the edge sidewall modifies greatly the balance condition, described by Equation (3), for planar growth. Here, the Gibbs energy of a catalyst droplet, contacted to a step corner, is composed of both surface and interfacial energies. The catalyst droplet is allowed to deform to minimize the Gibbs energy, and switch among the different contact scenarios. Though the details of the analytic model are beyond the scope of this Review, the interested readers can refer to ref. [60] for a comprehensive discussion. In short, the major conclusions can be summarized, as shown in Figure 11e, where the total Gibbs energies, seen by the leading catalyst droplets (after structural adjustment to minimize the Gibbs energy), are plotted against the diameters of the droplets. It is interesting to see that, a guided growth along the step edge is not always energetically favorable, particularly for the tiny In droplets, which will prefer instead growing into flat surface area (shun away from the guiding edges) or adopt a convex-corner contact. For the larger droplets, guided growth with concave contact becomes more energetically preferable, as they allow the catalyst droplet to arrive at a lower Gibbs energy, compared to other scenarios. Of course, for too large droplets, with diameter much higher than the height of the guiding step, a striding over contact is indeed the most favorable situation. Indeed, these predictions are mostly verified in experimental observations. This model thus provides critical fundamental understanding, as well as a practical guide, for achieving a reliable guided growth of in-plane SiNWs. It was also shown that, the guided SiNWs can be released at pointy or sharp turning of the step edges, for example, a guided SiNW was observed to detach from the guiding edge at a sharp turning (≈130°) place, see the SEM image in Figure 11f, and got captured again by another guiding edge after a free travel in planar surface region.

4.5. Catalyst Doping Control in Planar NWs

Doping has been a critical aspect for NW-based electronic and optoelectronic applications. For metal droplet catalyzed VLS or IPSLS growth, the incorporation of catalyst atoms into the as-grown NWs is known to result in effective p-type[49,62] or n-type[63] doping, which are promising alternative strategy to the conventional doping controls of VLS SiNWs by using gas dopants.[64] For example, by using bismuth (Bi) or BiSn alloy as catalyst, n-type vertical SiNWs have been grown without the use of any toxic phosphine gas dopants, providing a beneficial basis for the construction of radial junction photovoltaics.[42g,63b] For the in-plane growth of SiNWs, the In catalyst atoms are also observed to be incorporated into the SiNWs, serving as p-type dopants to give off hole carriers, which has been verified in the transfer properties of SiNW FET devices.[62] For the incorporation of aluminum atoms into Si NWs, a colossal injection model was proposed by Moutanabbir et al. in 2013,[63a] where the key kinetic steps in the incorporation of catalyst atoms into c-Si lattice were identified and discussed. In fact, the incorporation of catalyst atoms into the as-grown NWs is almost an inevitable phenomenon, as well as a unique aspect, for all the metal-droplet-catalyzed self-assembly growth of NWs. Taking it as a disadvantage or an opportunity depends on to what extend we can understand, control, and make a better use of these incorporated catalyst atoms for desired functionalities.

In order to understand the distribution of the incorporated catalyst atoms, atomic probe tomography (APT) provides the most straightforward tool to reconstruct the atomic and compositional distribution in a chosen volume of SiNWs. Several reviews are available for the readers who hope to obtain detailed information of the APT technology.[65] For instance, the distribution of In atoms in a selected volume of $40 \times 40 \times 875$ nm^3 in In-catalyzed SiNWs was obtained by using APT analysis (**Figure 12**a,b), which reveals that the In atoms, with a concentration as high as $\approx 10^{19}$ cm^{-3}, can be clearly distinguished among the Si lattice. However, the In atoms are known to induce a defect level lying 160 meV above the valence band top of c-Si, which is much deeper than the activation energy of 45 meV for boron atoms. This leads to a rather low ionization rate of the incorporated In atoms even in substitutional positions, which is estimated to be equivalent to a boron doping of only $\approx 40 \times 10^{17}$ cm^{-3},[66] a medium level that will not cause too much doping for the SiNWs to serve as semiconducting channels. Indeed, prototype FET device fabricated on the In-catalyzed SiNW demonstrated a p-type channel behavior with hole mobility of around 200 cm^2 V^{-1} s^{-1},[67] indicating that the In catalyst incorporation in SiNWs is indeed helpful to achieve active and efficient p-type doping and, at least, not detrimental. High performance SiNW-based thin film transistors (TFTs) devices also confirm this point, which will be elaborated with more details in the following chapters.

Then, the catalyst atom incorporation dynamic into the SiNWs grown via IPSLS mechanism was investigated systematically by Chen et al. in 2014,[49] by using APT and HR-TEM technologies, in close comparison to the SiNWs grown via VLS mode by using In and Sn catalysts (Figure 12b), rather high concentration and uniform distributions of In and Sn atoms have been witnessed in the IPSLS-grown SiNWs, which can be measured to be 1.5×10^{19} and 1.3×10^{19} cm^{-3} for the In and Sn atoms, respectively. In comparison, the incorporation concentrations of the In and Sn atoms in the VLS-grown SiNWs, even at a high growth temperature of 400 °C, are only 1.5×10^{18}cm^{-3} and 6.8×10^{18} cm^{-3} for the In and Sn atoms, respectively, roughly an order's of magnitude lower than that in IPSLS SiNWs. Actually, even the lower In atom concentration in the VLS-grown SiNWs is much higher than the

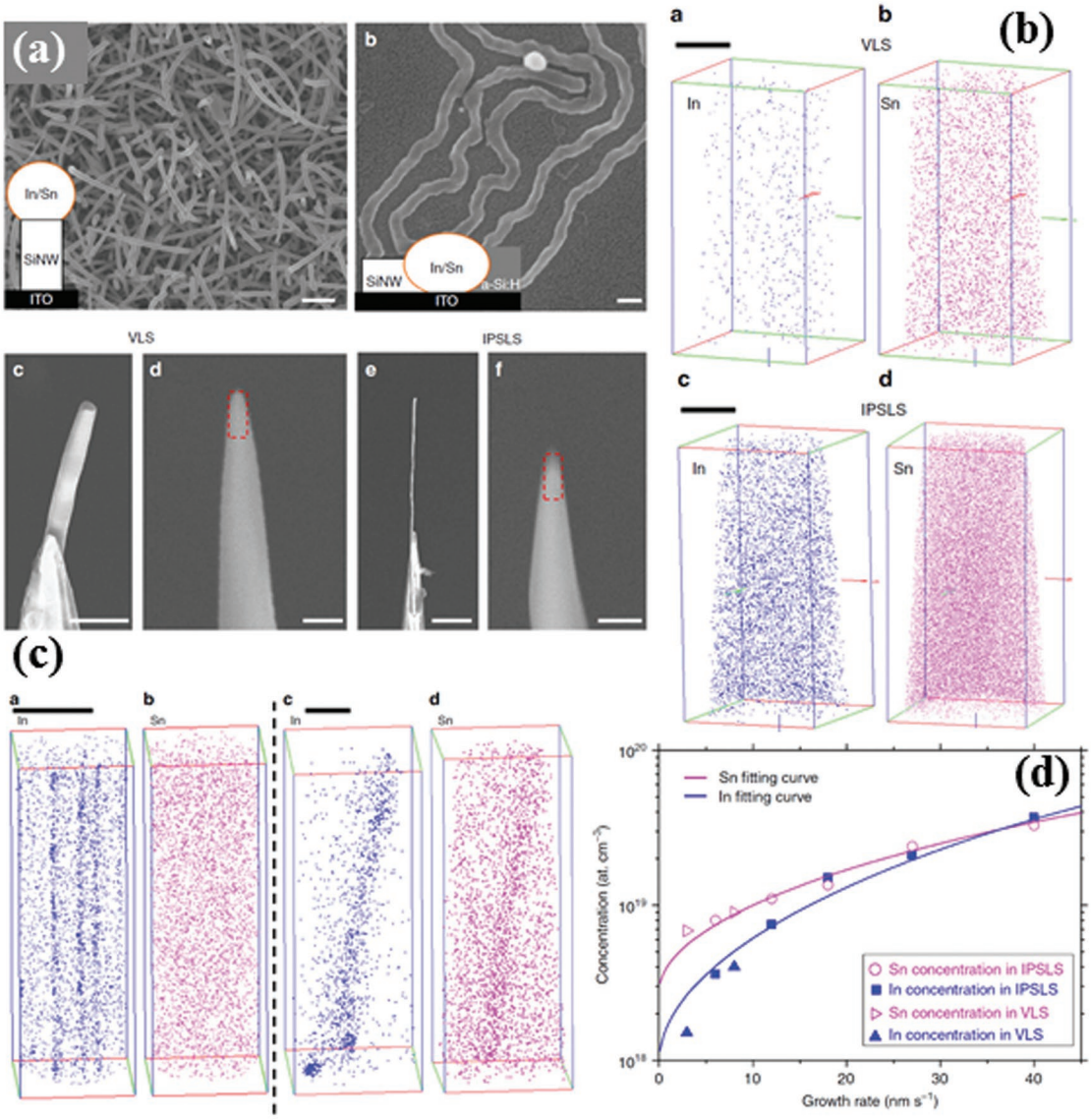


Figure 12. Doping control in SiNWs via catalyst atom injection. a) SEM images of the SiNWs grown via VLS or IPSLS mechanism for atomic probe tomography (APT) characterizations. b,c) Comparison of the reconstructed 3D distribution of the incorporated In or Sn atoms in the as-grown SiNWs via VLS and IPSLS processes, without or with the presence of twin planes, respectively. d) The increased catalyst atom concentration of In and Sn atoms in the SiNWs, as functions of growth rates. The scale bars in (a) are 500 nm, 500 nm, 500 nm, 100 nm, 2 µm, and 100 nm, respectively. The scale bars in (b) and (c) are 20 nm. a–d) Reproduced with permission.[49] Copyright 2014, Springer Nature.

equilibrium concentration with c-Si, which is in the order of 10^{17} cm^{-3} for In atoms in c-Si lattice, while for Sn atoms the equilibrium value is much higher to be 10^{19} cm^{-3}.[68] In fact, the only difference for the IPSLS-grown planar SiNWs and the VLS-grown vertical SiNWs is the growth rate, and the former is typically in the range of 10 to 10^2 nm s^{-1},[49] while for the VLS growth the rate is usually <1 nm s^{-1}. The fundamental reason behind is the different feeding precursors, where the a-Si thin film feeding is indeed much denser compared to that could be arrived by using a gas precursor feeding (Figure 12c), the incorporated catalyst atom concentrations are not simple constants for both the In and Sn mediated growth of SiNWs via IPSLS or VLS modes. Rather, they all increase monotonically with the increase of growth rate, and this trend is more prominent for the incorporation of In atoms (Figure 12d), which is observed to increase by more than one order of magnitude when the grate rate is boosted from 6 to 40 nm s^{-1}. For the very high concentration of In atom incorporation, precipitation of In to the nearby twin planes was detected by both APT and high-resolution STEM.

This finding indicates a unique nonequilibrium catalyst atom injection mechanism that can be adopted to achieve a tunable catalyst atom incorporation over a wide range of concentration. While more details of the model are already discussed in ref. [49], the key mechanism can be assigned to the rapid atomic piling kinetics happened at the fast growing SiNW/catalyst interface.

In brief, when the growth rate is increased, the chance for the attached catalyst atoms to be imprisoned/or covered by the following Si atom deposition increases proportionally, or in other words, the relaxation time for the catalyst atoms to retreat away from the newly forming SiNW top interface is reduced for a faster growth of SiNW. This will lead to the incorporation of more catalyst In or Sn atoms into the SiNWs. Note that, the very fast growth rate, enabled by the IPSLS growth mechanism, is the key for this nonequilibrium catalyst atom injection effect to manifest and become potentially useful for controlling the doping effect in the in-plane SiNWs.

4.6. Compositional Control of Ge/Si Island-Chain NWs

In addition to the geometry or diameter engineering of NWs, compositional modulation is another key dimension of control that can help modify the band profile in the 1D channels to enable a series of artificially designed electronic, photonic, and phononic functionalities.[69] A rather straightforward logic can be followed in the metal catalyst assisted growth of NWs, that is, the composition of the NW segment, formed at specific moment, is all determined by the feeding precursor, or more precisely by the ingredient atoms dissolved in the leading catalyst droplets. Therefore, it is easy to apply this logic in a VLS growth procedure, where alternating the gas feeding of GeH_4 and SiH_4 will yield hetero-NWs with alternating Ge and Si segments, and this has indeed been demonstrated successfully by different groups in the last decades.[70] However, this approach also demands a stringent gas alternation control during the VLS growth of NWs, and an abrupt compositional switching from one ingredient to another in the NW is difficult to achieve due to a reservoir effect in the catalyst droplets.[71] For example, hetero-Ge/Si NWs or Ge/Si superlattice NWs, grown via VLS approach with alternated Ge and Si gas supplies, can only achieve a Ge content modulation in the range of 0–30%.[70a] In order to improve the compositional contrast, long intervals and purging steps have to be inserted between the Ge or Si growth periods,[70a,72] or by using alloy catalyst droplets[73] or lowering the growth temperature,[74] to reduce the remnant ingredient concentration in the catalyst droplet. So far, abrupt Ge/Si transition of several atomic layer thick has been accomplished via a vapor–solid–solid mode, but only at an extremely slow growth rate <0.4 nm min^{-1}.[75]

Another strategy to accomplish an efficient compositional modulation in the NWs is to explore the growth dynamics of the leading catalyst droplets. Though the strong interface stretching or squeezing forces during an IPSLS growth has been utilized to produce diameter modulated island-chain SiNWs, the potential of this in-plane growth for compositional modulation has not been investigated until recent years. In 2018, Zhao et al. proposed an a-Si/a-Ge bilayer feeding growth of in-plane NWs to accomplish a self-modulated hetero-Ge/Si superlattice-like NWs.6[9] Specifically, a thin film of a-Ge layer was first deposited and then buried by an a-Si capping layer, as diagramed schematically in **Figure 13**a. When the In catalyst droplets are active to grow in an annealing at 350 °C, the liquid droplets developed a unique rolling and bouncing nanoscale hydrodynamics, which helps to modulate the effective absorption depth into the underlying bilayer automatically and periodically.

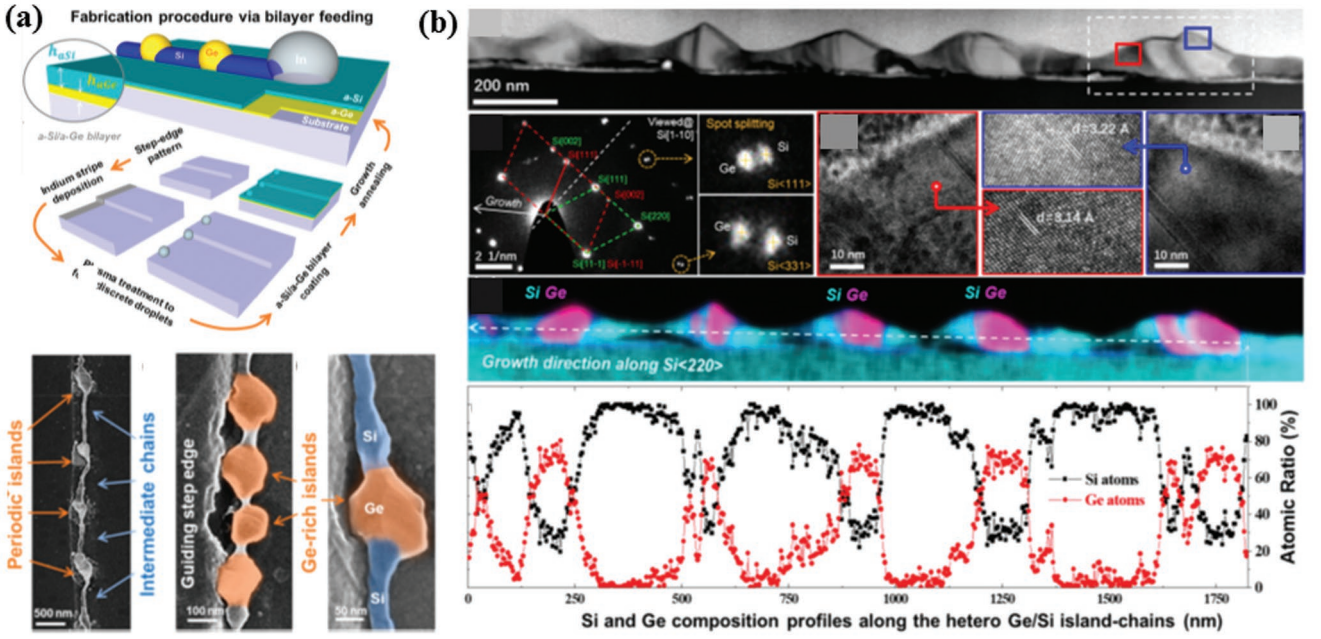


Figure 13. Compositional engineering and the formation of Ge/Si island-chain superlattice hetero-NWs. a) Schematic of the fabrication procedure of Ge/Si island-chain hetero-NWs by adopting a stacked a-Si/a-Ge bilayer precursor, with typical SEM images shown in the lower panels. b) HR-TEM characterization and EDS mapping of a segment of Ge/Si NW, with the extracted Si and Ge content variation plotted in the lower panel. The scale bars in (a) and (b) are 500 nm, 100 nm, 50 nm, 200 nm, 1 nm, 10 nm, and 10 nm, respectively. a,b) Reproduced with permission.[69] Copyright 2018, American Chemical Society.

As a consequence, the as growth NWs are composed of a chain of Ge-rich (>75%) wider island nodes, connected by narrower pure SiNW segments. The c-Ge segments are identified as the brighter and wider islands in the dark-field TEM imaging due to their higher density compared to that of the c-Si phase as seen in Figure 13b. The Ge/Si transition interface is rather sharp, with a transition region thickness of only ≈4.1 nm, considering that this self-modulation growth was accomplished without any external control and intervention. The compositional modulation was further confirmed by surface potential scanning mapping, where due to the type-II band alignment between Ge and Si regions, electrons, and holes are separated automatically and accumulated into the Si chain and Ge-rich island regions, leading to detectable potential variation on the surface of the Ge/Si NWs.

For the formation mechanism, the authors proposed a descriptive mode, where the rolling forward behavior of the droplets and its impact on the convective mass transport and absorption inside the catalyst droplets are highlighted. It is reasonable that a liquid droplet moving on substrate surface will be forced into a rolling dynamics, as otherwise a simple sliding on solid ground will be far more energetically costly and inefficient. This thus causes a convective mass transport inside the droplet that will encourage the absorption from the front interface, while suppressing the absorption or consumption on the bottom interface. If the droplet can proceed fast enough, the rolling and thus the convective transport will become significant, to an extent that the droplet will not consume all the a-Si layers during its lateral travel. The author also provided experimental proof for this unique floating in-plane growth, as for some catalyst droplets the monolayer of a-Si will not always be completely absorbed and the remnant a-Si layer can be clearly discerned in the SEM image. Then, after a period of floating growth of the catalyst droplet over the top a-Si layer, the speed will gradually slow down and this will lead to an eating through of the top a-Si layer, touching the buried a-Ge layer. Interestingly, Ge atoms have a much higher equilibrium concentration in In than that of Si atoms, and thus the Ge layer can be quickly absorbed by the catalyst droplet to precipitate a larger Ge-rich island node. Of course, the absorption of the underlying a-Ge layer is also limited by the capping a-Si layer, and to some extent the In droplets will be pushed by the newly formed Ge-rich island to pick up the speed and roll forward again. This scenario has been supported by a straightforward in situ SEM observation of the Ge/Si hetero-NW growth, where the positions of the front and the rear interfaces are followed in real time, so as to extract the change of growth rates for these interfaces and the droplet as a whole. Periodically changes of the moving rates (slowing down and accelerating) were indeed observed and coupled to the formation of apparent Ge-rich island nodes. While a more comprehensive model has to be established in order address all the dynamics details of this self-modulated Ge/Si hetero-NW growth, this simple bilayer feeding approach has a great potential to be used as a new dimension of control for achieving simultaneous compositional and geometrical engineering in the in-plane Ge/Si NWs. Meanwhile, the potential of this approach to tailor the composition in NWs of other material systems remains still to be explored.

5. Device Applications Built on Planar Nanowires

Planar assembly of synthetic NWs or direct growth of horizontal NWs into orderly arrays or precise locations, with known channel numbers and orientations, provide the solid basis for a reliable construction of scalable electronic logic gates, optoelectronic, photodetector, and sensor applications in the mature planar integration architecture. In the following sections, the prototype devices based on the NW building blocks arranged, connected, and deployed on planar surface will be reviewed.

5.1. Sensors, Photodetectors, and Photovoltaics

Si or other semiconducting NWs, which are grown via VLS procedure, transferred, and connected upon oxide coated wafer substrates, have been widely used to prototype various field effect biosensors, with different surface functionalization techniques.[10a,b,i,k–o,76] The major advantage of self-assembled NWs for biosensing applications is that the surface grafting of targeted bio or gas molecules, with characteristic charge status, can result in an effective gating effect on the quasi-1D NW channels, which can be rapidly detected as convenient electric signals with a rather high sensitivity. Meanwhile, a low temperature metal droplet assisted self-assembly fabrication of the NWs exempts the use of elaborated and inefficient EBL technology to pattern nanoscale channels, and the as-grown NWs have a potential to be transferred and integrated directly upon soft substrates for flexible sensors and other electronic applications.[5d–f,77] Actually, there are already several excellent reviews on the bio- and gas sensing applications based on the self-assembled NWs.[5b,8c,78] So, this Review will focus solely on the sensors, detectors, and logics built upon NWs grown laterally on planar substrates.

The advantage of a self-oriented horizontal growth of NWs, as described in previous section, is that their starting places and the orientations can be known beforehand, which allows a precise electrode connection to the NW channels for photodetector device fabrication, as shown in **Figure 14**a. For example, this capability has been extended to grow parallel horizontal zinc selenide (ZnSe) NWs upon flat or faceted sapphire substrates for blue–UV light detection, exploring the relatively wider bandgap of ZnSe of 2.7 eV.[27] It was shown that the high crystallinity of the ZnSe NWs can help to achieve a rather low dark current and rise and fall response time scales of 74 ms and 0.2 s, respectively, which are the fastest among the ZnSe-NW-based photodetectors. Then, horizontal NWs of direct-bandgap semiconductor were also fabricated, which enables the demonstration of visible-range photodetectors with rather fast photoresponses.[5g,h,15d,24b,25,27,28b,36a,79] The rise/fall response time scales are both around 2 µs, with responsivity up to 347 A W^{-1} and photoconductive gain of 911, both of them are essential capabilities for optoelectronic applications. Then, trigate transistors and photodetectors were fabricated upon horizontally grown CdS NWs at wafer scale, where a rather high on/off current ratio > 10^8 has been obtained, with an even shorter response time in the order of 10^2 ns (Figure 14b),[5g] opening exciting opportunities for high performance NW-based

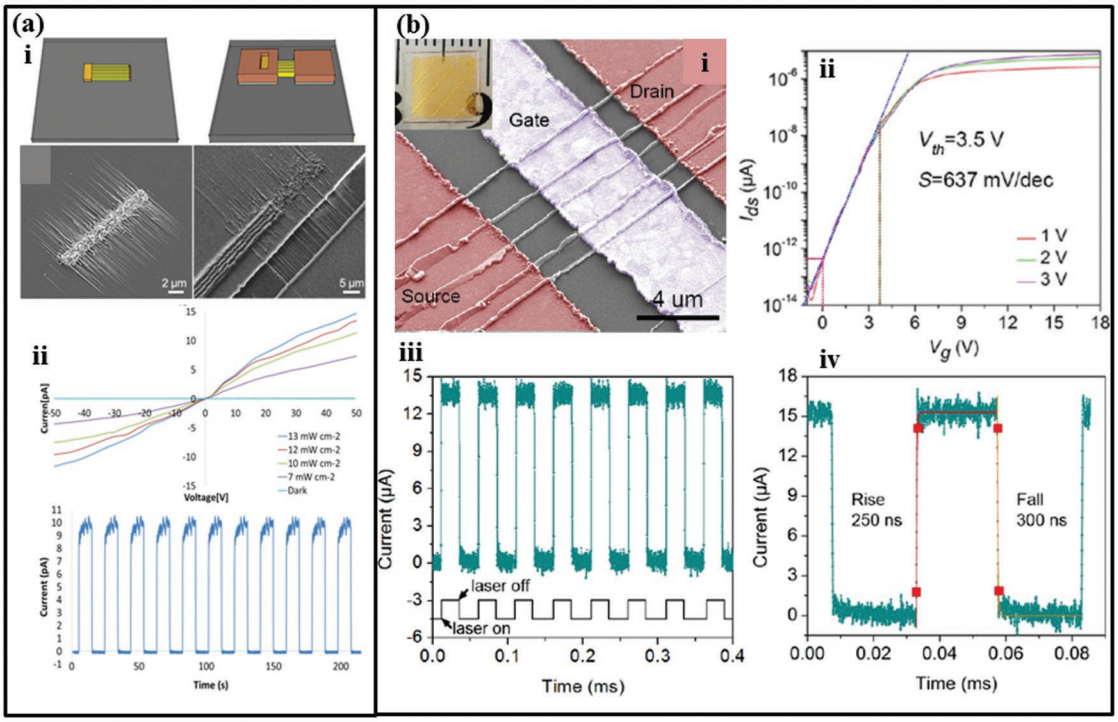


Figure 14. Photodetectors built upon self-aligned horizontal ZnSe and CdS NWs. a) A schematic illustration of the epitaxial in-plane growth of ZnSe NWs on sapphire substrate, as well as the configuration of the photodetector device. The *IV* characteristics measured under different 405 nm illumination intensities and dark conditions are shown below, together with the dynamic response behavior under modulated illumination. Reproduced with permission.[27] Copyright 2015, Wiley-VCH. b) SEM of the trigate FET device fabricated upon CdS nanowalls or NWs, as well as the transfer property and the photocurrent response under a modulated 405 nm laser illumination. a,b) Reproduced with permission.[5g] Copyright 2017, American Chemical Society.

electronics and photodetectors. In **Table 1**, the photodetectors fabricated upon planar NW structures in the literature are summarized and compared in terms of their key device performance.

On the other hand, the planar NWs can also be exploited to construct nanoscale solar cells to drive nearby nanoelectronics. This concept was first proposed and demonstrated by Tian et al. in 2007, where p-type SiNWs grown via VLS process were coated with polycrystalline (poly)-Si intrinsic absorber and n-type doped layers to form coaxial core–shell p–i–n junctions, and then transferred to planar substrate surface for electric connection and device characterization. Though these coaxial solar cells demonstrate only a moderate power conversion efficiency (up to 3.4%), they are sufficient to drive ultralow power nanoelectronic sensors and logic gates.[15b] The photovoltaic cells can also be fabricated directly upon crystalline SiNWs, by forming rectifying metal–semiconductor Schottky contact,[11b,87] providing a convenient test bed to measure the photocarrier lifetime and recombination velocity of the NW absorber. In view of scalable device application or precise alignment to the nearby nanoelectronics, it is also important to guide and control the alignment of the bottom-up NW photovoltaic units, as accomplished by Oksenberg et al. in 2017.[5h] The core–shell ZnSe@ZnTe NW solar cells were grown heteroepitaxially upon C(0001) sapphire substrate, with controlled crystal phase and crystallographic orientations, which demonstrated rectifying behavior and photovoltaic response under 405 nm illumination.

5.2. Logic Gates and Thin Film Transistors

The first high level NW-based nanoprocessor was constructed by transferring and positioning 496 Ge/Si core–shell NWs[9a] upon planar substrate surface, which were patterned and connected by using standard EBL, evaporation, and etching procedures.[5f] the Ge/Si NW channels were coated with a composite $Al_2O_3/ZrO_2/Al_2O_3$ layer to achieve programmable and nonvolatile memory effect (see **Figure 15**a–c). In a two-layered logic tile configuration, the nanoprocessor can operate as a full adder, full subtractor, multiplexer, demultiplexer, and even clocked D-latch functions (Figure 15d–i), representing a significant advance in the complexity and functionality of nanoelectronics for computing, memory, and addressing functionalities.

Then, the ability to grow self-aligned ZnO NWs has been implemented to produce horizontal NW channels upon R-plane sapphire substrates by Schvartzman et al.[37] In order to define the starting places of the NWs grown via VLS mode, the Au catalyst pads were first prepatterned by using EBL technology on the substrate. The subsequent oriented growth of ZnO NWs is directed by the underlying crystalline sapphire lattice to develop into two opposite directions, making them easy to be located and electrically connected for device fabrication. The as-produced NWs were typically 6 μm long with a standard deviation of 12%, and more than 99% of the NWs were found to align within 0.1° angle deviation, see **Figure 16**. An overall yield of 85% for the final FET devices is also impressive for the bottom-up self-assembly growth fabrication. In addition to

Table 1. Comparison of the photodetectors built upon planar NW structure in the literature.

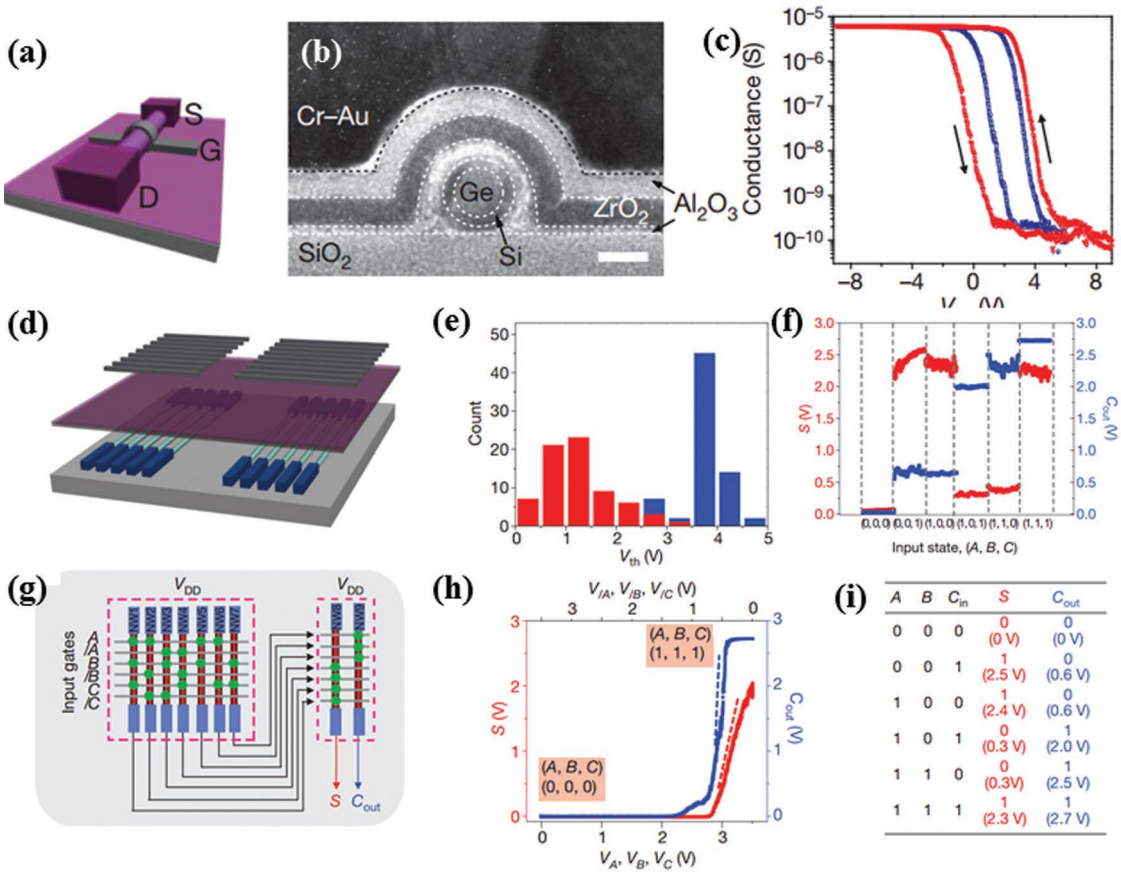
Type of NWs	Fabrication method	Responsivity [A W^{-1}]	I_{On}/I_{Off} ratio	Response time (t_r/t_d)	Ref.
CdS nanowalls	CVD	84@405 nm	180	260/310 ns	[5g]
p-Type ZnTe NWs	CVD	NA@532 nm	120	<5/5 ms	[24b]
CdSe NWs	CVD	14–347@473 nm	1.6×10^3–5.6×10^5	2.3/2.5 µs	[25]
CdS–CdSe core–shell NWs	PVD	1.2×10^3@405 nm	≈2 orders	<250/<330 ns	[80]
GaN MW arrays	Catalyst-free MOCVD	1.17×10^5@325 nm	≈ 1 order	36.3/75.2 ms	[36a]
a-IGZO/(SnO_2 NWs)	CVD	329@350 nm	≈4 orders	NA	[79f]
ZnO–CdO nanofiber	Electrospun	1@325 nm	≈4 to 5 orders	3s	[79d]
ZnO NWs	Electrospun	7.5×10^6@365 nm	≈5 orders	0.56/0.32 s	[81]
Si NW network	EBL	25@532.5 nm	≈1 order	0.58 ms	[82]
CsPbBr3 perovskite NWs	CVD	3.8@438 nm	1.2×10^4	2 ms	[83]
$CsPbBr_3$ nanowire network	CVD	NA@421 nm	10^3	100 ms	[31a]
$MAPbI_3$ network	Solution synthesis	0.1@650 nm	340	0.3 ms	[84]
$CsPbI_3$ single NW	CVD	4489@532 nm	$>10^4$	<50/<50 ms	[85]
$MAPbI_3$·DMF NW array	Solution synthesis	410@532 nm	≈1 order	0.22/0.79 ms	[86]

demonstrating working ZnO NW FETs with mobility of around 60 cm^2 V^{-1} s^{-1}, the authors managed to fabricate a complex multidevice circuit based on the guided growth, a tree address decoder made of 14 interconnected NW FETs. This is indeed the first example of massively parallel self-integration of discrete NWs into complex electronic circuitry.

Though self-assembly growth of planar NWs, via metal-droplet-catalyzed VLS or IPSLS mechanism, have accomplished a series of remarkable technical breakthroughs in reliable batch-manufacturing, transferring, precise location, and orientation controls, as summarized above, they are still not supposed to replace or even challenge, in near future, the standard top-down processing technology, which includes high resolution lithography, etching, and so on, for ultralarge scale integration of microelectronic devices. Nevertheless, there are still plenty of emerging application and market places to conquer for the planar NW technology. A good example is the so-called macro or large area electronics, which refer to the electronic logics that need to be fabricated over very large glass or particular substrates, of several meters instead of typical wafer-sized, which is usually the case for the flat-panel display industry. In order to fabricate high performance control logics over these large area substrates, semiconducting thin film materials have to be deposited uniformly over large surface and typically only a low temperature <600 °C process is allowed, constraint by the highest temperature endurable for the glass pieces as substrates. Because of this, the field effect transistors in large area electronics are called thin film transistors (TFTs), which are also in pursuit of high carrier mobility, high on/off current ratio, low power consumption, and steep subthreshold swing, as sought for by the FETs in microelectronics. However, the electronic performance of the TFTs is seriously limited by the poor lattice quality in the disorder, amorphous or polycrystalline thin film materials, which are now dominated by amorphous Si (a-Si), low-temperature poly-Si (LTPS) and indium–gallium–zinc oxide (IGZO) TFT technologies[91] in the display industry.

A-Si TFTs are the only technology that can be scaled up to the Gen. 11th production lines with substrates measured around 3.2 m × 3 m. However, its application to high resolution display is limited by a low carrier mobility of only ≈1 cm^2 V^{-1} s^{-1}.[89] LTPS TFTs are fabricated upon poly-Si thin film, with higher carrier mobility ≈100 cm^2 V^{-1} s^{-1},[46b,90] by using excimer laser scanning crystallization of a-Si thin film, which are now used for high resolution displays dominantly in mobiles or laptops.[94] However, the size of the LTPS technology is limited by much smaller Gen. 6.5th production, mostly because of the complexity and scalability of laser scanning crystallization equipment. Actually, to these large area TFT applications, a high yield and high throughput production of semiconducting Si NWs, with high crystallinity, nanometer-sized diameters and proven high mobility, could be an ideal choice. However, the challenge is to place the NW building blocks into precise locations upon large area substrates, where one-by-one manipulation of NWs or the use of high precision lithography technologies such as EBL is unacceptable.

Built-on the unique capability of IPSLS growth mechanism in achieving precise growth orientation and position control, Xu et al. recently proposed an in-plane droplet-scanning crystallization technology to batch-manufacture in-plane SiNW arrays as high mobility channels for construction advanced fin-TFTs.[67] The SiNW fin-TFTs were fabricated upon glass and wafer substrates, via a procedure sketched schematically in **Figure 17**. As described previously in the in-plane growth of SiNWs, the SiNWs were catalyzed by using In nanodroplets with a-Si thin film as precursor layer. The growth of in-plane SiNWs is guided by predefined simple edge lines, formed by etching into the glass or oxide-coated wafer substrates. SiNWs growth started from the crossings of the In stripes and the guiding edges, where the In droplets were formed by H_2 plasma treatment and trapped by the nearby step edges to produce horizontal SiNWs along at the root of and along the step edges. It is important to note that, for TFT device applications, the remnant a-Si



A	B	C_{in}	S	C_{out}
0	0	0	0 (0 V)	0 (0 V)
0	0	1	1 (2.5 V)	0 (0.6 V)
1	0	0	1 (2.4 V)	0 (0.6 V)
1	0	1	0 (0.3 V)	1 (2.0 V)
1	1	0	0 (0.3V)	1 (2.5 V)
1	1	1	1 (2.3 V)	1 (2.7 V)

Figure 15. Nanoprocessors constructed upon the in-plane Si/Ge core–shell NWs. a) Schematically the configuration of the NW FET device, b) with a cross-section TEM image. c) Transfer and memory properties of the FET device under different programming conditions. d) The two-block tile arrangement of the NW arrays, where the cyan lines stand for the Ge/Si NWs with blue electrodes, purple for dielectric layers, and gray for metal gates. e) The distribution of the V_{th} of 70 NW FET nodes in block 1 in the first tile. f) Output voltage levels for six typical input states. g) Circuit design for implementing one-bit full adder. h) Voltage transfer function for S (red) and C out (blue) for input states of (0, 0, 0) to (1, 1, 1). i) Truth table of full-adder logic for the six input states. a–i) Reproduced with permission.[5f] Copyright 2011, Springer Nature.

layer can be selectively removed by a low temperature (100 to 150 °C) H_2 plasma etching, which preserved only the SiNWs on the surface. A rather high SiNW activation and growth rate >98% has been demonstrated, via a low temperature procedure (350 °C for the annealing growth step), indicating a promising potential to be scale up upon large are substrates within the framework of basically an a-Si TFT technology. Furthermore, when the SiNW array was grown upon glass substrates, guided by step edge lines separated 3 µm apart, which is the typical lithography resolution for large area electronics, the overall SiNW/glass sample is 80% transparent. This is because the tiny SiNW channels have an average diameter of only 60 nm, which is much smaller than the visible wavelengths (400 to 700 nm). Therefore, the incident lights are only slightly scattered by the sparse but orderly SiNW arrays. This feature is beneficial for developing high aperture or even transparent displays in the future. Importantly, the Fin-TFTs fabricated upon the SiNW arrays demonstrate a high mobility of 100 $cm^2\ V^{-1}\ s^{-1}$, a high on/off ratio $\approx 10^6$ and a subthreshold swing of 163 mV dec^{-1}, as well as a threshold voltage lying very close to 0 V.[67] There performances are comparable and even superior to the best LTPS TFTs in the market, but accomplished via a scalable low temperature Si thin film technology, having the potential to establish a new TFT technology routine for large is high-resolution display applications. A comparison of the key performance of the FET or TFT devices, based on 1D NW or CNT channels, in the literature is presented in **Table 2**. Despite of these encouraging progresses, the potential of planar NWs for industrial TFT application has yet to be examined and verified in many critical aspects, such as large area scaling, cost control, process compatibility, and device reliability.

5.3. Stretchable Electronics

The ability of in-plane growth of SiNWs, of several hundred micrometers to millimeters long, into precise locations allows for a programmable line-shape engineering of the c-Si nanochannels. It has been well known that the crystalline bulk Si, the dominant semiconductor material that underpins large scale integration of microelectronics and the development of modern information society, is intrinsically rigid and brittle, which is unable to sustain large bending and stretching strains. However, the development of biocomfortable sensors

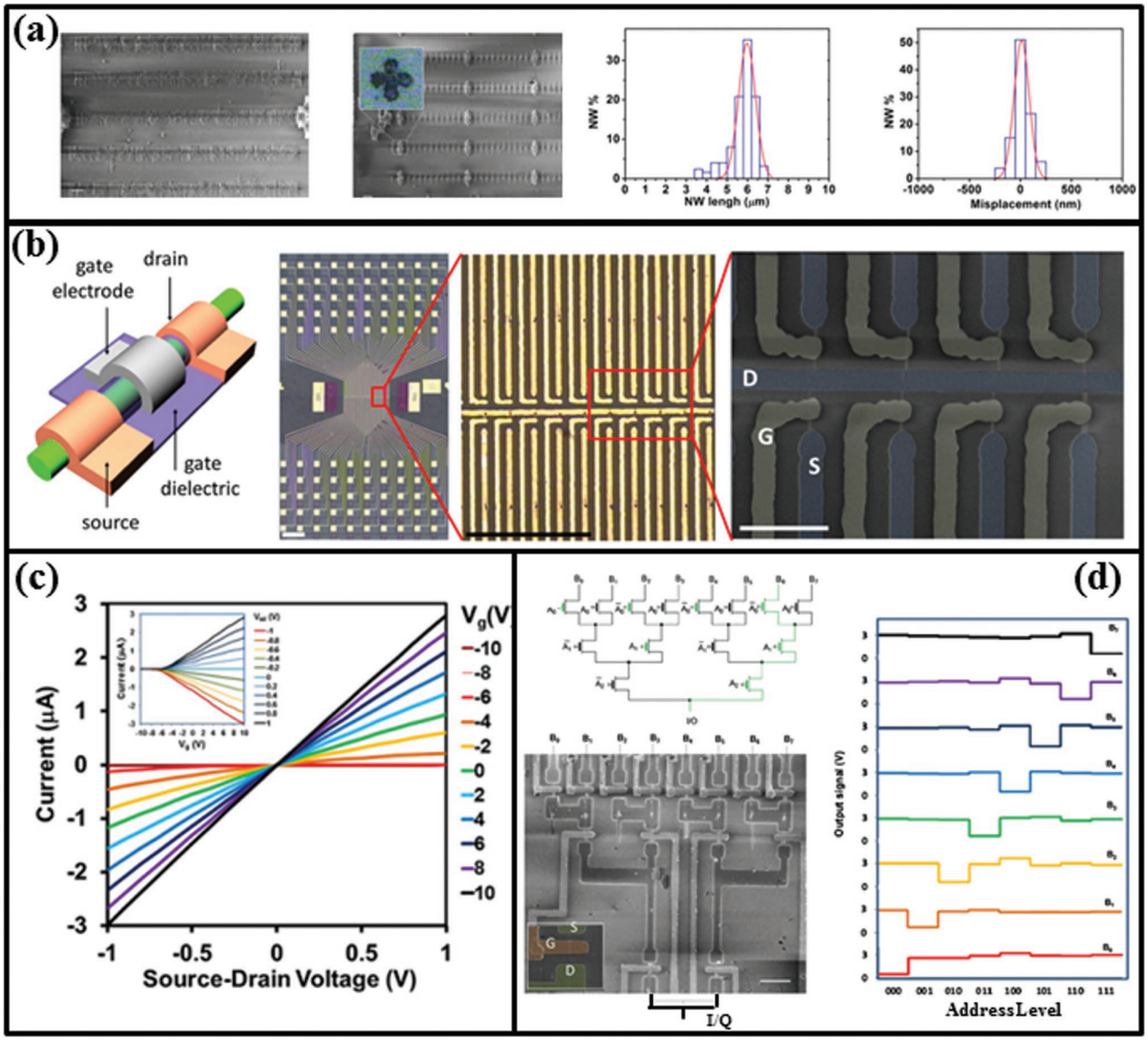


Figure 16. Epitaxial growth of orderly arrays of horizontal ZnO NWs on R-plane sapphire and FET devices. a) SEM images of the NW arrays with intervals of 2 and 6 μm, and their corresponding length distributions. b) Device fabrication and electric connections on the NW array. c) Output curves of a top-gated ZnO NW transistor (inset: the transfer curve). d) Schematic diagram of a three-level tree address decoder and the device characterization. The left-bottom inset is the SEM picture of the NW decoder, composed of 14 interconnected ZnO NW FETs. The scale bars in (b) and (c) are 8 μm and 6 μm, 50 nm, 200 nm, 1 nm, 10 nm, and 10 nm, respectively. a–d) Reproduced with permission.[37] Copyright 2013, National Academy of Sciences.

and electronics upon soft, curvilinear, and deformable skins or tissue surfaces[104] or stretchable displays[105] require an elastic mechanical property of the electronic circuitry that bulk Si wafer is hard to offer, as it can sustain only a very limited tensile strain up to 0.1%.[106] That is why, so far, most of the stretchable electronics have been prototyped by using polymer and organic semiconductors,[107] where the electronic characteristics, in terms of carrier mobility, doping control, passivation technology, and mostly importantly the stability are evidently inferior compared to that can offer by c-Si based electronics.[107] Therefore, many recent research efforts have been devoted to fabricate stretchable Si nanospring channels, by using EBL, etching and patterning, out of monocrystalline Si box layers in SOI structure.[108] For example, elastic 2D ribbons, serpentine, and fractal layouts,[109] buckled 3D out-of-plane wrinkles enforced by contractive elastomer,[110] sinusoidal SiNW springs grown via VLS mode[111] have been prepared to achieve largely stretchable c-Si channels. Particularly, the VLS growth of NWs within predefined 1D nanochannels patterned by using EBL,[19b] demonstrates a unique capability for programmable line-shape or geometry engineering of the 1D NWs, with diameters of 80 to 120 nm.[19b] Despite of these successful demonstration of stretchable NW springs, the use of EBL is still too expensive to scale up for large area electronics. Actually, in view of a planar

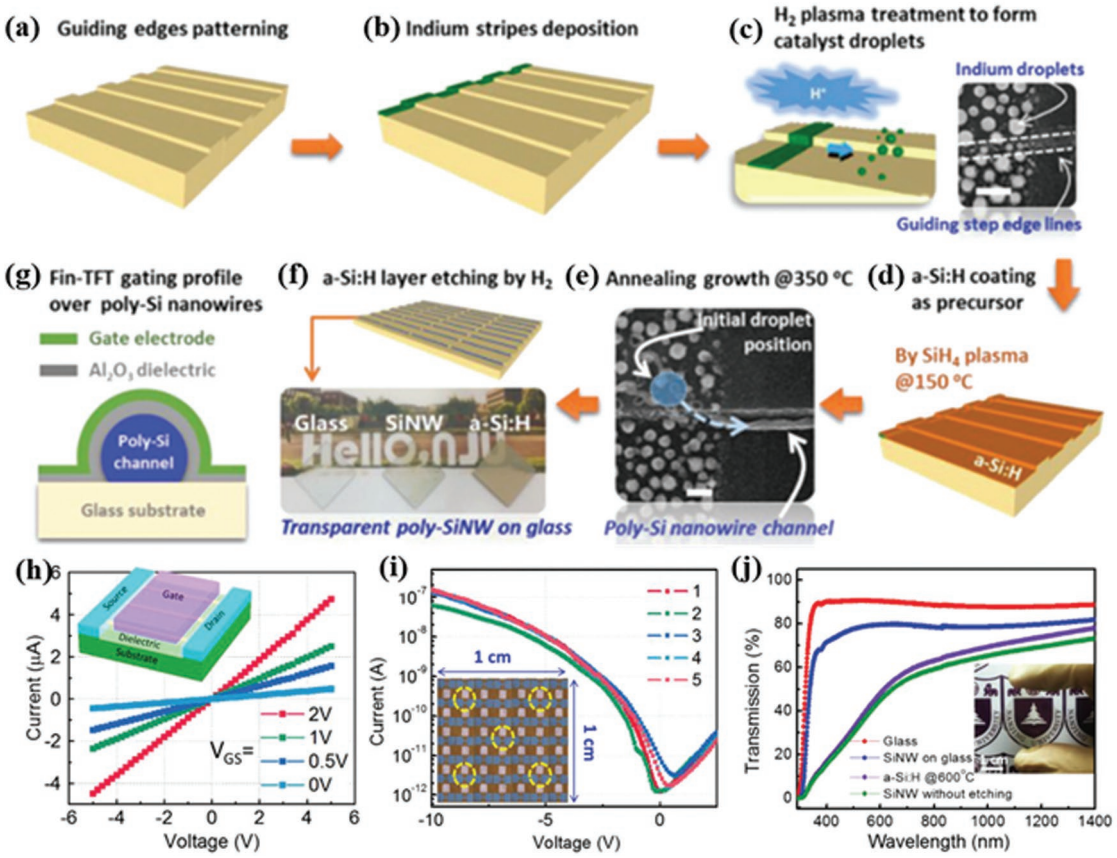


Figure 17. In-plane growth of SiNW array on glass or wafer substrates for thin film transistors (TFTs) in flat-panel display. a–d) The fabrication procedure of guided growth of parallel SiNWs, led by In droplets. e) SEM image of the SiNW grown from the crossing of guiding edge with In stripes. f) SiNWs grown upon glass substrate, compared to the samples of glass with or without a-Si coating. g) The cross-section configuration of the fin-gate SiNW TFT device. h) The output curves of a top-gated TFT device with 30 parallel SiNW as channel. i) Transfer curves of five different devices marked by yellow circles in the inset. j) Transmission properties of glass, SiNW on glass, a-Si on glass, and SiNW without etch on glass. a–j) Reproduced with permission.[67] Copyright 2017, Royal Society of Chemistry.

Table 2. Comparison of the key performances of FETs based on 1D NW or CNT channels.

Channel	Method	Structure	T_{growth} [°C]	I_{on}/I_{off}	μ_{FE} [$cm^2 V^{-1} s^{-1}$]	SS [$mV\ dec^{-1}$]	Ref.
CNT	CVD	Orderly	900	≈10^4	1600	125	[92]
Single wall CNT	Dip-coating	Random	<150	10^5	46	109	[93]
Single wall CNT	CVD	Single	900	≈10^7	3300	100	[94]
ZnO NW	MBE	Single	945	10^7	61.7	115	[95]
ZnO NW	Hydrothermal	Single	600	10^7	>50	≈100	[96]
SnO_2 NWs	CVD	Orderly	1400	≈10^6	71.68	≈200	[28b]
Ta-doped SnO_2 NW	PECVD	Single	900	≈10^4	179	312	[97]
In_2O_3 NW	CVD	Single	Laser-ablation	10^5	243	≈200	[98]
In_2O_3 NWs	Electros-pinning	Random	400	8.7×10^7	9.4	580	[99]
InGdO nanofiber	Electros-pinning	Random	150	4×10^8	17.4	160	[100]
SiNWs	Printing	Random	270	≈10^7	15	250	[101]
SiNWs	Supercritical-fluid–liquid–solid	Random	<300	4×10^6	2	600	[102]
SiNWs	PECVD	Orderly	350	6.4×10^5	100	163	[67]
SiNWs	PECVD	Orderly	350	>10^7	60	330	[103]

assembly and applications of stretchable NWs, planar growth of NWs represents arguably a more straightforward and convenient approach.

As proposed and demonstrated by Xue et al. 2017,[112] the self-assembly growth of SiNWs out of molten catalyst liquid droplets resemble, to some extent, the crystal pulling of c-Si ingot from molten Si (see **Figure 18**a). So, in order to program the geometry of the SiNWs, one should manage to control the moving course of the leading droplets, which has become possible with the guiding growth technology for the IPSLS growth. The SiNW springs, grown along predefined horseshoe or more complex 2D Peano patterns, defined by conventional lithography (Figure 18b). It is found that the in-plane growth of SiNWs with a diameter of around 80 to 100 nm can be quite stable, given proper controlled growth parameters, over a long travel distance of more than several hundreds of micrometers, which is a key basis for the geometry engineering to form more complex and potentially more functional NW patterns. Meanwhile, the authors also investigated and discussed the stability of guided growth over convex and concave turning places, and it is found that deviations from the growth balance conditions can indeed cause nonuniform diameter (island-chain

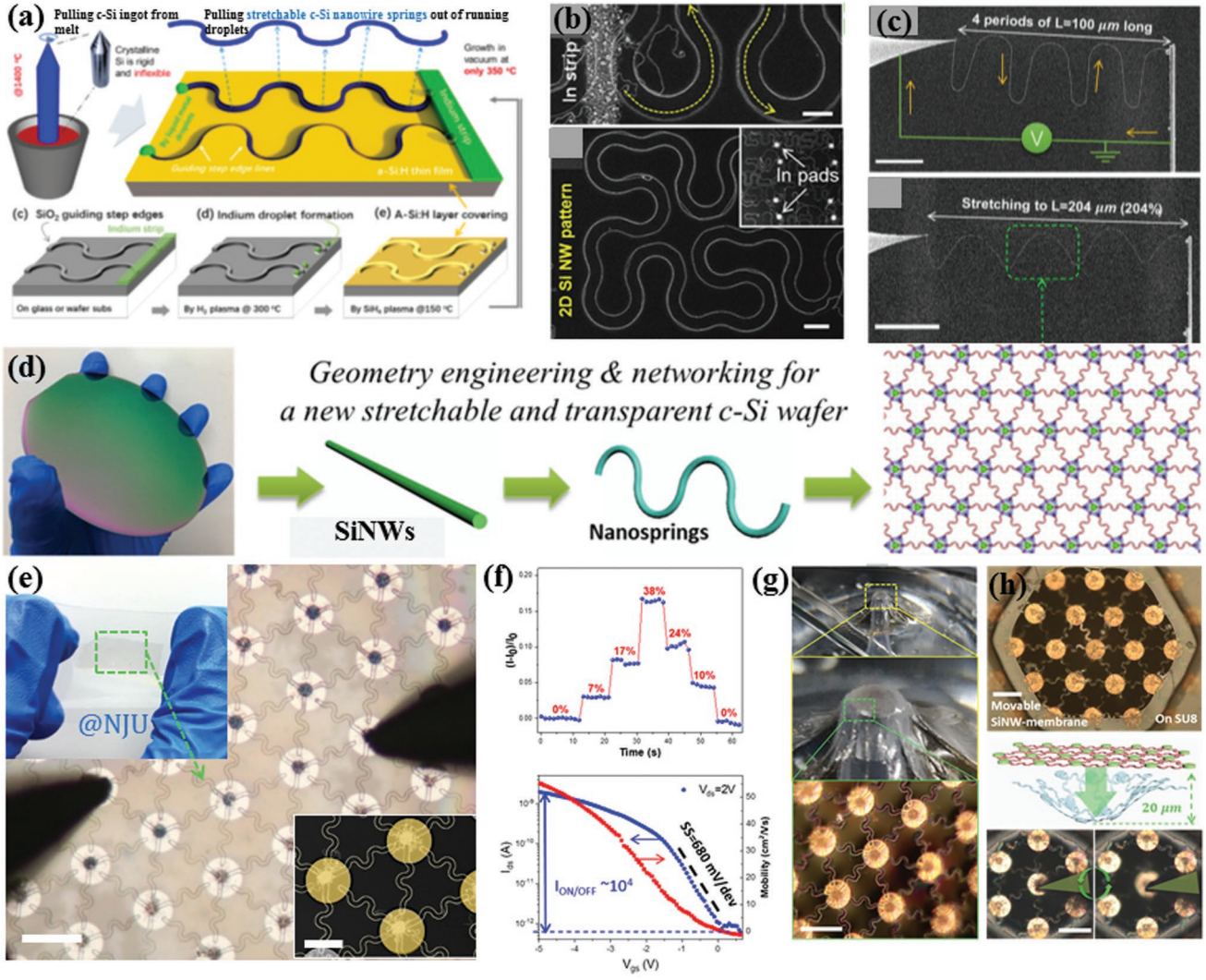


Figure 18. a) The fabrication procedure of elastic SiNW springs via step edge engineering, b) with corresponding SEM images of the SiNWs grown into Peano and horseshoe patterns. Scale bars are 5 and 10 µm, respectively. c) The in situ stretching and *IV* measurement testing of a SiNW spring segment. Scale bars are 25 and 50 µm, respectively. d) The strategy to form continuous SiNW spring network, toward establishing a stretchable and transparent c-Si wafer technology. e) Microscopy image of a SiNW network transferred to PDMS elastomer, with insets showing the photos of stretched SiNW-network@PDMS thin film by hands and the SEM image of the network joint by Pt/Au electrode pads. Scale bars in (e) and its bottom-right inset are 50 and 30 µm, respectively. f) Top panel: the variation of the transport current measured under a constant bias of V_{ds} = 10 V when subject to different stretching strains. Bottom panel: the transfer property of the SiNW network FET fabricated upon 450 nm SiO_2-coated wafer with a bottom-gate configuration. g) Attaching the soft SiNW-network@PDMS layer conformally to the tip of a pointed tube and its close-up photo image (scale bar for 50 µm). h) Self-sustained suspended SiNW network membrane over a hexagonal void formed in SU8 thin film, and the illustration and photos of their elastic deformation and recovering under the pressing of probe. Scale bars are for 50 µm. a–c) Reproduced with permissions.[112] Copyright 2017, American Chemical Society. d–h) Reproduced with permission.[113] Copyright 2017, American Chemical Society.

structure) modulation and even breakage the convex turning, or derailing of SiNWs from the guiding tracks at the concave bending. Remarkably, HR-TEM analysis of a half-cycle segment of the SiNW spring reveals that, despite of the largely engineered line-shape, the lattice images taken at different places along the bend are almost coherent, indicating a high crystalline quality in the NW springs.

Mechanical testing of the geometry engineered SiNW springs were carried out in SEM chamber by using nanomanipulator. A SiNW spring of four periods long was chosen and connected at the one end to an AFM tip and the other end to a probe, spanning an initial distance of 100 μm (Figure 18c). The bonding of SiNW to the tip or probe was realized by amorphous carbon deposition in the SEM chamber. Then, the spring was pulled or stretched to different extents up to 204%, that is double the initial span of the NW spring, and current–voltage curves were recorded at different stretching status. Impressively, a rather stable electric transport can be sustained under large stretching. The resilient force of the NW spring was calculated by using finite element simulation, which predicted a stiffness according to Hooke's law, of only $k = 4.3 \times 10^{-5}$ N m^{-1}. The simulation also revealed that the maximum tensile (compressive) stress accumulated at the inner (outer) edge over a bending with local radius of 3.5 μm, is still <140 MPa, which is well below the fracture limit of c-Si, ranging 2 to 10 GPa.[106] This programmable and deterministic line-shape engineering of ultralong SiNWs has a potential to batch-manufacturing high quality NW channels for stretchable sensing and logics. More recently, a so-called "soft wafer" technology has been successfully demonstrated by assembling the SiNW springs into a quasi-continuous and highly stretchable network (Figure 18d), which can be batch-manufactured and reliably transferred to soft PDMS elastomer, providing an ideal basis to construct a new generation of stretchable FETs (Figure 18e,f).[113]

Interestingly, the line-shape engineered SiNWs provide also ideal scalable nanomasks to pattern 2D materials into nanoribbons, as recently demonstrated by Liu et al.[115] Graphene nanoribbons (GNRs) are widely considered as promising candidates to serve as flexible and transparent interconnections or semiconducting channels for nanoelectronics.[116] However, to be integrated into microelectronics, GNRs have to be patterned to narrow width <100 nm, usually formed by etching out of graphene monolayer with the aid of expensive and inefficient EBL technology. Meanwhile, it is also important to engineer the geometry of the GNTs into elastic spring shapes, so as to achieve large stretchability catering to the needs of flexible and stretchable electronic and sensor applications. The maximum strains tolerable to graphene sheets or GNRs are in the ranges of 1% to 3%,[117] while GNRs patterned into 2D zigzag, serpentine spring shapes[118] or 3D wrinkles[119] to achieve a stretchability up to 30%.[119] In addition, the 2D zigzag or serpentine spring channel design is also subject to a geometric constraint, that is the ratio of the bending radius over the GNR width, $g \equiv R_{\text{bend}}/D_{\text{GNR}}$, has to be large enough, typically >20, to avoid local strain concentration effect (otherwise cracking will emerge).[120] Therefore, a narrow GNR channel width is also critical to reduce the overall spring channel dimensions for designing stretchable GNRs or NWs nanochannels (**Figure 19**a), a scalable and precise nanowire lithography (NWL) technology was demonstrated by taking the ultralong and orderly IPSLS SiNWs as masks. The geometry-designed SiNW array was transferred onto monolayer or few layer graphene sheet, serving as shadow masks to pattern the underlying graphene sheets and produce very thin GNRs of only 50 nm wide over large area wafer or flexible polymer substrates. Importantly, the programmable line-shape engineering was inherited from the NW array to fabricate basically any one-touch-draw 2D patterns of GNRs, including even a nanoscale "NJU" logo for Nanjing University, written by in-plane NWs and GNRs (Figure 19b). Compared to the NWL technology demonstrated before by using relatively simple, straight, and random VLS grown SiNWs,[4c] or by printing organic nanowires via sequential electrohydrodynamic approach,[121] this approach boasts a higher level of manipulability and a high efficiency in batch-manufacturing orderly GNR array with elastic line-shapes to achieve a large stretchability >30%, as indeed witnessed in the stretching and IV characteristic measurements. This NWL technology could also find applications in batch-patterning or integrating other 2D materials as active channels and interconnections for the advanced flexible electronics.

5.4. Extensions to 3D Growth and Integration

Though the planar growth of NWs, via IPSLS or VLS modes, has been developed on flat substrate surface, where the NWs are either constraint by the amorphous feeding precursor,[42,60,61,112,122] surface channel templates[19] or epitaxial interfaces,[22,36d] their potentials are not just limited to simple flat surface. Particularly, taking the IPSLS growth of SiNWs as example, the catalyst droplets are attracted by the feeding a-Si layer that can be coated basically on whatever surface, being it flat, vertical or curved, and this offers a unique capability to deploy them over the extra surfaces that are difficult to address by conventional lithography technology. This capability is crucial for building 3D electronics, where an important promise is to integrate more functionalities into a given footprint area. The extra space in the *z*-axis dimension, on the out-of-plane oblique or vertical sidewalls, can also be in principle used to accommodate more electronic units for achieving even higher density integration. Indeed, more and more recent efforts have been devoted to the fabrication of 3D multichannel structures, comprising of stacked lateral SiNW channels.[5i] Note that, this stacked channel configuration is considered more convenient and practical for reliable electric connection and addressing via standard mature planar processing, compared to the vertical channel device configurations, which require usually much more complicated processing to achieve electric connection. Stacked SiNWs have been manufactured by using a carefully controlled Bosch etching[123] or a selective etching and oxidation of epitaxially grown Si/GeSi multilayers,[124] and their superior electronic properties have been indeed verified in stacked channel FETs.[5i] Most of them require high precision EBL lithography on SOI substrates,[123b,c,124b,125] as well as unfavorable high temperature >1000 °C processing.[123c] In comparison, for the self-assembly growth of SiNWs, the leading catalyst droplets really tiny and thus basically insensitive to the influence of gravity, which is negligible in comparison to

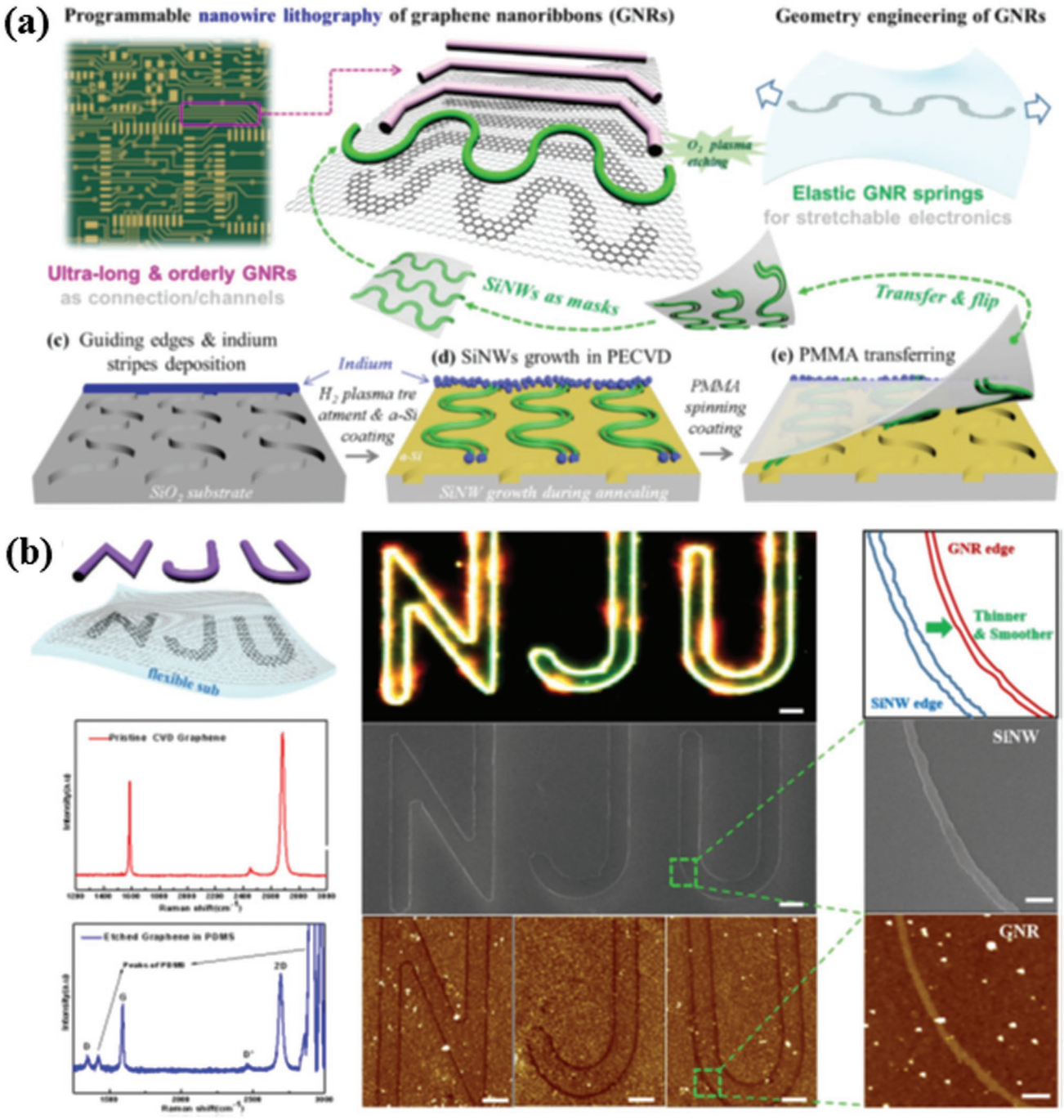


Figure 19. Graphene nanoribbons (GNRs) patterned by a programmable SiNW lithography. a) Schematically the graphene nanoribbons etched with transferred SiNWs as mask. b) Writing of GNR "NJU" logo by using engineered SiNWs as masks, characterized by using SEM, optical microscopy, and AFM, as well as the Raman spectra of the graphene samples before or after the SiNW lithography etching (in the left panels). The scale bars in the middle and the right pictures of (b) are 2 µm and 200 nm, respectively. a,b) Reproduced under the terms of the CC-BY Creative Commons Attribution 4.0 International License (http://creativecommons.org/licenses/by/4.0/).[115] Copyright 2019, The Authors, published by Springer Nature.

strength of surface or interfacial tensions in nanoscale. This makes it possible for the metal droplets to take on the roles to work on the out-of-plane surfaces, and to deploy the critical discrete and well-defined semiconducting NW channels, directly on the extra vertical/oblique sidewalls for incorporating more nanochannels for devising. For the famous VLS growth of SiNWs, SiNW bridges can be grown directly on the facing sidewalls and electrodes over a gap,[126] but unfortunately, a precise location and level height control is still rather difficult.

Very recently, 3D vectorial sidewall growth of SiNWs on vertical or oblique sidewall surfaces has been demonstrated by Wu et al.,[103] where they explore metal catalyst droplets to absorb

sidewall-coated a-Si thin film to produce orderly 3D multilevel lateral SiNW stacks, via an IPSLS growth mechanism, following the guidance of sidewall terraces (**Figure 20**a), the oblique sidewall terraces can be formed by adopting a simple alternating etching technique, where a photoresistor resin of is first patterned upon a thick SiO_2 layer, which serves as the mask for subsequent C_4F_8 etching by using ICP plasma to form the first ministep; then, O_2 plasma is applied to erode the edges of photoresistor strips, forcing the edge to retreat and expose a new plateau for the next ministep. Repeating these two steps for N times yield eventually an oblique sidewall terrace comprising of N ministeps with tunable ministep profiles. For example, the SEM images show that oblique ministep terraces (tilted at ≈53°) with four ministeps of 160 nm height and 120 nm wide. Note that the formation of such high density ministeps has been accomplished via an alternating ICP etching with the use of only conventional and scalable (to large area substrate) lithography technology. Another approach to fabricate vertical sidewall grooves was accomplished by a selective etching of the exposed sidewalls of stacking SiO_2/SiN_x multilayer (Figure 20b), where a uniform multilayer is first deposited with designed sublayer thicknesses, followed by a treatment of 5% HF solution to selectively attack the SiO_2 sublayers, as the etching rate of SiO_2 is at least ten times faster than that of SiN_x. This produced periodic concave grooves on vertical sidewalls, as witnessed in the SEM image (Figure 20b). Note that, while the edge-to-edge spacing among oblique sidewall ministeps is still limited by the finite plateau width, as well as the catalyst

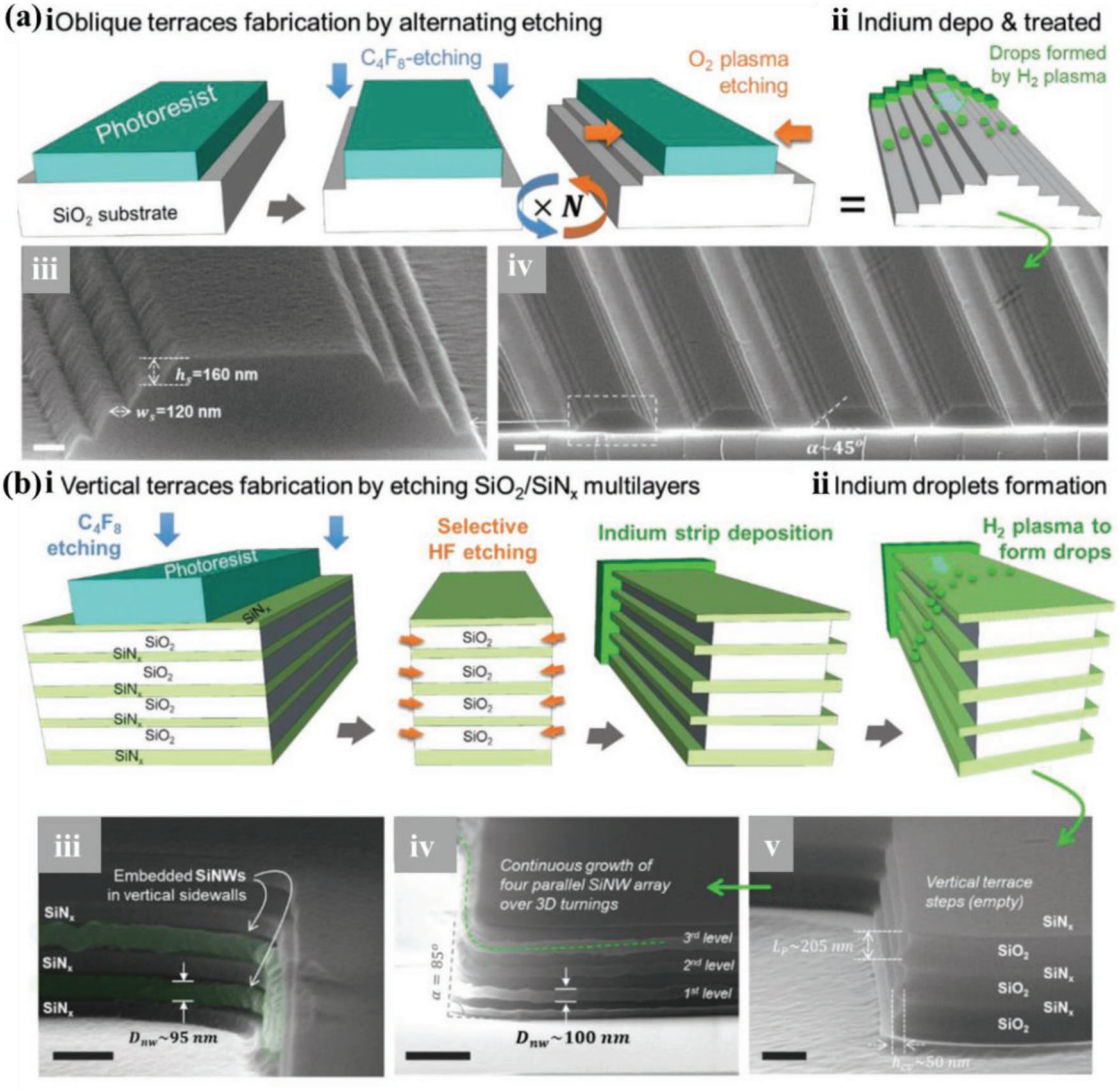


Figure 20. 3D guided growth of SiNWs upon the oblique terraces or vertical sidewall grooves. a) (i) Fabrication procedure of the oblique sidewall terraces by alternating C_4F_8 plasma (for etching SiO_2) and O_2 plasma (for etching photoresist) processes in ICP system. (ii) Deposition of indium catalyst stripes by thermal evaporation. (iii,iv) The SEM picture of the oblique terraces and the as-grown SiNWs. b) Vertical sidewall grooves formed by etching SiO_2/SiN_x multilayers. (i) Multilayer etching by using C_4F_8 plasma in ICP, followed by lift-off and selective HF etching of the SiO_2 sublayers to form concave grooves. (ii) H_2 plasma treatment to transform In stripe to droplet. (iii–v) The SEM images of the vertical sidewall grooves, with and without SiNWs growth, respectively. The scale bars in (a) and (b) are 200 nm, 1 µm, 300 nm, 600 nm, and 400 nm, respectively. a,b) Reproduced with permission.[103] Copyright 2019, Wiley-VCH.

diameter, a vertical sidewall guiding terrace can help to break this geometric limit, as the SiNWs grown on the vertical sidewall have always a constant footprint of a single SiNW channel width. For instance, by controlling the SiO_2 and SiN_x sublayer thicknesses to be ≈160 and ≈45 nm, respectively, after a selective HF etching, clear sidewall grooves were developed with a separation of ≈205 nm and a smooth caving depth of ≈50 nm.

With these 3D sidewall ministeps or grooves, a reliable deployment of sidewall-positioned or just suspended long SiNW array, with diameter of 50 nm and inter-NW spacing ≈100 nm, has been accomplished, without the use of high resolution lithography. Prototype FET devices built upon the stacked multilevel channels demonstrated a rather high on/off current ratio $>10^7$, a hole mobility ≈60 mV cm^{-2} and a low leakage current down to 0.1 pA for a channel consisting of 6–7 SiNWs. These results open a new way toward the integrating more stacked channel for FET devices, which is beneficial for boosting the drive current (when serving as TFTs in flat panel displays) for AMOLED applications, or developing other novel 3D electronic and NEMS applications.

6. Conclusion and Perspectives

A precise and reliable planar growth/arrangement of semiconducting NWs represents a key milestone toward scalable integration into planar electronic architecture, which is now and will continue to be the most convenient platform to prototype and deploy various NW-based functionalities. Three major strategies have been reviewed to accomplish this goal, via: (1) vertical VLS growth of NWs and precise transferring and rearrangement, (2) lateral VLS growth of NWs confined and directed by homo- or heteroepitaxial interface, nanochannels, and templates on surface, and (3) IPSLS growth of in-plane NWs with surface-coated thin film as precursor. In addition, it is shown that a surface-confined planar growth brings in a set of new growth control strategies to engineer the geometry, doping, and composition of NWs. A faithful planar guided growth enables potentially a large scale integration of orderly bottom-up NW array for batch-manufacturing high performance photodetectors and FETs. Furthermore, designable growth pathways and programmable line-shapes of in-plane NW can help to endow extra flexibility and even stretchability to the intrinsically rigid NW channels. It is also observed that the in-plane growth technology is also applicable to out-of-plane and curved surfaces that are inaccessible by conventional lithography technology. Most of these new capabilities and strategies are derived from the fundamental aspects of self-assembly growth control, highlighting the potential of new bottom-up approaches to grow, integrate, and deploy high quality NW building blocks in planar architecture for advanced functionalities.

In the future, the potentials of self-assembled NWs for building a wide variety of electronic logics, sensors, or photodetector applications have yet to be testified in practical and specific implementation backgrounds, especially in planar circuitry architectures for scalable device fabrication. For the synthesis-then-arrangement approach, based on VLS-grown NWs, the assembling technology has to be low-cost, precise, and importantly compatible with the standard electronic procedure. The rich compositional choices for VLS-grown NWs and the possibility to assembly them layer-by-layer into complex 3D network provide a unique basis to explore new functionalities and architectures for more advanced, powerful or power-efficient logics, memories, and sensors. In parallel, the epitaxial growth of NWs, obtained via VLS or IPSLS mechanisms, is promising for constructing a wide range of homo-[127] or heterojunction applications,[28c,79f,83,128] where the lattice mismatch can be well dissipated at the nanoscale epitaxy interfaces and the different band alignment can be exploited to explore high performance transistors,[79f,127] versatile photodetection,[79f,83] and flexible imaging.[128b] In view of large area electronics and optoelectronics, a reliable and cost-efficient growth and transfer technology of the epitaxial NWs is desirable, particularly for those of high quality III–V or II–VI material systems. For the IPSLS mechanism with amorphous thin film as precursors, extending this in-plane growth approach, now limited to Si or Ge NWs with corresponding a-Si or a-Ge precursors, to other semiconducting materials (elementary, compound or hybrid organic and inorganic) is particularly interesting, urgent and rewarding, if succeed. In short, the research on planar growth and integration of semiconducting NWs will continue to forge new understanding, new principles, and new approaches to explore the self-assembly NWs for building advanced nanoelectronics and optoelectronics, with a particular focus on developing reliable strategies to narrow or bridge the gap between fundamental research and practical applications.

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Conflict of Interest

The authors declare no conflict of interest.

Keywords

arrangement and integration, inorganic semiconducting nanowires, nanowire electronics, planar self-assembly growth

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