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• REVIEW •

Special Topic: Recent Progress of Fundamental Research on Post-Moore Novel Devices

Toward monolithic growth integration of nanowire electronics in 3D architecture: a review

Lei LIANG[1], Ruijin HU[2] & Linwei YU[1*]

[1]*School of Electronic Science and Engineering, Nanjing University, Nanjing* 210023*, China;*
[2]*School of Physical Science and Technology/Microelectronics Industry Research Institute, Yangzhou University, Yangzhou* 225002*, China*

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Abstract Quasi-one-dimensional (1D) semiconducting nanowires (NWs), with excellent electrostatic control capability, are widely regarded as advantageous channels for the fabrication of high-performance microelectronics, memories, and sensors. For example, the latest Si field-effect-transistor (FET) technology nodes, <N5 nm, use horizontally-stacked SiNWs or nanosheet channels in a gate-all-around (GAA) configuration. However, further scaling of the top-down etching fabrication is reaching physical limits, necessitating the development of new fabrication or integration technologies in monolithic three dimensional (3D) architecture to push Moore's law forward. These new capabilities are also critical, for implementing of more advanced non von Neumann paradigms of in-memory and neuromorphic computing. For this, a versatile and highly controllable low-temperature growth integration of orderly 1D SiNW channels is desired, as it will provide an alternative or complementary new route to fabricate a multilayer of Si CMOS logics/memories in a fully 3D stacked manner. In this study, we assess the evolution and recent progress of catalytic growth strategies for ultrathin 1D channels in-plane or planar NWs, and revisit the key mechanisms and technological milestones in geometry, lattice quality, line-shape, position, and composition controls. We aim to eventually establish a reliable catalytic growth integration strategy, suitable for the fabrication of GAA FETs and the implementation of a monolithic 3D integration architecture. Finally, we also present a summary and perspectives on the current challenges and future opportunities of monolithic growth integration of NW electronics in 3D architecture.

Keywords catalytic growth, silicon nanowires, electronics, monolithic 3D-integration

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1 Introduction

The last decade has witnessed an explosion in demand for computing power for the implementation of emerging applications such as deep learning [1–3], artificial intelligence (AI) [4–7], big data [8, 9], and block-chains [10], all of which have profoundly transformed our daily lives in almost every aspect and reshaped our visions of future technology landscapes. In other words, computing power will become the most important form of productivity and competitiveness in the digital economy. As the most abundant, mature, and well-known semiconductor material, crystalline silicon (c-Si) has long served and will continue to serve as the most sophisticated, dependable, and cost-effective technology platform for the development of large-scale integration microelectronics, underpinning the entire digital society, economy, and civilization. To meet the increasing demands for computing power, Si-based microelectronic technology has evolved rapidly over the last half century, adopting novel structural designs and technical innovations, as part of an aggressive size downscaling of the fundamental logic unit of metal oxide semiconductor field effect transistors (FETs) [11–16]. Although there are several excellent reviews on the evolution and miniaturization history of Si-based microelectronics, following the famous Moore's law [11, 14, 17], we have prioritized only the trends and new opportunities of structural evolution, fabrication, and monolithic three dimensional (3D) integration.

* Corresponding author (email: yulinwei@nju.edu.cn)

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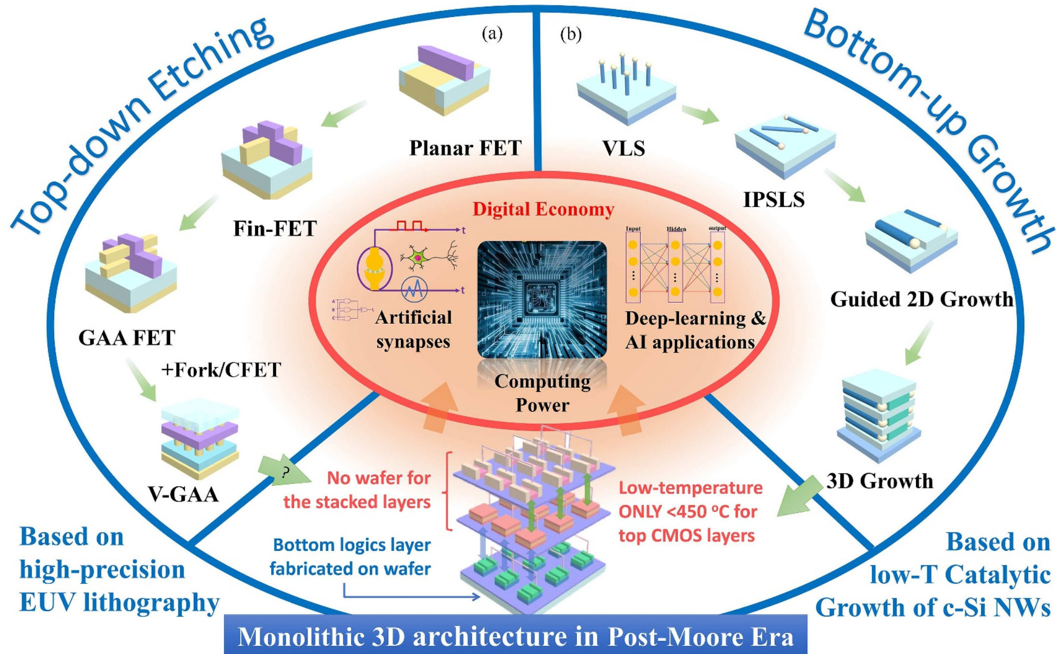

Figure 1 (Color online) Nanowires electronics based on (a) top-down etching, (b) bottom-up growth, and monolithic 3D architecture in the post-Moore era.

For example, in pursuit of stronger electrostatic control, a key capability for suppressing the short channel leakage with shorter channel length [12,14], planar FET channels have evolved into standing tri-gate configurations, in the technology nodes below 22 nm [11,14,18,19], as shown in Figure 1(a), followed by the adoption of more efficient 3D channels of horizontally stacked nanowires (NWs) or nanosheets (NSs) in a gate-all-around (GAA) FET structure, as introduced for N3 nm in 2022 [11,14,20]. It is crucial to note that, while these ultrathin 1D channels with a critical dimension <5 nm allow for the strongest channel-gate capacitive coupling for the transport current modulation [21–23], a single NW channel alone is inadequate to carry a large enough ON current to drive the fan-out logics [20,22,23]. Therefore, stacking a group of multilayer SiNWs in the vertical z-direction is a clever way to reduce the channel footprint area of a single FET unit. This discrete channel design of stacked SiNWs begins a new evolution journey for planar microelectronics to explore the vast space and opportunity in 3D architecture. Furthermore, the more advanced FET, such as fork-sheets FET (Fork-FET), (complementary FET) CFET and vertical-GAA (V-GAA) will also be discussed in Section 5. The fabrication procedure for the GAA FETs will be explained in Section 2.

Compared with stacking a group of multilayer SiNWs in the vertical z-direction, there is undoubtedly a simple way to integrate multiple logic/memory layers in a vertical stack. The vertical interconnection of silicon wafers or chips through Si vias technology [24–26], such as die-to-die bonding or chiplet technology [27], represents a mature technology route to boost the equivalent integration density, with the least modification of the established planar microelectronics. However, this transfer-bonding technology is commonly referred to as 2.5D integration, and is applicable only for block-to-block interconnection because its spatial alignment resolution is typically in the range of 1–10 μm, which is much larger than the feature sizes of individual logic gates [28,29]. In fact, achieving truly monolithic 3D (M3D) integration, with direct unit-to-unit interconnection among vertically stacked logic layers is critical to minimizing resistive loss and RC circuit delays [28,30–32]. Therefore, the second or the stacked logic/memory layer is supposed to be fabricated directly over the previous logic layer, as shown in the bottom panel of Figure 1. In this way, a relatively precise vertical alignment and efficient via connection can be guaranteed as a result of the mature advanced lithography and etching procedures, which is also a key capability in realizing the potential of M3D electronics, as a reliable alternative integration routine to push Moore's law further [28,30–33].

However, fabricating another stacked logic layer on top of the previous one is difficult and fraught with difficulties. There is no simple way to prepare another piece of highquality and thin monocrystalline Si wafer in the stacked layer, as provided in the planar microelectronic processing on c-Si wafer for the bottom

logic layer, also known as the front-end-of-line (FEOL) layer. Furthermore, to protect the integrity of the bottom FEOL layer, the fabrication of the second CMOS logic layer, which is usually the back-end-of-line (BEOL) processing, has to be $< 450°$C [23,34]. Thus, many recent efforts have been made to incorporate non-Si semiconductor materials, such as the 2D van der Waals materials, into the fabrication of M3D stacked logics [31, 35–37], and low-temperature processed metal oxide thin films [38, 39]. The former offers a diverse range of mono- or double-layer semiconducting materials, such as black phosphorous and transition metal dichalcogenides (TMDC), with atomically thin channel thickness, excellent tunability in the bandgap, and a fully passivated surface [31,36,40]. However, a reliable and scalable wafer transfer or growth deployment of these 2D materials has yet to be demonstrated for practical applications. Interested readers should refer to these wonderful recent reviews for the most recent progress in this approach [37,40]. Another non-Si alternative is provided by the amorphous metal oxide thin film, such as the mature indium gallium zinc oxide (InGaZnO or IGZO) technology, which can be uniformly deposited at a relatively low temperature over a large area and has been widely used as thin-film transistor (TFT) logics in the flat panel display industry [39, 41, 42]. Despite successful demonstrations of IGZO BEOL logics [43] with planar or vertical channel configurations, its relatively low carrier mobility, of $\sim$10 cm^2/Vs, the lack of complementary doping (only n-type) and the intricate stability issues pose limits to its application in high density integration of rather compact high-performance electronics, particularly in the latest or more advanced technology nodes, such as <N14 nm [39, 41, 44]. More in-depth reviews on this topic can be found in the literature for further reading [45, 46].

To extend the most mature, reliable, and high-performance c-Si CMOS technology into monolithic 3D integration, the first mission is to fabricate high-quality mono-like c-Si channels, ideally in advantageous ultrathin fin or 1D channel geometries, in the stacked or BEOL logic layer. For this purpose, the c-Si layer can be created by performing a solid phase epitaxy (SPE) of an a-Si layer, touching through holes down to the bottom seeding sites on the c-Si wafer surface, followed by a conventional top-down lithography and etching procedure to pattern the ultrathin 1D fin or NW channels [47,48]. However, the SPE formation of mono-like c-Si demands a high annealing temperature of $> 800°$C for achieving a lateral epitaxy growth rate of <100 nm/min [49]; hence, instead of the top-down etching formation approach, these ultrathin 1D channels can be directly generated from a low-temperature bottom-up catalytic growth strategy, commonly led by nanoscale metal droplets, by consuming gaseous or solid phase precursors [50, 51]. As shown in the right side of Figure 1, the catalytic growth of SiNWs or nanowhiskers, mediated by metallic particles, was discovered more than half a century ago [50–55], but their potential applications in nanoscale electronics were not fully recognized until the end of the 1990s, thanks to the development of more powerful and convenient characterization or observation tools and more sophisticated manipulation techniques, such as scanning electron microscopy (SEM), transmission electron microscopy (TEM) and film deposition equipment and so on [50, 54, 56–58]. Catalytic growth of SiNWs is best known as a high-yielding, low-cost fabrication method capable of producing various ultrathin NW structures with high crystallinity and at relatively low temperatures. Although high-performance SiNW-based prototype electronics and sensors have been effectively demonstrated based on the vapor-liquid-solid (VLS)-grown SiNWs collected and transferred onto a planar substrate surface [50,57–60], an exact spatial arrangement of these tiny building blocks, as orderly c-Si NW channels ready for electronic device integration remains a formidable challenge. This is, however, a key capability for this "bottom-up" growth strategy to establish a reliable integration routine that is compatible with planar or 3D monolithic device integration. This review focuses on their evolutionary history as well as their most recent progress.

Herein, we concentrate on the monolithic growth integration of NWs electronics in 3D architecture, which follows the bottom-up fabrication pathway as illustrated in Figure 1(b). This review is divided into the following sections. Section 2 provides a comprehensive overview of the evolution of top-down etching extending Moore's law scaling and functionality beyond non von Neumann paradigms containing in-memory and neuromorphic computing. Section 3 discusses the representative bottom-up synthesis of the VLS method, which can achieve high quality and composition control nanowires at low temperatures with the help of a catalyst, and as well as ways to position and transfer NWs. Section 4 shows a representative in-plane solid liquid solid (IPSLS) growth mode with position, geometry, morphology, and composition controls. Section 5 reports the most recent research advanced in 3D stacked nanowire structure with VLS and IPSLS precise growth integration, 3D stacked SiNW arrays application, vertical FETs and other materials used in 3D integration. Finally, in Section 6, the summary and perspectives about a brief review of the current challenges and future opportunities in NW development are provided.

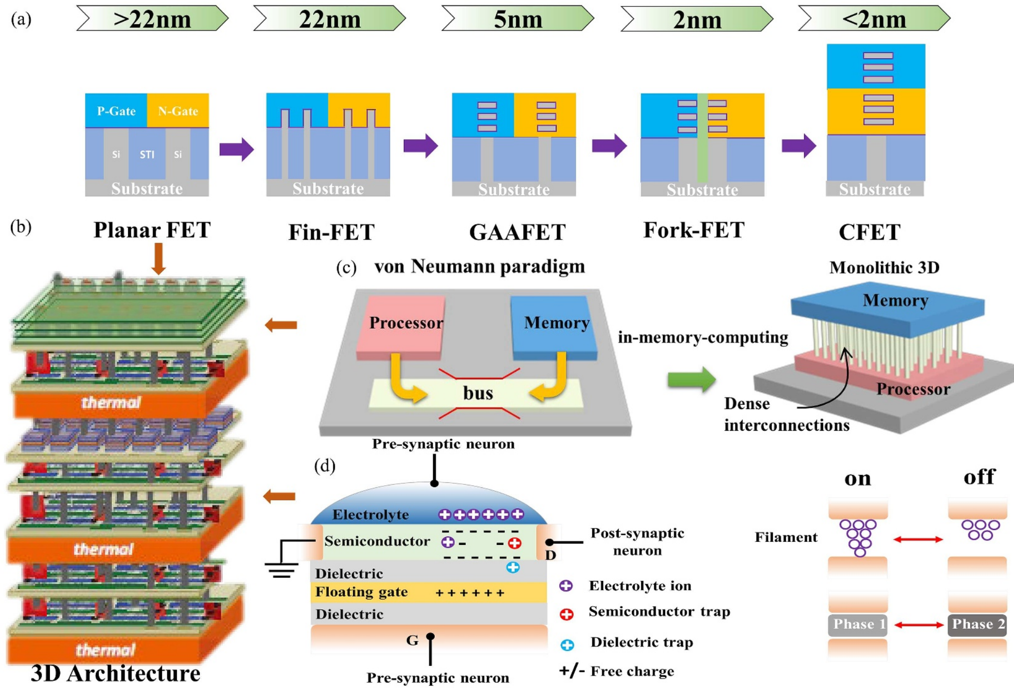

Figure 2 (Color online) Post-Moore's law, M3D, and non-von Neumann paradigms. (a) Transistor structures and architectures for Moore's Law continuation; (b) schematic diagram of M3D structures quoted from Figure 6 in [30] Copyright 2020 IEEE; (c) schematic diagram of in-memory computing [62] Copyright 2019 John Wiley and Sons, [32] Copyright 2017 Springer Nature; (d) schematic diagram of an artificial synapse and memristive switching [63] Copyright 2020 Springer Nature.

2 FEOL transistor evolution and non-von Neumann paradigms

The aggressive scaling of the dimension of FETs in Si microelectronics, following Moore's law over the last 60 years, has marked the most phenomenal technology development in human history. One of the key of driving forces is the pursuit of ever stronger electrostatic gating control over the semiconducting channels, which have evolved constantly from planar, fin-gate to GAA gating configuration, as illustrated in the top-down etching route in Figure 1, to gain an increased capacitive gate-channel coupling for more efficient current modulation and reduced leakage power consumption [12, 14, 61]. This is accompanied by rapid miniaturization of the feature size of FET, particularly the term of channel length frequently referred to as technology nodes, from fin-gate FET @<N22 nm to GAA FET @<N5 nm (see Figure 2 [62, 63]), all supported by the mighty high-resolution top-down EUV lithography and patterning technologies [16]. However, despite these landmark progresses, the evolution of Moore's law is running quickly into fundamental and economic limitations in single-digit-nanometer regimes, while the term "channel length" in technology node is no longer an exact physical measure of any feature size in the FET unit since N14 nm [14, 64].

The classic scaling of planar transistors by simply reducing the physical dimensions ended in Node 130 nm, even with the introduction of strained-silicon and high-k metal gate technologies, still hit the obstacles due to severe short channel effects (SCEs) issues in N22 nm. In order to obtain stronger electrostatic control over the channel, the architecture of transistors had a major revolution for the first time, evolving from single-gate planar to tri-gate three-dimensional fin. This transition allows the channel length to be shorter, meeting the demand for a smaller layout. Until now, the Fin-FETs are still the mainstream in the industry and will push the transistor roadmap to N5 nm by using self-aligned quadruple patterning (SAQP) backed with 193 nm immersion lithography or more advanced extreme ultraviolet (EUV) patterning. As the scaling continues, the GAA FETs, which can offer maximized gate-channel capacitive coupling and higher current per footprint by stacking multiple NW/NS vertically, will be the next-generation device structure beyond Fin-FET at Node 3 nm. To further scale the standard cells composed of NMOS and PMOS, the spacing between different type of FETs need to be reduced. Thus, the fork-sheets structure is proposed with only a narrow dielectric wall in between to separate them. Beyond that, the CFET where NMOS and PMOS are stacked on top of each other, instead of positioning

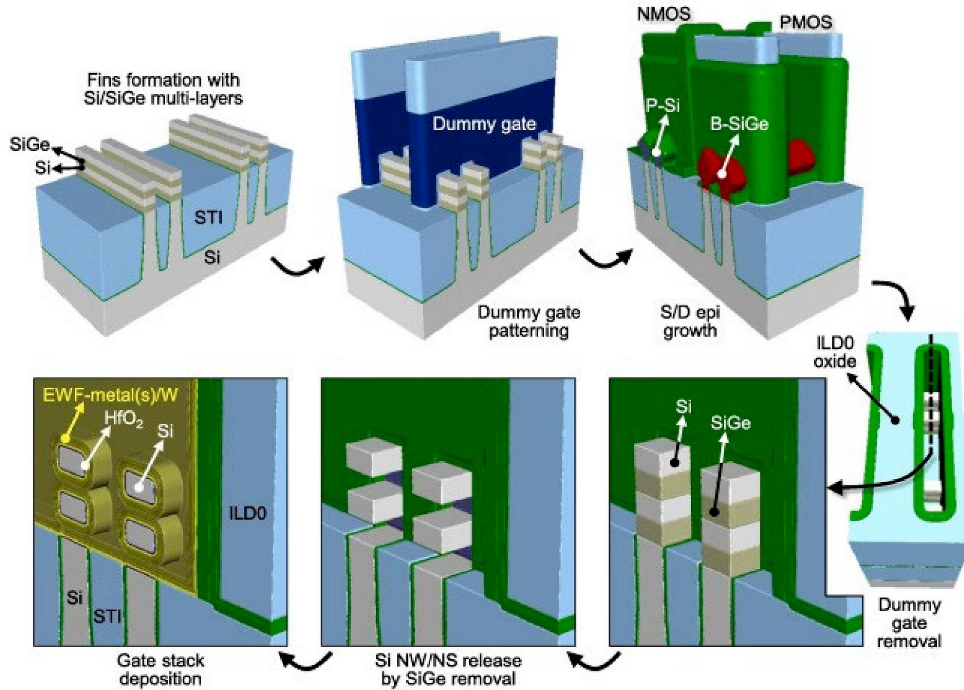

Figure 3 (Color online) Key steps for the fabrication of vertically stacked lateral Si nanowires or nanosheets on bulk Si substrates [11] Copyright 2020 Elsevier.

them side-by-side, can dramatically decrease the cell footprint by half, offering the preferable architecture <N2 nm. The innovation for device structure may prolong to a vertical FET, directly addressing the fundamental scaling constraints for the lateral device by decoupling gate length from the layout footprint. Figure 2(a) illustrates the evolution of transistor architecture from planar to 3D vertical.

However, the scaling merely on a single transistor/cell level will quickly run into the limit when the physical dimension reaches a few nanometers [65]. The conventional von Neumann computing systems have separate processor and memory units, leading to significant latency and energy expenses associated with the transmission of large amounts of data between the units [66]. On the other hand, non-von Neumann architectures that merge processor and memory unit into one single unit, such as in-memory-computing and neuromorphic computing, can greatly reduce the data transfer time and energy consumption by implementing massive parallel computations [67]. Luckily, there is plenty of space remaining to be exploited in the third dimension. By building up the functional layers layer-by-layer on the same substrate, the M3D structure will boost the integration density enormously [68], as seen in Figure 2(b). Moreover, M3D technology is also beneficial for constructing a non-von Neumann system, by vertically stacking memory units on top of logic layers to implement the in-memory-computing architecture [69]. Even though the performance of logical processors is greatly improved by taking the advantage of transistor scaling, the speed of memory trails badly [61, 68], resulting in wasting a lot of time on data transmission. This phenomenon, also known as "memory wall" [67], becomes more severe with the increasing computing demand for data-intensive applications such as big data and artificial intelligence. By using dense interconnections between the bottom logic layer and the top memory layer, a massive amount of data can directly and parallelly transfer to each respective underlying logic unit and process in situ [67], solving the memory wall issue (Figure 2(c)). Besides, the M3D structure can further develop its potential by integrating synapse devices on the top layer, forming a high-density and complex 3D network between memory units and process units just like the human brain [66, 70]. This neuromorphic computing architecture [71] offers an alternative method to increase computing power.

To gain more insight into the advanced FET structure, an exemplary fabrication procedure of GAA FET on Si substrate via the top-down selective etching of stacked Si/SiGe multi-layers is described in Figure 3, where (1) first, multi-layers of stacked Si/SiGe were epitaxially grown on the bulk Si substrate, followed by forming fin structures by patterning and etching into the multilayers. (2) Then, the SiO_2/poly-Si dummy gates and nitride spacer were defined before epitaxy growing doped Si layer for NMOS and SiGe layer for PMOS in the source-drain regions. (3) The dummy gate was removed, followed by the

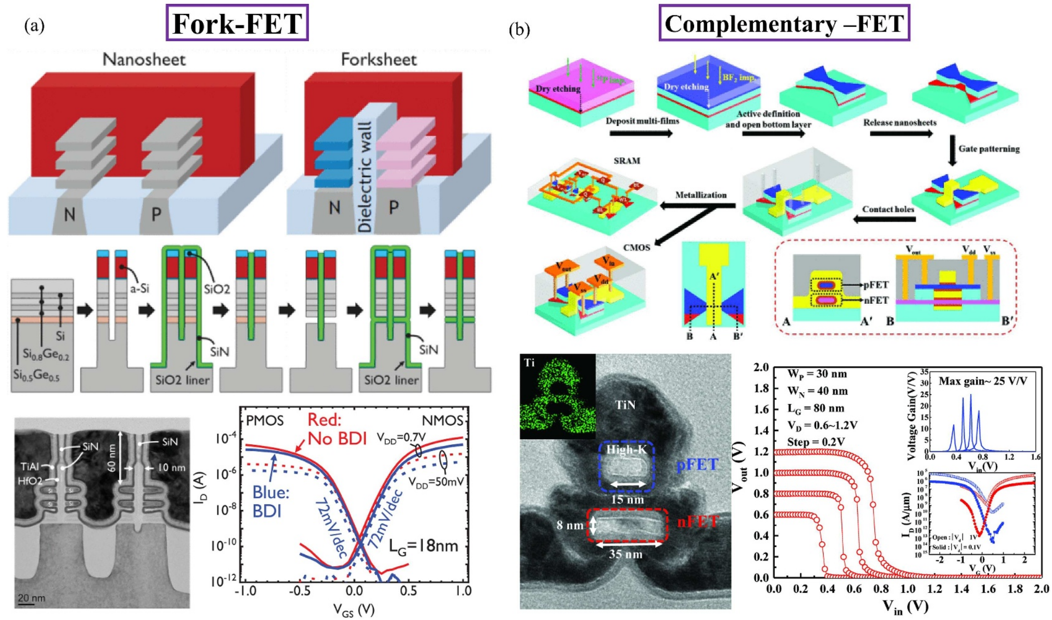

Figure 4 (Color online) Advanced transistor device architectures. (a) Schematics of Fork-FET device structure and fabrication process quoted from Figures 1 and 3 in [73] Copyright 2022 IEEE; (b) schematics of the CFET device structure and fabrication process quoted from Figures 2 and 3 in [74] Copyright 2019 IEEE.

suspension of SiNWs via selectively etching off the sacrificial Ge-rich interlayers using vapor HCl or CF_4. In this structure, the height of the Si layers should be low enough to suppress the short channel effect and the number of the stacked Si layers, i.e., the number of suspended SiNWs, must be sufficient to carry a high enough drive current. (4) On the other hand, the heights of the SiGe layers need to leave adequate room for inserting dielectric and gate layers to accomplish a beneficial GAA configuration. (5) Finally, the high-k dielectric layer and work functional metal (WFM) were deposited. Despite the successful demonstration of highperformance stacked NW GAA FETs, the need for epitaxial growth of Si and SiGe sublayers leads to increased fabrication cost and process complexity, while great care must be taken to minimize the accumulation of lattice mismatch strain and avoid the intermixing of Ge and Si during high temperature steps. On the other hand, stacked SiNWs can also be produced via low cost and high yield self-assembly approaches, which will be introduced in Section 5.

Though the GAA structure offers the strongest electrostatic gate control for further gate-length reduction, the large space between NMOS and PMOS limits the overall scaling of standard cells. Fork-sheets devices that derive from GAA structure, on the other hand, can provide more aggressive scaling by separating them only with a slim dielectric wall [72]. Moreover, this physical isolation will simplify work function metal (WFM) fill during the replacement metal gate (RMG) process. Using the bottom dielectric layer to isolate FETs from the substrate, instead of doping the ground plane with opposite polarity on either side, the width of the wall can be decreased to 10 nm, as seen in Figure 4(a) [73]. Beyond that, the CFET configuration which stacks NMOS/PMOS can further reduce the layout area, making it an excellent candidate for <N2 nm. This specific device structure can minimize the standard cell area by directly eliminating the N-P space. Besides, different channel materials can be introduced to NMOS and PMOS for higher hole/electron mobility. Chang et al. [74] first demonstrated the CMOS inverters and 6T-SRAM cells based on CFETs (Figure 4(b)). The fabrication processes were implemented at a low temperature (< 600°C), which is compatible with the M3D. This compact CFET inverter can also provide lower parasitic capacitance than standard CMOS because of the overlapping of gate fringe electric field line paths. Both fork-FET and CFETs will have the potential to enable denser, better performing circuits and realize more functionality including the M3D and von Neumann architecture.

Recently, GAA FETs with junctionless (JL) configuration have emerged as preferable candidates for synapses in neuromorphic computation due to the fabrication simplicity and robustness to drain-induced barrier lowering (DIBL) [21]. The improvement of on-state current will enable to derive more synapses and higher integration density without sacrificing the footprint area, As depicted in Figure 5(a), Han et al. [75] have demonstrated that a JL-neuron can reduce the current leakage and prefer to drive many synapses

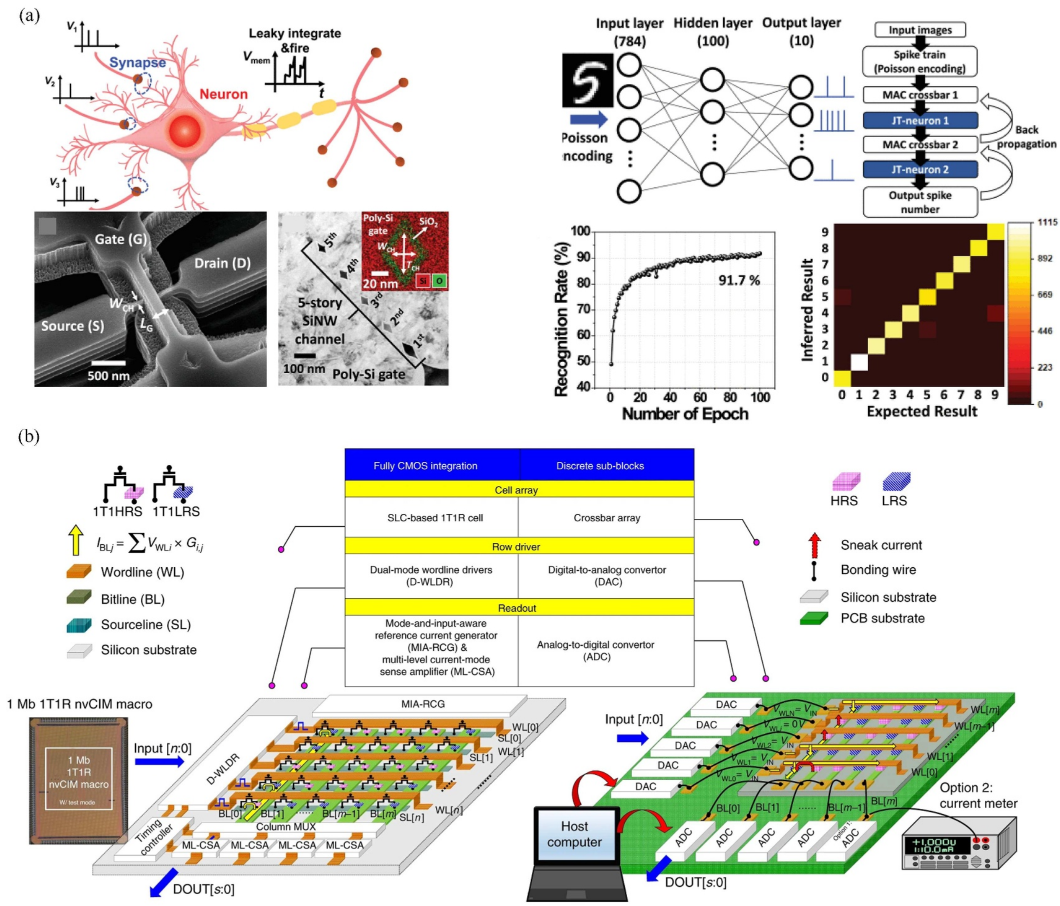

Figure 5 (Color online) Non-von Neumann paradigms based on the SiNWs with top-down etching. (a) Vertically stacked multiple nanowires for neuromorphic hardware quoted from Figures 1 and 6 in [75] Copyright 2022 IEEE; (b) CMOS-integrated non-volatile computing-in-memory macro [76] Copyright 2019 Springer Nature.

with high speed. The JL nature without abrupt source-drain (S/D) junctions is beneficial to decrease the manufacturing cost with simplified processes for M3D device structure. The gate voltage can manipulate the neuron activation and inhibition to realize the neuronal function learning efficiency. Apart from the neuromorphic computation built on the top-down etching method, non-volatile in-memory-computing could improve the energy efficiency of edge devices and overcome the memory wall for artificial intelligence applications beyond von Neumann architecture [66]. A fully integrated memristive non-volatile computing-in-memory structure can provide low latency for Boolean logic and multiply-and-accumulate (MAC) operations relying on the TMSC standard CMOS process in Figure 5(b) [76]. This novel architecture will avoid the long latency in the movement of data across multilayer memory hierarchies, reduce the amount of intermediate data, and shorten the latency of multiple logic or MAC operations. In addition, a memory cell array fully integrated with peripheral read/write circuits on the same chip will accelerate the computing speed and strengthen the energy efficiency.

Due to the advantages of the top-down etching method and more functional device modules, it is feasible to realize the bottom FEOL transistors and vertical interconnect for M3D via micro-nano fabrication technologies on the wafer. The sophisticated lithography-based top-down fabrication strategy still represents basic technology for silicon microelectronics, while entering the single digit nanometer regime approaches to fundamental and economic limitations. In addition, the high-temperature process and the requirement for silicon substrate as a starting layer make it unsuitable for fabricating top BEOL transistors. On the other hand, it is apparent that a bottom-up assembly strategy which can obtain nanoscale building blocks at a low temperature, could be appropriate to explore BEOL applications. It will complement the conventional top-down-based silicon microelectronics with extraordinary attributes and fancy functions.

3 Bottom-up catalytic growth strategy

In strong contrast to the subtractive top-down etching of c-Si wafer to produce ultrathin c-Si channels, crystalline c-Si nanostructures can be readily formed via a nanoscale additive catalytic growth, where the constituent atoms are sequentially piled up, in a layer-by-layer manner, at the precipitating interface joining the nanocrystal solid and the molten metal catalyst droplets oversaturated Si atoms [52, 54, 77, 78]. In this so-called bottom-up fabrication approach, the precursor sources can be gaseous molecules, such as in the VLS growth [50, 51, 79], amorphous thin films, as found in the solid-liquid-solid (SLS) mechanisms [80–83].

One of the most attractive features of the catalytic growth, in view of nanoscale channel fabrication, is the unidirectional 1D growth of high-quality crystalline semiconductors, led by tiny catalyst droplets, which can happen at a rather low temperature (Low-T), typically <500°C, enabled by the relatively lower eutectic point of metal-Si alloy [84, 85] or by using low-melting point metal as catalyst [86, 87]. In other words, these liquid catalyst droplets provide a soft template to confine and determine the diameters of the as-growth SiNWs, which can be easily scaled down to tens nm or <10 nm, by choosing the discrete metal particle deposited on substrate surfaces [51, 53, 55, 80] or colloid metallic particles with very well controlled size and geometry [52, 54, 58].

Apparently, if this extremely high-yield catalytic growth can be tamed and precisely controlled to produce orderly ultrathin c-Si channels on the planar surface, it will help to exempt the use of the sophisticated and expensive lithography technologies, particularly for the latest <N22 nm nodes. More importantly, this low-T growth of crystalline Si channel structures is exactly what is needed for the fabrication of the stacked CMOS logics in the implementation of M3D architecture; see the right technology route in Figure 1. Of course, to make all these happen, a prerequisite is to establish a reliable and scalable technology to achieve a precise location, orientation, and geometry control of these synthetic SiNWs building blocks, which is, unfortunately, still a formidable challenge or a bottleneck for most of the catalytic growth strategies to establish as a reliable integration technology. Nevertheless, much exciting progress in these aspects has been made in the past two decades, and in this section, we will first focus on the recent research efforts devoted to the VLS-grown SiNWs and the emerging assembly technologies aimed at deploying them as orderly channels for microelectronics on planar substrates.

3.1 Vapor-liquid-solid growth mechanism

As the most famous and best investigated catalytic growth mechanism, the VLS growth phenomenon was first reported as a detrimental phenomenon in the annealing step of Si processing, where the metallic impurities were found to catalyze a 1D growth of slim and long c-Si nanowhiskers that could bridge and short-circuit the neighboring units [88]. Later in the 1990s, this VLS growth of 1D SiNWs started to draw considerable and increasing research interests, as it offered a new convenient way to batch manufacture ultrathin c-SiNWs with much exotic transport, optoelectronic, and mechanical properties, arising in part from the unique high aspect-ratio geometry and significant size confinement effects within the tightly confined 1D channels [50, 52, 55, 57, 77, 79, 80].

As depicted in Figure 6(a), a typical VLS growth starts from the incorporation of Si atoms into a metallic catalyst nanoparticle or cluster, where the SiH4 or other gas precursor molecules arriving at the particle surface are dissociated, with the aid of surface metal catalytic effect [53, 88] or plasma assisted bond-breaking mechanism [51, 89], and absorbed to establish a supersaturation status within the catalyst particles. Note that the metal-Si alloy formation usually leads to a binary system with a eutectic point much lower than the melting points of the pure constituent elements. Take for example the phase diagram of Au-Si alloy system presented in Figure 6(a), which shows that the Au particles dissolve with ∼24% Si atoms melt at only 363 K, much lower compared with the melting temperatures of 1064 and 1414 K for Au and Si, respectively. So, the Au particles will quickly melt into liquid droplets upon the absorption of Si atoms even at a rather low temperature (say <400°C). With the continuous adding of more Si atoms, the status of the Si-loaded Au droplet is gradually shifted into an oversaturated mix phase regime, with coexisting liquid and solid phases as marked in the dark grey region, where c-Si seed is continuously precipitated. As the precipitation or deposition of c-Si only happens at the touching interface between c-Si seed and Au droplet, an 1D growth kicks off with a diameter roughly equal to the size of the leading metal particle (Figure 6(a)).

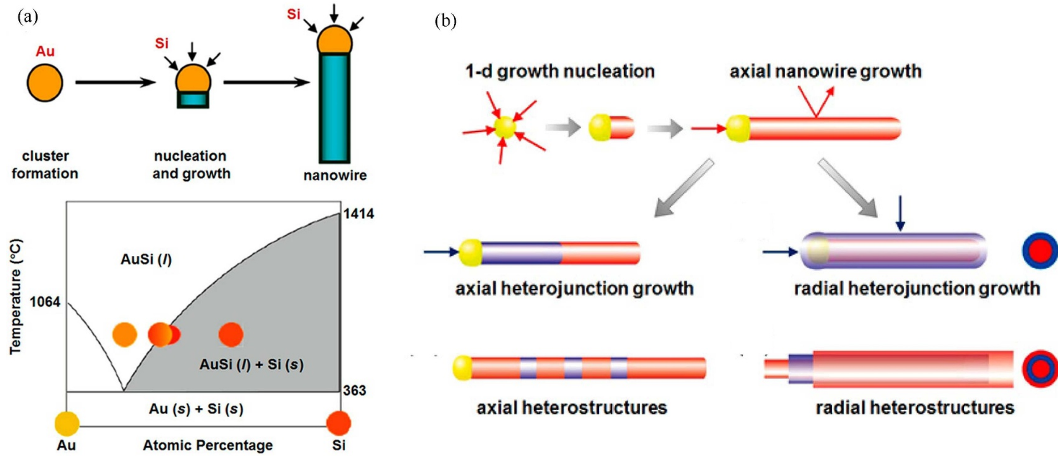

Figure 6 (Color online) Vapor-liquid-solid (VLS) growth mode. (a) Schematic illustration of the VLS growth mechanism [53] Copyright 2006 Institute of Physics; (b) schematic illustration of NWs heterostructures growth [94] Copyright 2004 The Royal Society.

So far, the thinnest diameter of the VLS-grown SiNWs is d_{nw} ≈5 nm, catalyzed by using Au particles [90], which were found to be monocrystalline with typical growth orientations of Si⟨110⟩ for those with diameter <10 nm [91–93], while the thicker ones were usually found to grow along Si⟨111⟩. There are many control parameters that could influence the growth orientation of the VLS SiNWs, such as surface passivation, catalyst metal, growth temperature, and the choice of different precursor gases. So, it is feasible, at least in principle, to control the crystallographic orientations of the catalytic growth of SiNWs into the preferred ones for the p- or n-type channels in FETs. The interested readers are referred to more systematic readings in [50, 53, 58, 80]. Besides the excellent diameter control, more complex, and potentially more functional, 1D superstructure can be constructed during the VLS growth (Figure 6(b) [94]). For example, the SiNW core can be coated with a shell layer with different doping types to form radial p-i-n junction, or distinct composition, like Si-core and Ge-shell or vice versa, to form Type-II heterojunction that has proven to be beneficial for high hole mobility electronics [53, 58, 79, 95, 96]. In addition, axial doping, and composition modulation of the 1D NWs are also possible during the VLS growth, as the feeding gas species can be altered periodically and sequentially in a programmable way.

Despite all these advantages of the catalytic VLS growth approach, there is still one critical challenge that has been hindering a precise integration of these bottom-up 1D building blocks to serve as scalable channel materials for FETs. The reason is apparent considering the fact that the VLS growth is fed with gaseous precursors, and thus tends to grow into a standing random matrix, like the grasses grown in nature, if there is no other direction control imposed from the bottom substrate or overhead. Unfortunately, this vertical morphology is incompatible with the mainstream planar electronic architecture, which demands exact control over each SiNW channel in a precise location with predesigned alignment. Therefore, first, these VLS-grown SiNWs must be collected, transferred, and re-arranged onto planar substrates, to be useful for practical electronic applications.

3.2 Planar integration of VLS-grown SiNWs

In order to enforce a planar growth of SiNWs, the most straightforward way is to confine them within narrow tunnels, formed for example by capping layers, while leaving open ends to allow for precursor gas to permeate in. As shown in Figure 7(a) and [97], a short segment of Au catalyst was embedded within the capping layer, which then catalyzes the growth of SiNWs extending out of the two open ends. In this way, a preferential growth orientation is set for the following VLS growth of the crystalline SiNWs. Though a very well controlled planar growth of SiNWs has been accomplished within the fully confined tunnels, there is still a considerable chance for the extended SiNWs to grow into tilted or deviated directions. Later on, Pevzner et al. [98] reported a more deterministic and programmable fully confined growth of VLS SiNWs with narrow trenches of basically arbitrary line-shapes, as seen in Figure 7(b), where it was experimentally verified that the VLS growth can really proceed continuously within the ultralong trenches. However, caution must be taken to avoid the use of too long guiding trench, as the gas feeding to the catalyst droplets, sitting at the deep ends of the fully capped guiding tracks, becomes inefficient

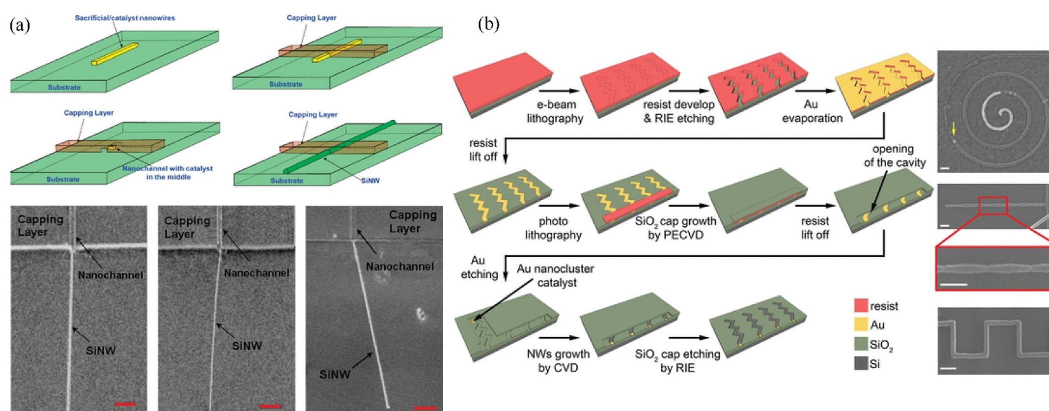

Figure 7 (Color online) Surface-confined VLS growth of SiNWs. (a) Schematic illustration of planar VLS growth directed by nanochannels [97] Copyright 2008 American Chemical Society; (b) schematic illustration of planar VLS growth with the shape-guided method [98] Copyright 2012 American Chemical Society.

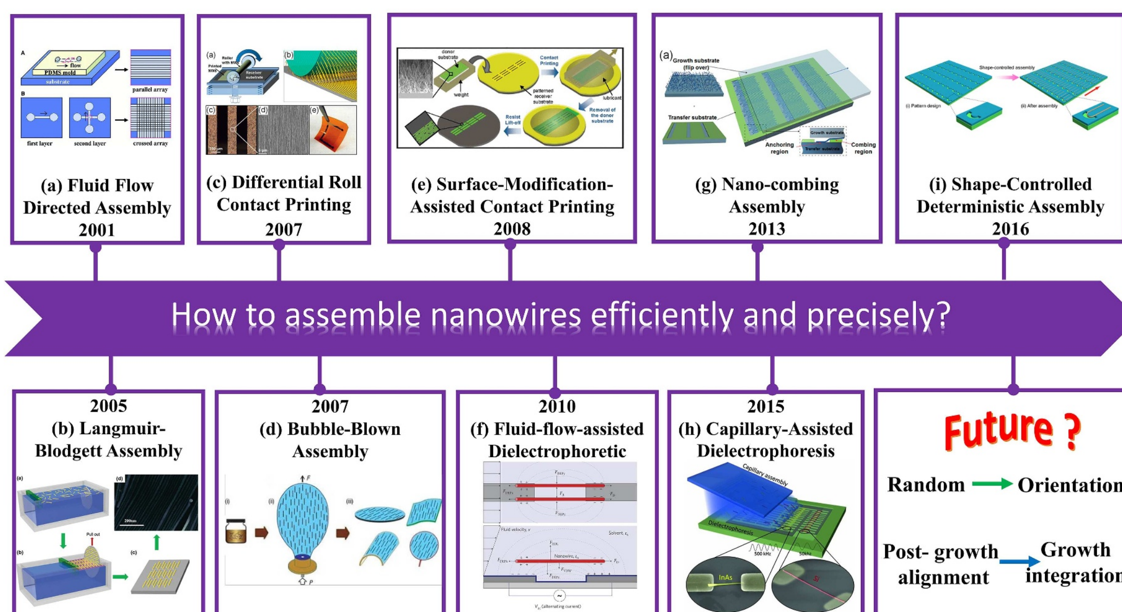

Figure 8 (Color online) Hierarchical assembly of nanowires. (a) Fluid flow directed assembly [95] Copyright 2001 American Association for the Advancement of Science; (b) Langmuir-Blodgett assembly [101] Copyright 2005 American Chemical Society Copyright, [99] 2012 American Chemical Society; (c) differential roll contact printing [102] Copyright 2007 American Institute of Physics; (d) bubble-blown assembly [103] Copyright 2007 Springer Nature; (e) surface-modification-assisted contact printing [104] Copyright 2008 American Chemical Society; (f) fluid-flow-assisted dielectrophoretic-assembly [105] Copyright 2010 Springer Nature; (g) Nano-combing assembly [106] Copyright 2013 Springer Nature; (h) capillary-assisted dielectrophoresis assembly [107] Copyright 2015 John Wiley and Sons; (i) shape-controlled deterministic assembly [108] Copyright 2016 American Chemical Society.

with the increase of trench length. On the other hand, the fabrication of such delicate fully confined tunnels or trenches must be accomplished by using sophisticated electron beam lithography (EBL), while the crystalline quality, growth orientation, and uniformity of these fully confined VLS SiNWs still need to be better understood for scalable device applications.

Considering the difficulty of enforcing a planar growth of VLS SiNWs, more research efforts have been directed to a collect-and-assemble strategy. The key benefit of this approach is that the VLS growth can be carried out first in an open vapor environment upon parent substrates that can sustain a high processing temperature, which is favorable to producing high-quality monocrystalline Si or other NWs, with relatively uniform diameters and lengths, as well as in much higher throughput. After that, these as-grown SiNW forests can be collected from the parent substrates and dispersed into solvents, which then can be spin-coated or dripped onto the target substrate [50, 80, 99, 100]. As summarized in Figure 8 [95, 99, 101–108], a series of techniques have been developed to re-arrange these VLS-grown

NWs into orderly arrays and assemble them onto planar substrate surfaces, which include, for example, a fluid flow directed assembly approach to enforce the NWs to align in a parallel array along specific orientation [95], which can also be repeated sequentially for two times, but in orthogonal directions, to form crossed NWs arrays, or a Langmuir-Blodgett (LB) technique [101], a differential roll printing [102], and a bubble-blown film assembly [103].

In addition, the SiNWs can also be transferred directly onto a solid substrate surface via a surface-modification-assisted contact printing process [104], where during a contacted sliding of the NWs-grown substrate over the receiver substrate, the NWs will break and attach onto the receiver surface with basically the same orientation. Based on the contact assembly, nano-combing and sharped-controlled assembly could organize the NWs with controlled position and geometry as well [106, 108]. Furthermore, the electric-field-assisted assembly of NWs makes a promising approach to manipulate nanowires precisely under the control of dielectrophoretic force [105, 107]. The interested readers are referred to more systematic readings in the relevant literature [50, 80, 99, 100].

Based on the transfer-and-place approach, prototype FET logics [50, 54, 57, 80, 109, 110] and sensors [55, 56, 59, 60, 77, 111] have been successfully demonstrated based on the VLS-grown SiNWs, with rather impressive performances thanks to the high crystalline quality and miniaturized diameter of the ultrathin SiNWs channels. For example, as presented in Figure 9(a), the diameter of Ge NWs of 14.6 nm thick, with an epitaxy 1.7 nm Si shells has been utilized as heterojunction 1D channels. Interestingly, the type-II band profile alignment enables a confined accumulation of holes into the c-Ge core, which can help to achieve a rather high hole carrier mobility with minimized influence from the surface scattering [112]. More importantly, the high-quality crystalline NW channels produced by catalytic-growth can be directly placed upon flexible polymer substrates, such as PI or even PDMS (see Figure 9(b)) [113], which are usually excluded from being reliable materials for high temperature processing. It is also possible to repeat this transfer process several times to produce stacked multilayer electronics. However, it is also noteworthy that, in each layer of the stacked NWs electronics, thousands of parallel NWs must be used together as the semiconductor channels, with only controlled orientations but without pre-known starting or ending places. So, this NWs assembly technology could find applications in large area printed electronics or sensors, where the integration density of the FET or TFT units is not a demanding issue, but apparently not a suitable choice for the construction of high-density microelectronic integration in planar or 3D architecture.

Though all the above-mentioned transfer-and-place approaches have accomplished a successful ordering control of the transferred SiNWs to some extent, most of them resort to intricate fluidic solution processing and stochastic mechanical transferring, which are difficult to apply for, or be compatible with, the high-precision fabrication procedure of integrated electronics. A fundamental obstacle arises from the difficulty of achieving a high-precision transfer of these tiny NWs building blocks, which were grown via VLS mechanism as a standing 3D matrix, but need to be deployed and integrated into the mainstream planar/2D electronic architecture. This dilemma leads us to wonder whether there exists a more straightforward catalyst growth approach, which is more suitable for batch-producing orderly planar SiNWs for reliable integration

4 In-plane solid-liquid-solid (IPSLS) growth of planar SiNWs

Actually, the gaseous precursor is not the only choice for catalytic growth of SiNWs; there are plenty of other choices, such as the oxide-assisted growth (OAG) [114], solid-liquid-solid (SLS) [83, 115], and solution-liquid-solid [78] modes. However, in view of seeking a planar growth of SiNWs on the substrate surface, most of the OAG and SLS growth modes encounter the same challenge as in the VLS growth mode, that is the as-grown SiNWs are difficult to assemble and manipulate. Fortunately, a relatively new in-plane solid-liquid-solid (IPSLS) growth phenomenon has been discovered by Yu in 2009 [82, 83, 116], where a thin film hydrogenated amorphous silicon (a-Si:H) has been taken as the precursor layer that can be easily deposited via conventional plasma enhanced chemical vapor deposition (PECVD) technique, at rather a low temperature, even at room temperature (RT) and over large area substrate. Importantly, they used a group of low-melting-point metals as catalysts, including indium (In), tin (Sn), bismuth (Bi), and gallium (Ga), which enable an easy activation of the molten catalyst droplets at rather low temperature to produce SiNWs. Of course, now as depicted in Figure 10(a), the as-grown SiNWs can be very well confined to grow only on the a-Si:H coated surface, exempting thus the most challenging

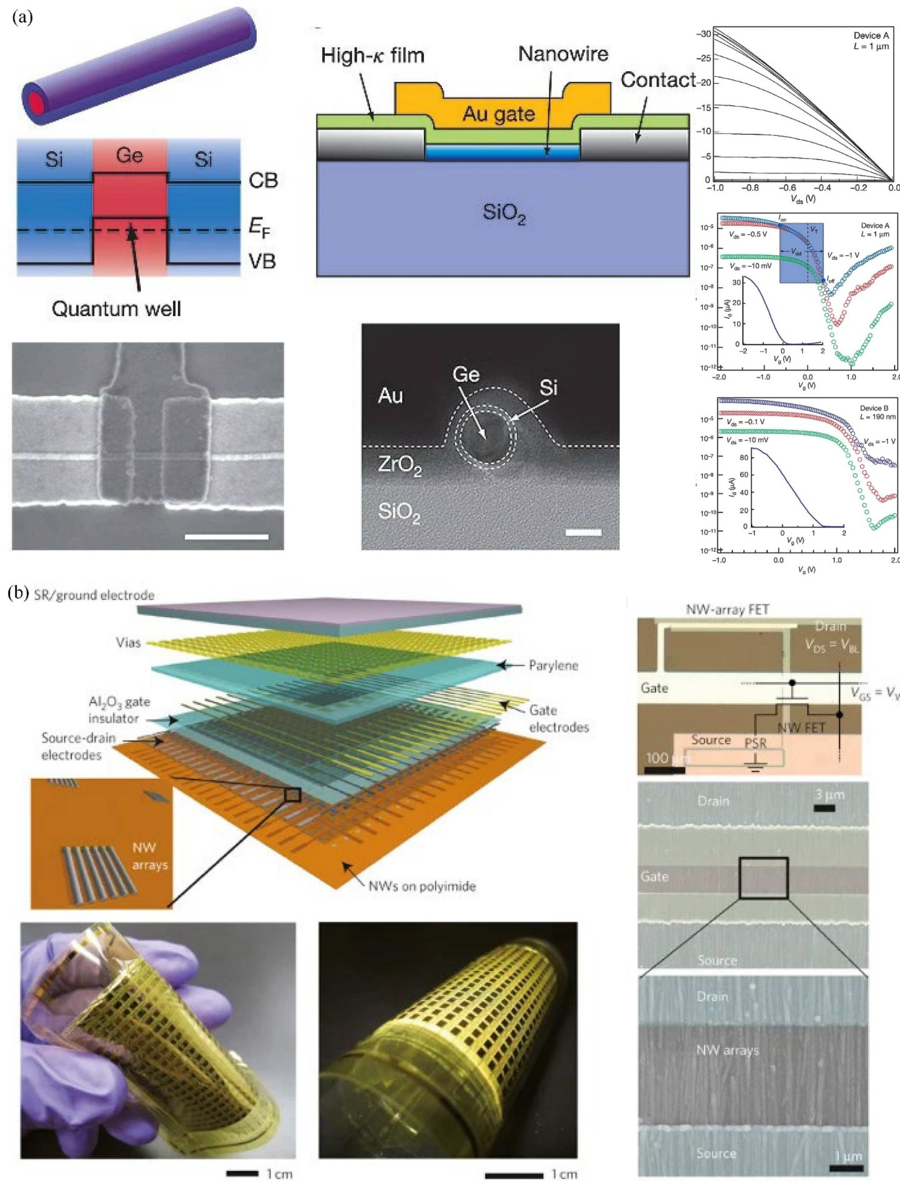

Figure 9 (Color online) Devices and integration applications based on the SiNWs with the VLS growth mode. (a) Ge/SiNWs heterostructures as FETs [112] Copyright 2006 Springer Nature. Scale bar 500 nm in SEM; Scale bar 10 nm in TEM. (b) NWs-based macroscale flexible devices [113] Copyright 2010 Springer Nature.

pick-and-transfer procedure as required for the catalytic VLS-grown SiNWs.

4.1 IPSLS growth mechanism

The major fabrication steps of the IPSLS SiNWs, taking the In-catalyzed SiNWs growth illustrated in Figure 10(a) as an example, include (i) a plasma treatment of In or ITO stripes to form discrete In droplets at a temperature above the melting point of In ($T_{\mathrm{In}} = 169°\mathrm{C}$) (say 250°C–300°C), followed by (ii) the deposition of a thin layer of a-Si:H at a lower temperature of 150°C, which is below the melting point of In. So, the In droplets were frozen into inactive solid status during the a-Si:H coating. After that, the samples were annealed at a typical temperature of 200°C–300°C in vacuum or in inert or H_2 ambient, during which the In droplets became molten again, starting to absorb a-Si:H medium at the front In/a-Si:H interface and precipitate crystalline SiNWs at the rear SiNWs/In interface.

During an IPSLS process, the fundamental driving force arises from the different Gibbs energies of Si atoms in crystalline or amorphous phases; that is roughly $\Delta E_{ac} = E_a - E_c \approx 0.12$ eV, for the typical hydrogenated a-Si:H thin film, but also tunable by altering PECVD deposition conditions [82,116]. So, at

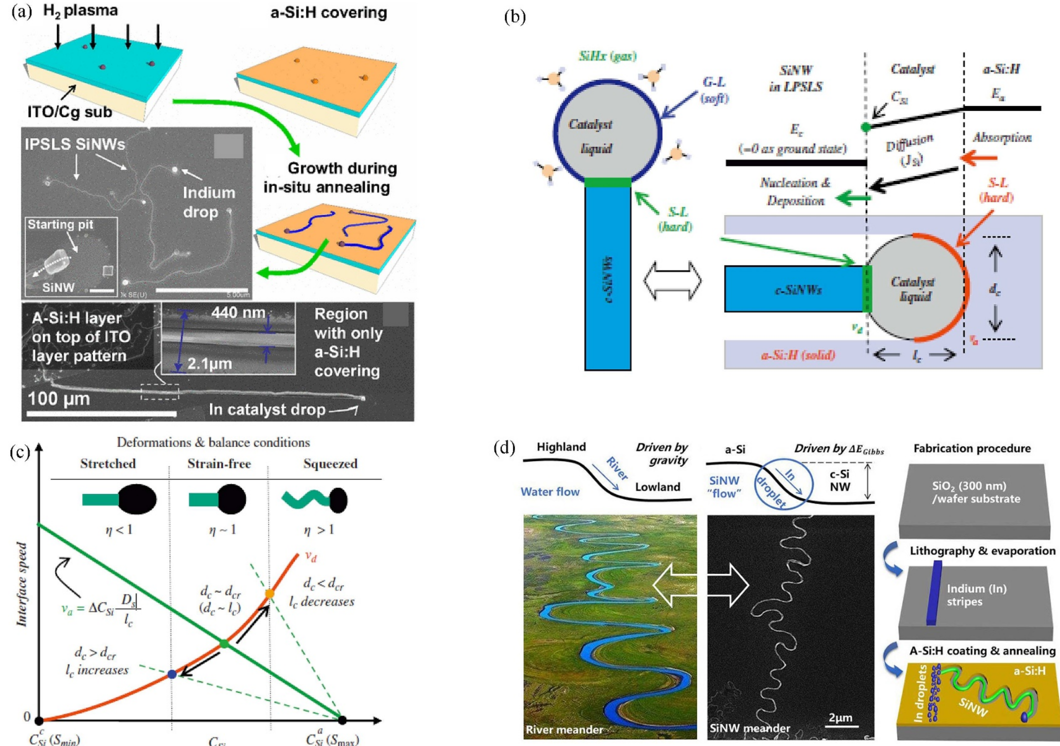

Figure 10 (Color online) In-plane Solid-Liquid-Solid growth mode. (a) Schematic illustration of the IPSLS growth of SiNWs [82] Copyright 2010, American Physical Society; (b) schematic illustrations of absorption and deposition interfaces in VLS mode and IPSLS mode [81] Copyright 2012 Elsevier; (c) typical SiNWs produced under different growth balance conditions [81] Copyright 2012 Elsevier; (d) self-oscillating growth of SiNWs springs [117] Copyright 2019 American Institute of Physics.

the front a-Si:H/In absorption interface, the local equilibrium Si concentration C^a_{eq}, is indeed higher than that at the rear c-SiNWs/In interface, by $C^a_{\text{eq}} = C^c_{\text{eq}} \mathrm{e}^{\Delta E_{ac}/kT}$. Therefore, a diffusion flux of the absorbed Si atoms will be established, within the tiny In liquid droplet, to sustain the continuous precipitation of c-SiNWs at the rear deposition interface [81]. When this diffusion happens, the Si concentration at the front absorption interface becomes undersaturated, which encourages the intake of more Si atoms from the contact a-Si:H medium. At the same time, the Si concentration at the rear deposition interface, defined as C_{Si}, becomes oversaturated with

$$S = C_{\text{Si}}/C^c_{\text{eq}} \leqslant C^a_{\text{eq}}/C^c_{\text{eq}} = \mathrm{e}^{\Delta E_{ac}/KT}, \tag{1}$$

which drives constant precipitation or growth of c-SiNWs along the moving course of the leading catalyst droplet.

Though sharing many common features with the catalytic VLS mechanism, such as basically the same diameter control of the as-grown SiNWs being proportional to the size of catalyst droplet with $D_{nw} \sim D_c$, a similar precursor atoms transport within the droplet, the IPSLS growth mechanism has several key aspects that are very much different, compared with the gas-feeding VLS growth process. As summarized in Figure 10(b), the catalyst droplet during IPSLS growth has two hard solid/liquid interfaces, with respect to the soft top gas/liquid interface in VLS growth, which can thus impose a strong force on the liquid droplet sandwiched in between. For example, if the front absorption interface tends to move faster (slower) than the rear deposition interface, usually happening with a relatively thinner (thicker) a-Si:H film supply, the In droplet will be stretched (squeezed) by the two interfaces to become longer but narrower (shorter but wider). Consequently, the diameter of the as-grown SiNW will also change, as it is always proportional to the width of the catalyst droplet. More interestingly, for the squeezed situation, the droplet can be forced to periodically change its growth orientation producing SiNWs of regular zigzag or meandering shapes, as seen in Figures 10(c) and (d) [81,117]; while in the opposite case, a strong pulling force will trigger another kind of repeated Plateau-Rayleigh oscillation of the leading droplets, resulting in the formation of island-chain SiNWs [118]. All these phenomena highlight the fact that, for the IPSLS growth, the growth balance condition, between the front absorption and the rear

deposition, is a key growth control parameter that can be explored to achieve or tailor the desired SiNWs geometries. Though an in-depth discussion of the growth dynamics of IPSLS SiNWs goes beyond the scale of this brief review, it is noteworthy that this growth balance condition can be conveniently tuned by a dimensionless ratio factor of

$$\eta = t_{\mathrm{aSi}}/D_c \tag{2}$$

where t_{aSi} and D_c are the a-Si:H layer thickness and the size of the catalyst droplet, respectively. This can be roughly understood from the mass-conservation argument that the effective front absorption interface area is proportional to $\sim t_{\mathrm{aSi}}\ /D_c$, while that at the rear deposition interface is to $\sim D_c^2$. So, the ratio of η is a simple reflection of the front Si atom supply over the rear outgoing flux. In short, for an $\eta \gg 1$, the supply of a-Si:H is more than enough, to guarantee a continuous SiNWs growth, and thus stimulates a squeezing dynamic of the droplet and a zigzag growth of SiNWs [81]. Also, for the $\eta < 1$, a stretching pull on the droplet will produce straight ones, or even island-chain structures to the extreme cases [81, 118]. More theoretical and experimental details of the self-automated geometry evolution of the IPSLS NWs are available in [80, 81, 118].

4.2 Directional guided growth of planar SiNWs

In order to control the growth direction of the IPSLS SiNWs, there are two feasible strategies, that is either by using a crystalline substrate that provides an epitaxial interface to guide the growth of SiNWs to follow crystallography orientations [119], or by using simple surface patterns, such as step edges to capture and lead the surface-rolling droplet to produce SiNWs in desired locations [120]. Actually, these two strategies are based on the advantage that the IPSLS SiNWs are confined to the ground surface by the a-Si:H coating layer, which is totally absent in VLS or other catalytic growth mechanisms. For the epitaxial guided growth, as shown in Figure 11(a), c-Si[100] wafer substrate was first used as homo-epitaxy substrate, which provides perfect lattice matching and regular orientation guidance of SiNWs to grow into rectangular routines along Si$\langle 110\rangle$ directions, without the use of any surface patterns or guiding features [119]. After that, planar hetero-epitaxial growth of SiNWs was also successfully demonstrated upon the R-plane sapphire substrate, which exposes a similar atom lattice to that of Si[100] surface [121]. The effective epitaxial guidance is realized by introducing a competing bottom nucleation interface, upon the crystalline substrate surface, which lies closer to the absorption interface than the rear deposition interface at the end of SiNWs, as depicted schematically in Figure 11(b). Therefore, a series of discrete pyramids of c-Si seeds were first formed on the epitaxial interface, with preferential orientations determined by substrate symmetry. Then, these pyramid seeds gradually expand, within the droplets, and merge into continuous SiNWs. While this epitaxial growth represents almost the simplest way to achieve an aligned arrangement of planar SiNWs, it is only applicable to specific crystalline wafer substrate with clean epitaxial surfaces, which is not always guaranteed for Si[100] surface as it is easy to be oxidized. For the more stable and insulating R-plane sapphire substrate, the challenge is to address the accumulation of small, but still significant, lattice mismatch strain, which could detrimentally impact the epitaxial guided growth. More importantly, the implementation of these epitaxial guided growth in monolithic 3D architecture seems to be even more difficult, considering the lack of crystalline wafer in the stacked layer.

The guided IPSLS growth can also be accomplished by using simple surface patterns. Thanks to the conformal coating of a-Si:H precursor layer over the sample surface, the extra a-Si:H supply coated on the vertical sidewall of a single-sided step edge can effectively attract the running catalyst droplet, as diagrammed in Figure 11(d) for different contact configurations, to move and produce SiNWs along the edge lines [122]. In contrast to the epitaxial growth, which can only grow straight SiNWs along specific crystallographic orientations, this step-guided growth is far more flexible or powerful to enforce the planar SiNWs to grow into arbitrary pre-designed routes, such as sinusoid wavy shape that endows excellent elasticity to the SiNWs springs [123]. Importantly, this step-guided growth of SiNWs channels can be carried out upon large area amorphous substrate, and the formation of single-sided guiding step edges, by itself, requires no high-resolution lithography. All these features are highly valuable for the fabrication of large area electronics, flexible sensors, and displays [80, 124–127]. In view of 3D monolithic integration, the single-step-guided IPSLS growth represents arguably the first catalytic growth technique that could be implemented for scalable integration of ultrathin SiNWs channels, without the need for pre-existing wafer substrate, which is a key capability for the building of stacked CMOS logics in 3D architecture.

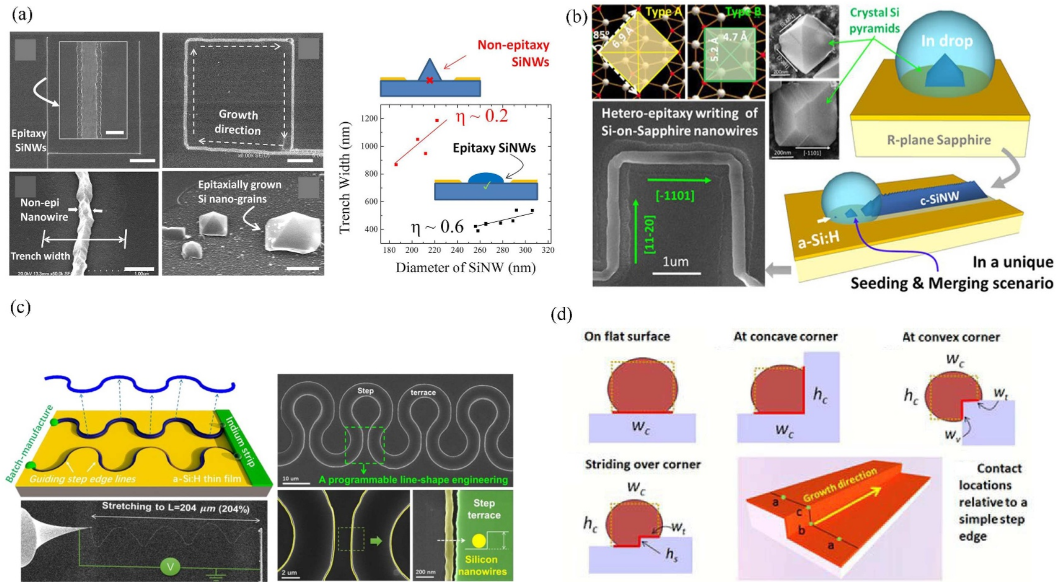

Figure 11 (Color online) Guided growth of planar SiNWs. (a) In-plane epitaxial growth on silicon substrate [119] Copyright 2014 American Chemical Society; (b) heteroepitaxial growth on sapphire [121] Copyright 2016 American Chemical Society; (c) SiNWs springs guided by step edges [123] Copyright 2017 American Chemical Society; (d) schematic illustration representative of steps guiding [122] Copyright 2015 Royal Society of Chemistry.

4.3 Low temperature catalytic growth

As an important promise of the catalytic growth approach, ultrathin mono-like crystalline SiNWs are supposed to be grown at a temperature much lower than the conventional crystal Si ingot pulling temperature, typically at 400°C–600°C [50, 51, 91]. This is also an important capability for achieving a direct layer-by-layer stacked fabrication of CMOS logics or memories, in a truly monolithic 3D architecture. For example, the use of Au-Si alloy catalyst enables a VLS growth of SiNWs down to eutectic point @ 363°C [53]. However, the incorporation of Au into c-Si will introduce deep bandgap levels that are known to be very efficient recombination centers and thus detrimental to high performance Si logics [77, 128]. So, a series of alternative catalyst metals, particularly the group of low-melting-point metals as catalysts, including In@169°C, Bi@270°C, Ga@29°C, as well as their alloys, have been actively investigated in the last decade. Actually, the In-catalyzed IPSLS growth of SiNWs can readily proceed at around 300°C, with a high enough growth rate of 10–100 nm/s [116]. Interestingly, the use of In-Ga alloy catalyst, as shown in Figure 12(a), can help to further reduce the growth temperature even down to $<$90°C, allowing for a direct growth integration of c-Si nanochannels upon flexible PI and PET substrates [86].

On the other hand, it is also possible to accomplish a really high temperature growth of high-quality SiNWs within a cold environment, via selective heating of the leading metallic droplet under near infrared illumination. This has been demonstrated by Zhang et al. [129] in 2021, where they choose the laser beam @808 nm to activate and sustain a very high-speed growth of planar SiNWs, up to 3.6 μm/s, upon glass, wafer, and PI substrates. At this laser wavelength, as shown in Figure 12(b), the light absorption is several orders of magnitude higher in the metal droplet, compared with those in the neighboring substrate and precursor environment. More importantly, the self-selected local laser beam heating enables also a rather swift activation and stopping of the catalyst droplets, providing an extra tool to modulate the geometry, length, and ending location of the IPSLS SiNWs.

4.4 Doping in SiNWs based on IPSLS mode

The doping control in the catalytic SiNWs is a crucial aspect of their microelectronic device applications. While the standard ion-implantation is certainly applicable to control the doping of pristine SiNWs channels, there are two unique approaches for the catalytic growth strategies that have been developed and proven in the literature, which include the incorporation of catalytic metal atoms into the c-Si phase to serve as effective dopants [50, 54, 130, 131], or the introduction of dopant atoms in the gaseous or solid precursor medium that will be later transferred to the as-grown SiNWs [80, 130, 131]. In 2013,

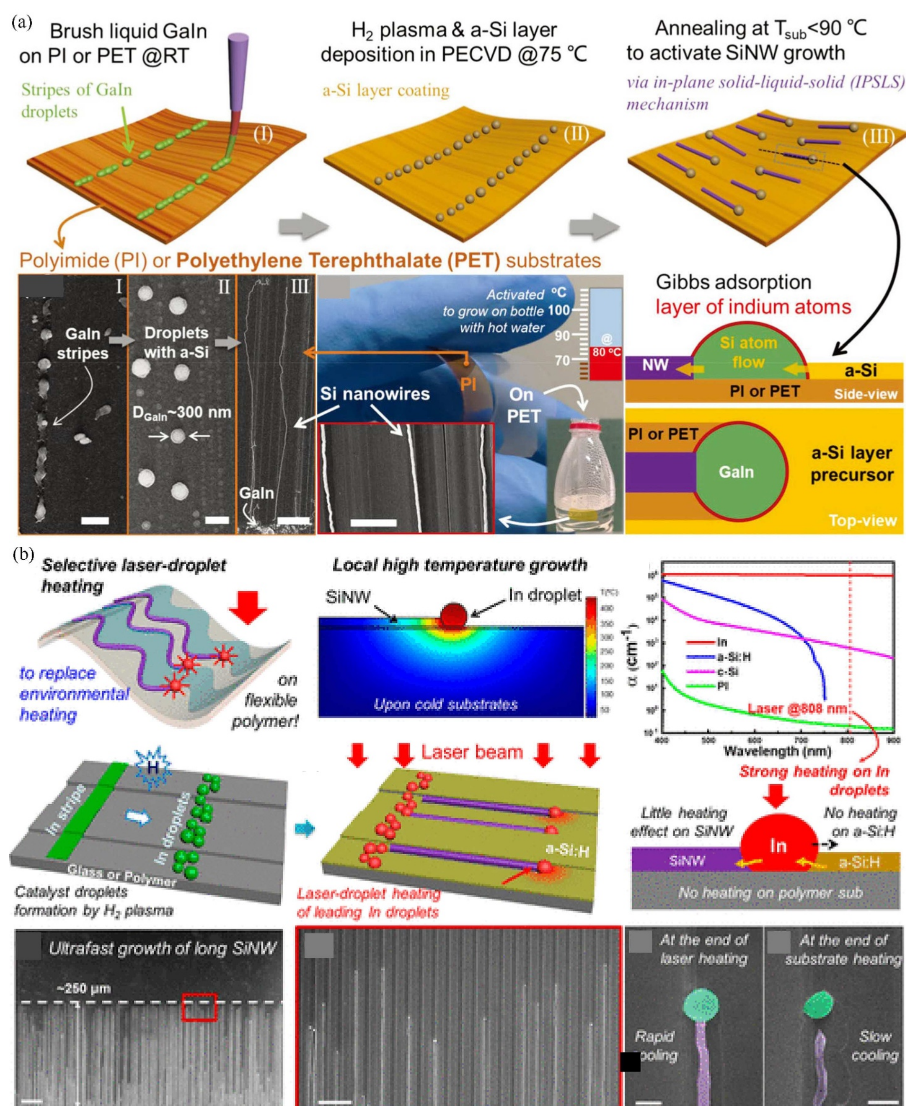

Figure 12 (Color online) Low temperature growth of IPSLS SiNWs via (a) the use of In-Ga alloys [86] Copyright 2020 Royal Society of Chemistry; or (b) activated by laser-droplet-heating (LDH) approach in a cold environment [129] Copyright 2021 American Chemical Society.

Moutanabbir et al. [132] reported a colossal injection of Al catalyst atoms into the VLS grown SiNWs, which achieved a rather high concentration of Al atoms, a p-type dopant in c-Si, into the as-grown SiNWs, far exceeding its equilibrium concentration limit by almost 4 orders of magnitude (Figure 13(a)). This peculiar phenomenon can be understood as the consequence of a fast atomic piling growth at the Al/SiNWs interface, where many catalytic Al atoms were trapped by the rapidly forming new Si neighbor atoms, which enables an extremely efficient and yet tunable injection of a large amount of Al atoms to tune the doping status of the SiNWs. Shortly later, Chen et al. [133] reported a similar catalyst atom injection effect in the planar SiNWs, as seen in Figure 13(b), where the concentration of In atoms in the as-grown SiNWs is found to be growth-rate dependent, which can give off an effective p-type doping equivalent to 10^{17}–10^{18}/cm^3. Other catalyst choice, such as the use of Bi as a catalyst allows an n-type catalyst doping in the IPSLS SiNWs [134]. These results indicate a new doping control dimension that is unique to the metal mediated catalytic growth, while there is still a need for more systematic work to better understand and use this doping strategy.

Another straightforward way for doping control can be accomplished via adding dopant atoms during the precursor feeding to catalytic growth. For example, effective n-type or p-type doping of the VLS-grown Si, or other, NWs have been widely investigated and realized by using dopant gases of diborane, TMB or phosphine [54, 80]. While there have been several excellent reviews for the VLS growth doping

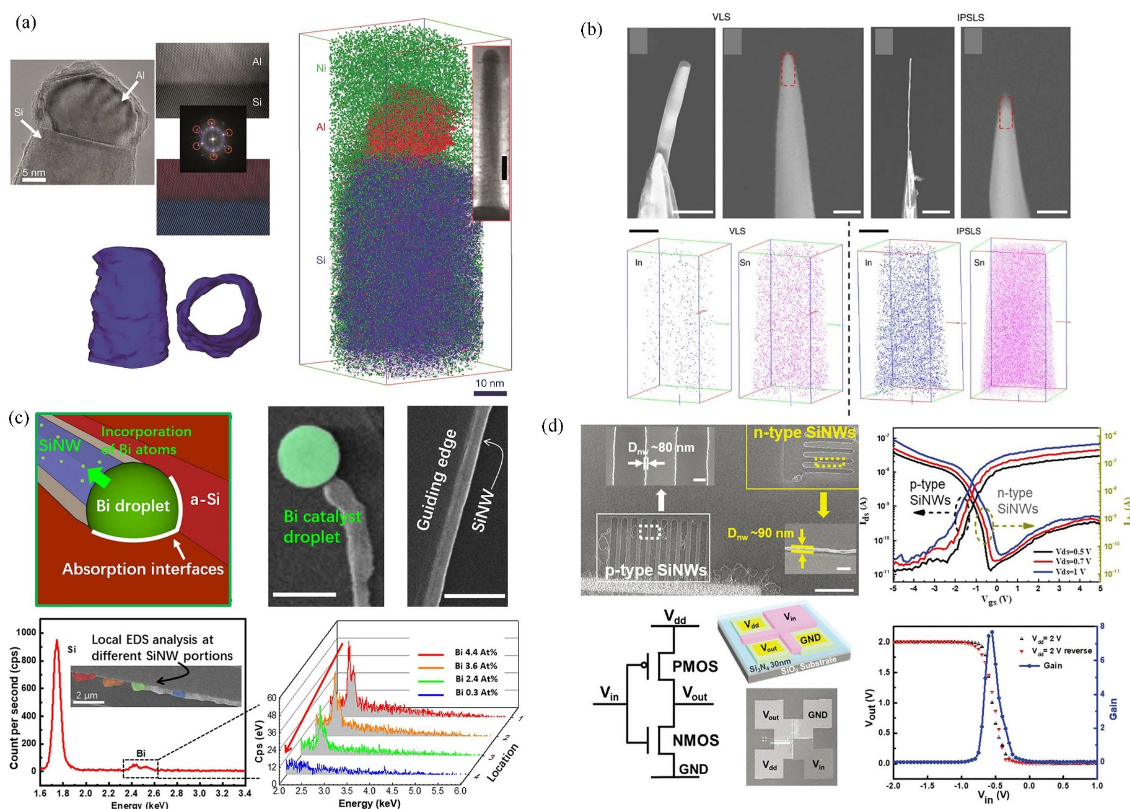

Figure 13 (Color online) Doping control in SiNWs via catalyst atom injection. (a) Al catalyst atoms into SiNWs [132] Copyright 2013 Springer Nature; (b) incorporation and redistribution of metal atoms into SiNWs [133] Copyright 2014 Springer Nature; (c) bismuth-catalyzed n-type doping [134] Copyright 2020 American Institute of Physics; (d) CMOS inverter based on P-type and N-type SiNWs grown via IPSLS mechanism [135] Copyright 2021 Royal Society of Chemistry.

of SiNWs [50, 54, 79, 80], the precursor doping of planar SiNWs was only reported recently. For example, Sun et al. [135] explored the use of pre-doped n-type a-Si:H thin film to accomplish effective and readily tunable n-type doping of the IPSLS SiNWs, converting it gradually from the intrinsic p-type doping status (due to In atom incorporation) to n-type, with the increase of phosphine flow during the a-Si:H precursor deposition in PECVD system. In this way, n-type SiNW FETs have been successfully fabricated, as seen in Figure 13(d), achieving a steep subthreshold swing of 10^5 mV dec^{-1}, on/off ratio of $> 10^7$ and electron mobility of 142 cm^2 V^{-1} s^{-1}. Also, SiNWs CMOS inverters are demonstrated based on closely integrated p-type and n-type SiNWs channels, with a conversion gain of 8 under a supply voltage (V_{dd}) of 2 V. Compared with the above-mentioned catalyst atom doping strategy, the a-Si:H precursor doping is easier to control and more reliable for CMOS device applications, thanks to the well-established a-Si:H doping process.

5 3Dgrowth and assembly of SiNWs

The successful demonstrations of well controlled SiNWs on planar surfaces, via confined or guided catalytic (IPSLS or VLS) growth modes, provide an important basis for a further adventure into more advanced stacked channel GAA FETs and M3D architecture [80, 136]. This represents an exciting opportunity to extend equivalently the scaling of Moore's law, by exploring the extra space in the vertical z-axis dimension that allows integrating more functionalities in a limited footprint area [80, 136, 137]. Particularly, in a stacked M3D architecture, the low temperature catalytic growth provides an important basis for the fabrication of high quality ultrathin SiNWs channels, without the need for the pre-existent wafer. Interestingly, in a 3D space, there are now two possible ways to place the semiconducting SiNWs channels, that is, in a vertically standing or in a horizontally stacked configuration.

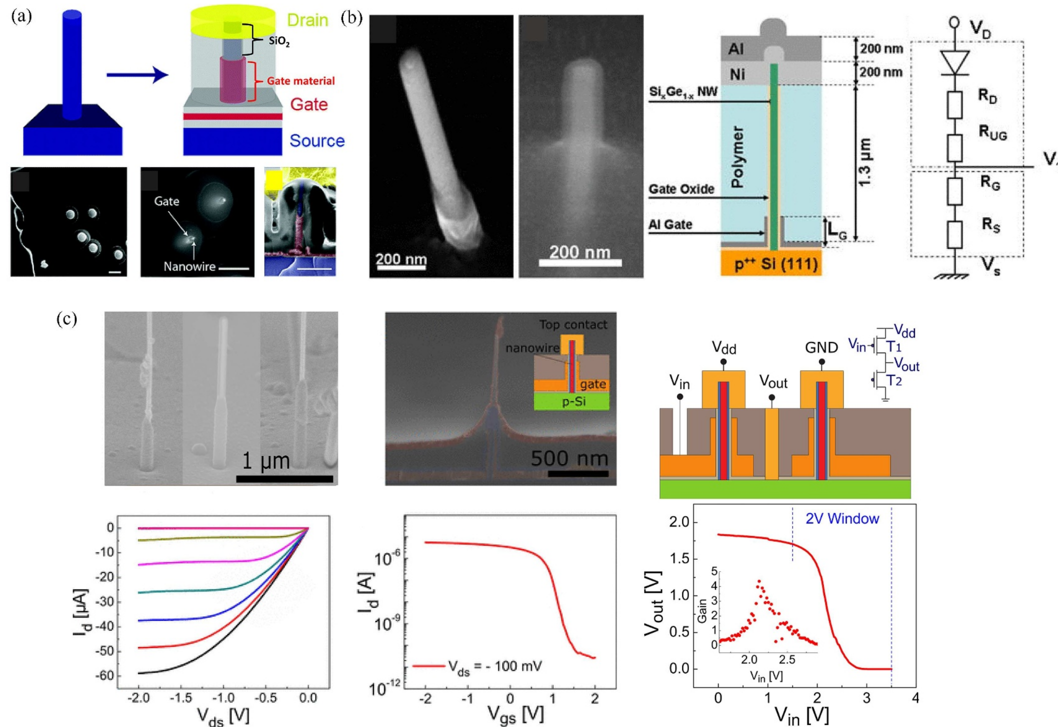

Figure 14 (Color online) Vertical-channel FET devices based on the catalytic VLS growth of SiNWs. (a) Vertical SiNWs FTEs [138] Copyright 2006 American Chemical Society; (b) vertical Si/Ge NWs FTEs [139] Copyright 2011 American Institute of Physics; (c) vertical Ge/Si core/shell NW junctionless transistors [140] Copyright 2016 American Chemical Society.

5.1 Vertical-channel FET based on catalytic SiNWs

Apparently, the most efficient way to minimize the projected footprint area of the NW channels is to place them in standing geometry. To this end, the vertical SiNWs grown via a gas-feeding VLS mechanism seems to be the best choice. As depicted in Figure 14(a), Goldberger et al. [138] demonstrated the first vertical-channel FET (V-FET) device, where the ultrathin VLS-grown SiNWs were electrically connected by the bottom substrate (Source) and the top overhead metal (Drain) electrode pads, in a wrapping gate configuration with a short channel length, as marked in Figure 14(a), determined by selective etching process. The vertical growth is guaranteed, to some extent, by the epitaxial growth of SiNWs starting from the bottom interface bonded to a crystalline c-Si substrate. Though a precise spatial control of these standing SiNWs channels is largely missing, and only a short portion of the SiNW in the lower part has been utilized for the channel, this vertical channel device represents at least the first experimental proof that it is possible to incorporate the low temperature catalytic c-SiNWs to serve as c-Si channels for fabricating advanced GAA FETs, without the need to transfer and place them onto a planar surface.

More recently, V-FET devices with VLS-grown SiGe alloy NWs [139] or Ge/Si core-shell NWs, as vertical channels [140] have also been successfully demonstrated, with reasonable FET device performances, as witnessed in Figure 14(c). More advanced pseudo-CMOS invertor logics were also constructed by connecting neighbored NWs into a serial 3D circuit with matched NWs numbers.

Despite the successful demonstrations of these V-FET prototypes, there are fundamental difficulties for the VLS SiNWs to be employed for scalable device integration in M3D architecture. First, a reliable growth orientation control of the standing VLS SiNWs is still missing, particularly upon non-crystalline dielectric substrate surface; second, the fabrication procedure, used to define the short channel length of V-FETs, is rather complicated and costly, with potential compatibility issues with the standard planar processing; third, a fully 3D logic layout or interconnection scheme for the S/D and Gating electrodes is still under development or in its infancy level for research.

5.2 3D stacked NWs array via layer-by-layer transfer

As a more practical, as well as less demanding, approach to implementing 3D stacked integration of catalyst SiNWs, the VLS-grown SiNWs can be transferred from parent substrates, and deployed via

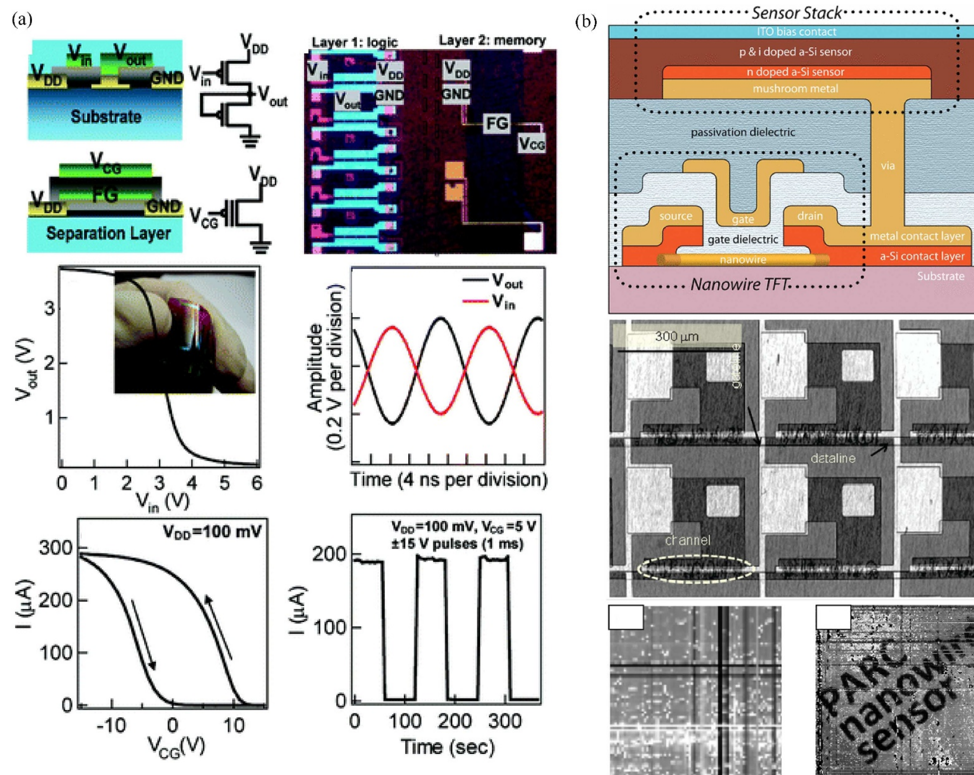

Figure 15 (Color online) Three-dimensional integration of multi-level NWs via layer-by-layer transfer method. (a) Three-dimensional multifunctional circuits based on the assembly of nanowires [110] Copyright 2007 American Chemical Society; (b) hybrid Si nanowire/amorphous silicon FETs for large-area image sensor arrays [111] Copyright 2011 American Chemical Society.

sequential layer-by-layer stacking [80, 136]. As illustrated in Figure 15(a), Javey et al. [110] demonstrated a monolithic 3D integration of parallel arrays of NWs for FET and logic gates, via a hybrid bottom-up and top-down methodology, where Ge/Si core/shell NWs were assembled with controlled orientation and density on the device substrate, followed by sequential contact printing of NWs and flexible plastic dielectric layers. Wong et al. [111] have succeeded in fabricating a prototype a-Si:H p-i-n sensor array integrated with hybrid NWs thin films for large-area electronics, as seen in Figure 15(b). Though these transfer-stacking approaches could find broad applications in a large area or flexible electronics, sensors and displays, the integration density of the as-fabricated devices is still rather low, which is fundamentally limited using a random array of VLS-grown NWs. As a matter of fact, a high density M3D integration will demand a precise position and alignment control of every single NWs channel, which is extremely difficult, if not impossible, for the growth-and-transfer approach. In other words, the high-quality c-Si or Ge/SiNWs are supposed to be grown-in-place for achieving a reliable growth integration of high-performance and highdensity NWs-based microelectronics.

5.3 3D integration based on other semiconducting materials

Though this review is focused on the growth integration of Si-based NWs for CMOS logics, it is also important to note that there are considerable recent research efforts devoted to non-Si FET channel materials, as promising candidates for potential M3D applications. These include carbon nanotubes (CNTs) [31, 32], van der Waals 2D materials [36, 37], and amorphous oxide semiconductor (AOS), for example IGZO and ZTO [39, 41], which also hold a potential for high performance microelectronics in M3D architecture.

A more promising candidate for high performance electronics comes from well-aligned CNT thin films, with proper chemical and chiral properties, which have been widely adopted as an excellent semiconducting thin film to demonstrate impressive integrations of millions of high performance logic/memory gates, even in an M3D architecture with fine-grained and dense vertical VIA connectivity between stacked layers of logic, storage, input, and output, as seen in Figure 16(a) [32]. In parallel, TMDC materials were emerging, in the last decades, as a new class of crystalline 2D materials, which have been heavily

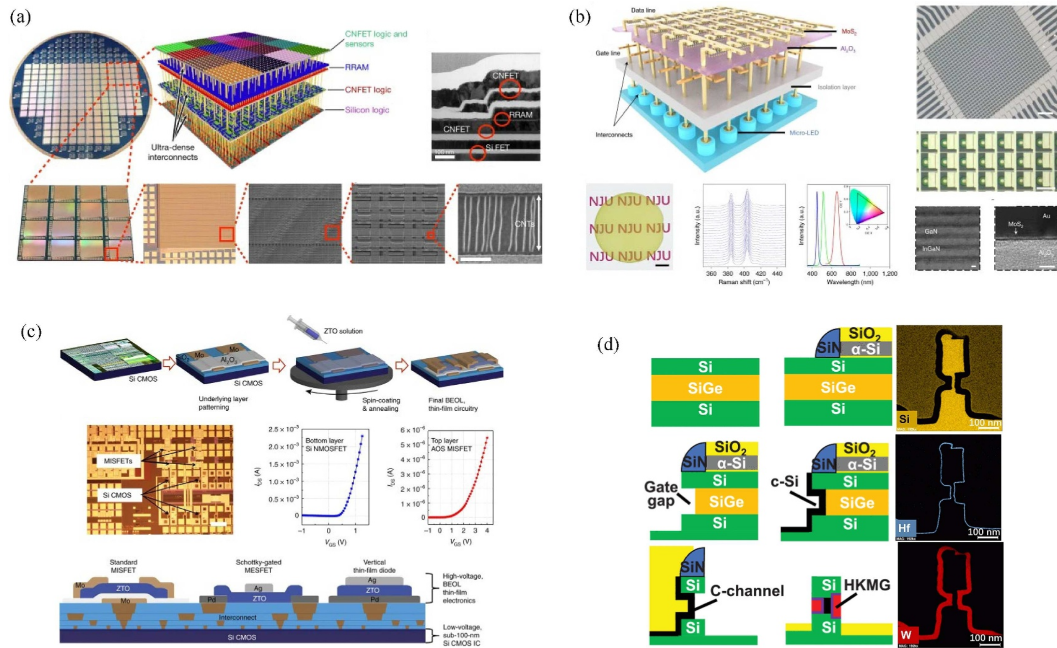

Figure 16 (Color online) Monolithic integration 3D with different top BEOL transistors. (a) Carbon nanotube transistors [32] Copyright 2017 Springer Nature; (b) MoS_2 transistors [35] Copyright 2021 Springer Nature; (c) metal oxide thin-film transistors [38] Copyright 2019 Springer Nature; (d) vertical-FETs quoted from Figures 1 and 3 in [143] Copyright 2022 IEEE.

researched for high performance electronics. For example, atomically thin MoS2 TFTs have been successfully demonstrated, serving as the driving circuits for active matrix micro-LED displays, and exhibited excellent electrical performance and uniformity (Figure 16(b)) [35]. In addition, AOS represents a group of important semiconductor thin film materials that can be readily sputtered over large area substrate at low temperature, with high optical transparency and excellent uniformity. Monolithic integration of standard AOS transistors directly on top of the state-of-the-art Si CMOS Fin-FETs (see Figure 16(c)) has been successfully demonstrated in [38].

Though all these non-Si nanostructured channel materials demonstrated high performance FET electronics, there are still several critical concerns or challenges that need to be better addressed, in view of building high performance CMOS logics in M3D architecture: (i) the lacking of complementary doping channel materials, particularly for high performance p-type AOS FET, which are necessary to construct true CMOS logics; (ii) scalability and reliability of the 2D TMDC and CNT channels still need to be systematically verified within the standard high-density microelectronic integration framework, especially for their processing compatibility to the cutting-edge <N22 nm c-Si technology node.

5.4 Horizontal SiNWs grown on oblique terraces

Considering the vast mature technological know-how on the complementary doping, surface passivation and processing built upon the abundant c-Si materials, ultrathin 1D SiNWs are probably the most promising channel materials to accomplish high density M3D integration. To this end, catalytic VLS growth of standing SiNWs provides excellent 1D channels for V-FETs, with advantageous GAA-gating configuration, but is unfortunately difficult to be integrated directly into the mainstream planar integration platform (see Subsection 5.1). Though recent research studies have demonstrated the growth of VLS SiNWs perpendicularly on the vertical sidewalls to bridge the gap between S/D electrodes [141,142], there is still no FET device ever made based on these laterally grown VLS SiNWs bridge channels, largely because of their random spatial distribution and stochastic variation in the growth directions. So, a more convenient and practical approach could be the catalytic growth of an ordered array of horizontal SiNWs, either as a vertical stack of SiNWs as 1D channels in a GAA FET unit [143,144], or deployed in different stacked logic/memory layers for achieving non-von Neumann M3D integration [75,145].

While the single-step guided IPSLS growth has enabled a precise location and geometry control of orderly planar SiNWs, the spacing of the SiNW channels is fully determined by the lithography resolution used to pattern the step edge lines [120]. To boost the integration density of the catalytic SiNWs, without

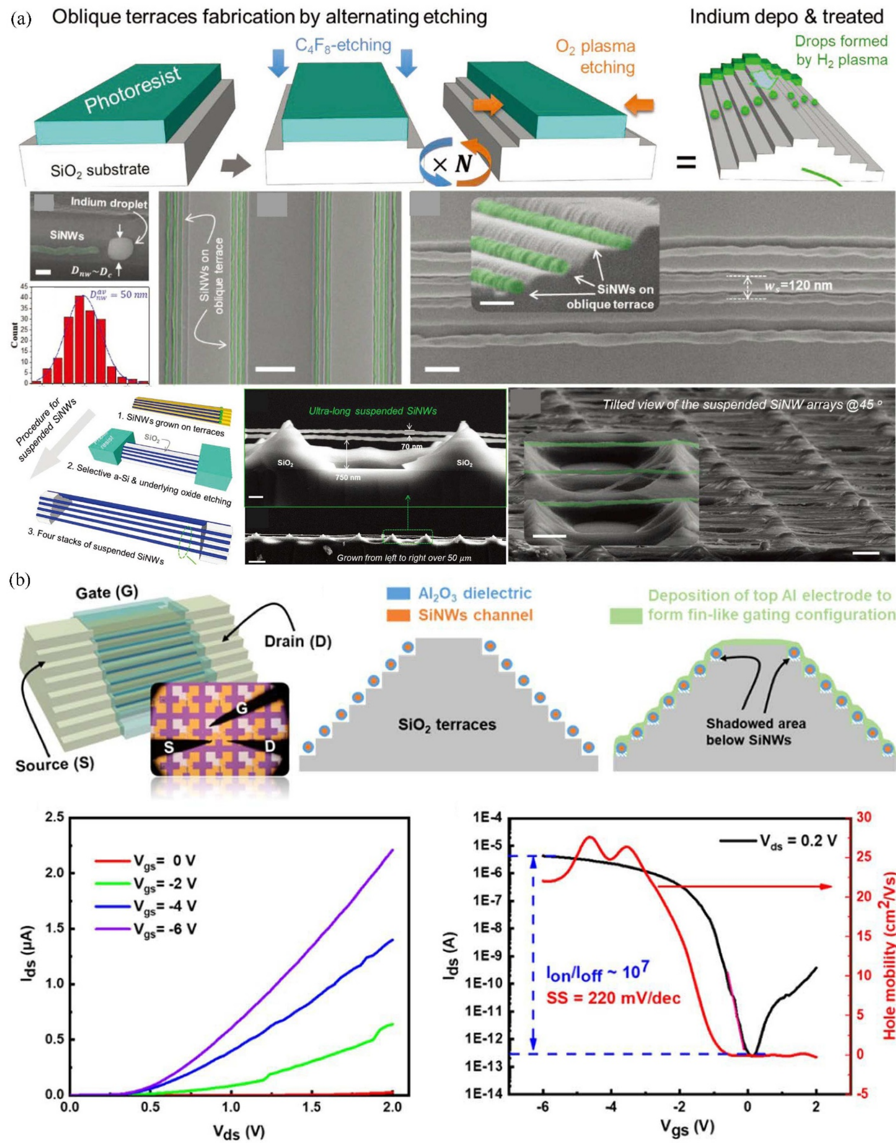

Figure 17 (Color online) Parallel NWs grown on oblique terrace. (a) Oblique terrace guided (OTG) growth of SiNWs [137] Copyright 2019 John Wiley and Sons; (b) high-density fin-TFT devices [146] Copyright 2021 Institute of Physics.

demanding higher lithography resolution, a terrace-confined guided strategy has been developed by Wu et al. [137], where a series of mini-steps were formed by simply repeating several cycles of etching-oxidation steps at the original place of edge lines defined by conventional lithography. During the etching cycle, mini-steps were first etched into the substrate in the region uncovered by the photoresist (PR), followed by an oxidation cycle that burns and retreats the edge of PR to a width controlled by the process duration. After several cycles, an oblique terrace composed of 6-10 mini-steps of ∼100 nm wide can be easily formed, providing a high-density array of guiding edges for the growth of closely packed IPSLS SiNWs, as shown in Figure 17(a). Based on these SiNWs channels, simple fin-gated and junction-less TFT device prototypes were also demonstrated, showing impressive device performance that is particularly suited to large area electronics or display driving logics.

Interestingly, these relatively thick and long SiNWs can also be easily suspended via a selective diluted HF solution etching, which removed the underlying oxide layer, leaving suspended long SiNWs held by the preserved pillars at the two ends [137]. By improving the etching stability for stable formation of tiny mini-steps, ultrathin SiNWs with a diameter down to 27 nm have been obtained, see Figure 17(b) and [146]. Though this low temperature catalytic growth guided by terrace mini-steps provides a route to the integration of a dense array of horizontal SiNWs, it is unable to produce vertically stacked horizontal

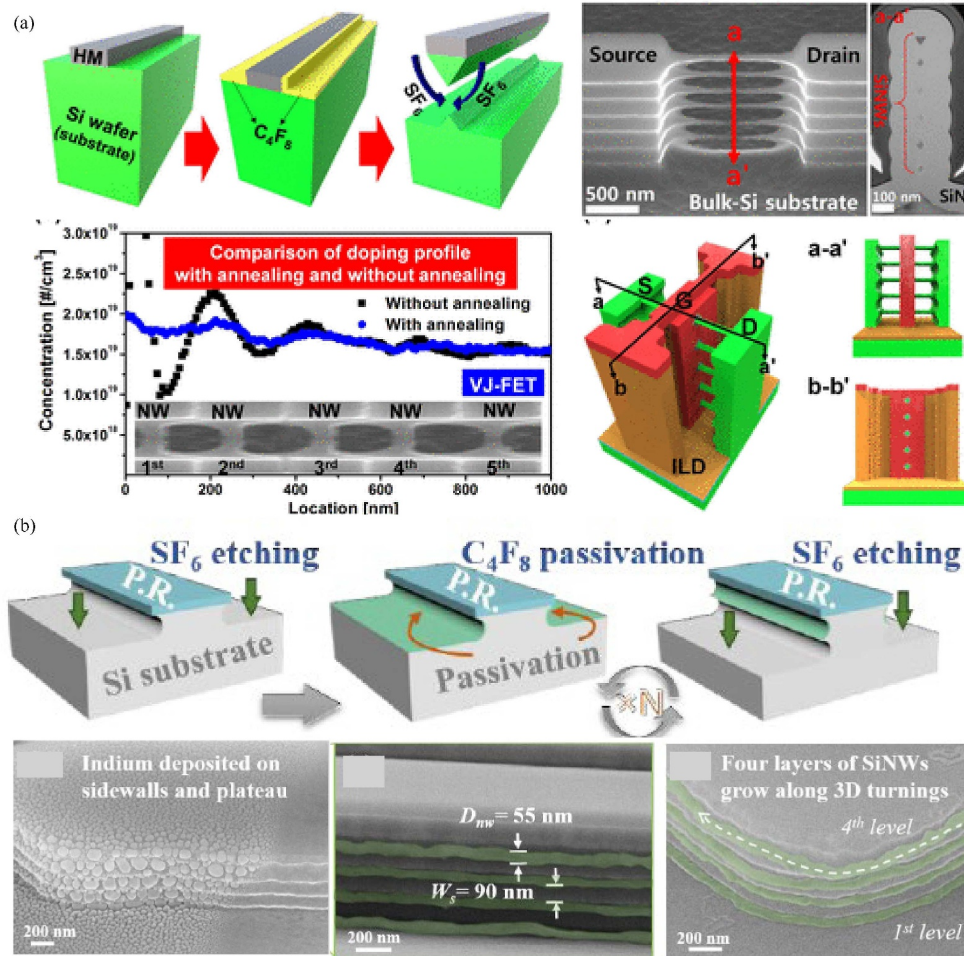

Figure 18 (Color online) Stacked horizontal SiNWs fabricated based on the Bosch-etching technology. (a) SiNWs formed by top-down etching of Si substrate via Bosh process [148] Copyright 2016 American Chemical Society; (b) SiNWs grown on Bosch-etched sidewalls via IPSLS mechanism [149] Copyright 2020 Royal Society of Chemistry.

SiNWs, which are needed for the construction of advanced GAA FET logics in <N5 nm technology node.

5.5 Vertical stack of horizontal NWs grown on sidewalls

It is noteworthy that the nanoscale IPSLS growth, by itself, is insensitive to the influence of gravity. So, it makes no difference for the leading catalyst droplets to move and produce SiNWs on a flat substrate surface or on the tilted or vertical sidewalls, as long as a-Si:H precursor thin film coating is present. So, following this logic, it is easy to conceive that a well-guided IPSLS growth of orderly SiNWs should also take place even on vertical sidewalls, of course, with the aid of patterned sidewall grooves to control the position and orientation of the as-grown SiNWs. Actually, the simplest form of such sidewall grooves can be easily obtained during a Bosch etching of c-Si wafer [147] which is a well-known high-aspect-ratio deep Si etching technique with alternating SF_6/C_4F_8 plasma. Bosch etching alone can be utilized to produce stacked horizontal SiNWs, as shown in Figure 18(a), where Lee et al. [148] demonstrated the formation of a five-story stack of SiNWs via a slightly overdone Bosch etching of a thin ledge that leaves discrete c-Si bridges suspended between heavily doped S/D electrodes. This top-down Bosch dry-etching approach is rather convenient and straightforward, but requires the pre-existing c-Si wafer and a final high temperature (> 900°C) oxidation to form the discrete nano-bridges, which are not fully compatible with M3D integration. Moreover, the uniformity of the as-formed Si nano-bridges could also be a challenging issue, as seen in Figure 18(a), where the cross-section and diameter vary significantly from the top level to the bottom one.

Fortunately, the nanoscale grooves formed on the Bosch-etched sidewalls by themselves are nice guiding tracks to direct the IPSLS growth of stacked horizontal SiNWs, as seen in Figure 18(b). Hu et al. [149]

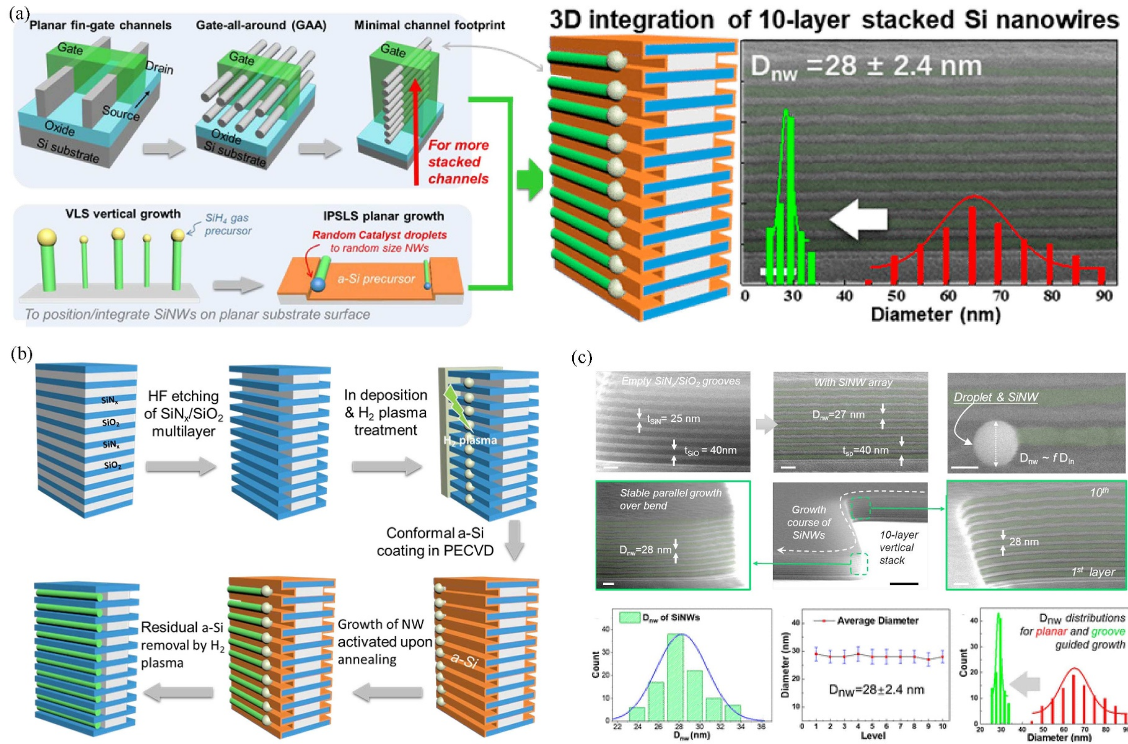

Figure 19 (Color online) IPSLS sidewall growth of 3D stacked SiNWs. (a) Schematic illustration of a 10-layer stacked parallel growth of SiNWs; (b) fabrication procedure for 3D parallel sidewall growth of SiNWs; (c) morphology and statistics of 10-layer stacked SiNWs [150] Copyright 2020 American Chemical Society.

demonstrated that the groove dimensions can be readily adjusted by tuning the Bosch plasma etching parameters. After catalyst droplet formation and a-Si:H coating, 4 layers of parallel IPSLS SiNWs were found to grow exactly along the sidewall grooves, even over the turning corners. The diameter and spacing of the sidewall SiNWs grown in the scallop-shaped grooves are around 55 and 90 nm, respectively, roughly determined by the Bosch etching conditions. However, further downscaling of the Bosch grooves, to produce even thinner SiNWs with even higher density, turned out to be technically challenging and instable. Also, the smoothness of the Bosch-etched grooves needs to be improved, otherwise, this random roughness will be copied by the grown-over SiNWs, leading to degraded uniformity of the SiNW diameters. So, a more precise and reliable sidewall groove formation technique is desired, to impose a stronger and more uniform guidance of ultrathin IPSLS SiNWs.

5.6 Ultra-confined stacked growth on superlattice sidewalls

There is indeed another approach to fabricating rather uniform and narrow sidewall grooves, as shown in Figure 19(a), where a superlattice stack of 10 periods of SiO_2/SiNx was first prepared by alternating plasma deposition in the same PECVD chamber, and then etched through to expose the vertical sidewalls at desired locations [137]. After that, the sidewall surface was treated in a diluted HF solution. During this selective etching process, the exposed SiO_2 layers were eroded faster than that of SiNx layers, and thus a regular array of concave oxide grooves, bounded by protruded nitride walls, were developed upon the truncated sidewalls. In this way, the widths of the grooves and the walls were fully determined by the corresponding PECVD deposition cycles, which can be readily controlled to a high precision of 1–2 nm, providing a key capability to confine and fine-tune the growth of SiNWs on the vertical sidewall surfaces.

Surprisingly, with the guidance of these ultra-narrow and uniform superlattice sidewall grooves, a 100% guided growth of 10-layer stacked horizontal SiNWs has been successfully accomplished, with a narrow diameter and NW-to-NW spacing of only 28 ± 2.4 and 40 nm, respectively [150], which can almost compete with the state-of-the-art top-down lithography and etching technologies, in terms of stacking number and channel uniformity. Also, the IPSLS growth was found to be rather stable, traveling over a long guiding track of Lnw > 50 μm, which offers an opportunity to fabricate multiple FET units upon single ultralong SiNWs, an extra bonus brought by the highly efficient catalytic growth.

In the standard top-down etching fabrication of GAA FETs, as introduced in Section 2, the stacked SiNW or nanosheet channels were patterned out of epitaxially grown GeSi/Si multilayers and released via selective etching of the Ge-rich portion. So, the channel width has to be defined by using sophisticated EUV lithography [151]. In comparison, the catalytic growth of multilayer of SiNWs can grow at a rather low temperature $< 350°C$ and the stacked SiNWs growth process will take place simultaneously in all the 10 grooves [150]. Obviously, this catalytic parallel growth does not rely on the delicate epitaxial growth of GeSi/Si multilayer as a starting wafer, and thus could be far more economical and efficient. On the other hand, during such groove-confined growth, the width and height of the SiNWs channels are defined by the oxide-layer thickness $t_{\rm ox}$ and the selective etching depth $d_{\rm etch}$, while both can be precisely controlled by the PECVD deposition or etching durations. So, it is by this feature dimension transformation strategy, that a relatively simple catalytic growth can be exploited to produce well-positioned, vertically stacked, and uniform SiNWs.

It is also interesting to note that, the capability to achieve 10-layer stacking of SiNWs channel could also help to alleviate the demand for high resolution EUV lithography. For example, in the latest GAA FET unit [22], 3–4 columns of 3-layer-stacked SiNWs were taken as a group to serve as the channel for a single FET unit. So, if all these channels can be stacked into a single column, as depicted in Figure 3(c), the channels can be arranged with a sparser separation. Based on this catalytic stacked growth, one can first use relatively low precision lithography to define the edge for SiNWs-stacking, and then grow all the SiNWs into a single stack, preserving equivalently the same lateral NWs channel integration density. Of course, such a high SiNWs-stacking-number design might bring in other technical issues that need to be better addressed, by developing new electrode connection technologies, in the M3D integration architecture.

In pursuit of even higher integration density and further downscaling of the SiNWs channels, a self-delimited catalyst formation strategy was developed to demonstrate a growing integration of SiNWs with critical dimension (CD) <10 nm, with channel width and height of 9.9 ± 1.2 nm (down to 8 nm) and 18.8 ± 1.8 nm, respectively, approaching to the CD-10 nm technology node [152]. This has been done with improved size and uniformity control of the leading indium catalyst droplets. As shown in Figure 20(a), proper control of the tilted angle of In vapor evaporation can achieve a special distribution of self-delimited In particles both on the walls and within the groove surface that will encourage a directional merging to fill in only the nearest grooves. In this way, the sidewall grooves can be safely downscaled to even smaller dimensions, to enforce the growth of much thinner and uniform SiNWs.

Furthermore, there are several distinctive features of catalytic growth that have been demonstrated in this work. First, it was shown that the SiNWs can be continuously guided to grow around sharply turning corners with a local radius of ∼150 nm. This makes it possible to compose or design more complex logic circuits directly upon the multiple rows of stacked SiNWs channels, with enhanced size uniformity and the least use of metal catalyst droplets. Second, HR-TEM characterizations confirm that all these ultrathin catalytic SiNWs were found to be mono-crystalline, with dominant growth orientations in Si⟨110⟩ direction and other abnormal growth orientations in Si⟨100⟩ and Si⟨211⟩ directions. Third, the aspect ratio of the SiNWs can be effectively controlled by varying the groove profile, which is a critical capability for the fabrication of GAA FET devices, where the channel cross-section tailoring is a key parameter that has a significant influence on the device performance.

Prototype devices were also made based on these ultrathin sidewall SiNWs channels, but in a simple JL Schottky Barrier FET configuration, with Pt (5 nm)/Al (55 nm) S/D electrodes connected to the SiNWs in sidewall grooves, without channel suspension and GAA gating. As shown in Figure 20(c), the SiNWs FET demonstrates $I_{\rm on}/I_{\rm off}$ ratio $> 10^6$ and SS of 125 mV/dec, mostly limited by the imperfect S/D contacts. Certainly, there are still plenty of work ahead to achieve a reliable suspension releasing of these catalytic SiNWs, improved epitaxial or ion implanted S/D contacts and testify their full device potential in proper gating configuration. In parallel, several fundamental aspects that still need to be systematically investigated and better understood, such as the role of groove confinement on the preferential growth orientation, doping profile engineering, growth stability of catalytic GeSi alloy NWs. In addition, whether there is a fundamental limit for the scaling of IPSLS SiNWs into deep nanometer region, for example, <3 nm.

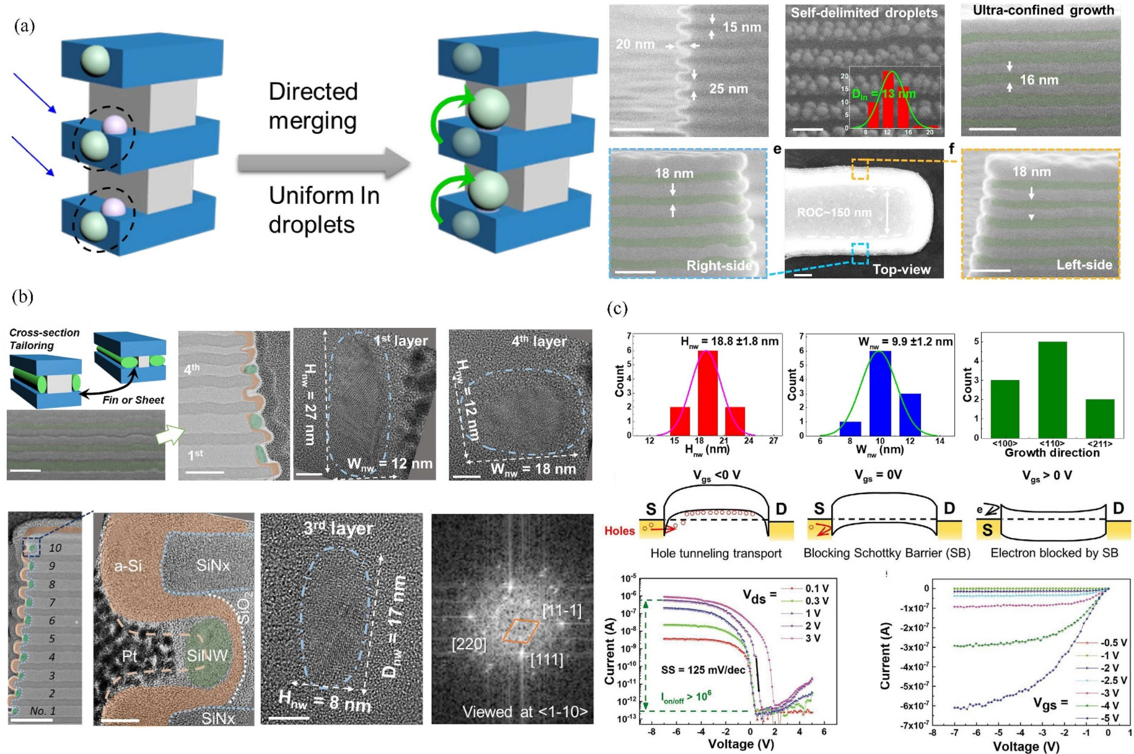

Figure 20 (Color online) Ultra-thin stacked SiNWs with CD <10 nm. (a) Self-delimited catalyst formation and growth; (b) cross-section geometry control; (c) Schottky Barrier FET [152] Copyright 2022 John Wiley and Sons.

6 Summary and perspectives

In this review, we first revisited the evolution of modern microelectronics over the last few decades, driven by the exponential need for computing power in the booming digital information economy and AI applications. During the aggressive miniaturization of c-Si CMOS logics, with FET channels evolving from planar to fin and GAA-gating configurations, the benefits of using ultrathin SiNWs as channels have been widely recognized. Similarly, monolithic 3D integration is a promising routine for pushing forward Moore's law and experimenting with new non von Neumann architecture paradigms of in-memory and neuromorphic computing. To address the challenges of high-precision lithography and 3D integration of c-Si logics, the catalytic growth of ultrathin mono-like SiNWs has been extensively investigated in the last 20 years, to establish an alternative bottom-up approach to batch fabricate high-quality semiconducting 1D channels via a high-yield and diverse low-temperature procedure for the construction of advanced FET logics, sensors, and memories. Among these, the gas-feeding VLS growth of SiNWs is the most studied and well-known catalytic process, and it has been widely used to prototype several high-performance SiNW logics and functionalities. The lack of reliable and convenient growth position control of the VLS-grown SiNWs has been identified as a major barrier to scalable device integration on the mainstream planar electronic framework. This issue can be addressed more effectively by using a relatively new IPSLS growth mechanism, that uses a group of low melting point metal catalyst droplets to consume a-Si:H thin-film precursor and produce well-aligned SiNWs, naturally confined on the substrate surface. Therefore, the evolution of the IPSLS growth technology was reviewed, with a focus on the key capabilities required to establish precise and reliable integration of SiNW electronics, such as deterministic guided growth on planar or vertical sidewall surfaces, complementary doping control, low temperature growth, and the potential of ultra-confined catalytic growth for critical dimension downscaling. Recent research on the fabrication of SiNWs FETs in vertical and stacked horizontal channel configurations is also investigated. With all these new advances in fundamental understanding and technological breakthroughs, the catalytic IPSLS growth, even though still in a burgeoning stage, has gradually come to establish itself as a feasible new routine particularly suited for high-yield production and monolithic integration of ultrathin and designable SiNWs channels, which can be reliably deployed in 3D architecture, for the implementation of emerging non von Neumann computing and AI-oriented functionalities.

For the future development of catalytic growth toward a reliable 3D device integration approach, it is critical to note that all these bottom-up catalyst growth strategies should be viewed as new functional supplements to mainstream top-down technologies, rather than a complete alternative, by bringing in new capabilities to address the challenges encountered in top-down lithography or 3D integration. As demonstrated by the strongly confined sidewall guided growth of ultrathin SiNWs, the potential of catalytic growth can only be realized within the framework and support of mature c-Si technology. There are still a plethora of research topics and opportunities on the horizon that merit more through systematic investigations. The main conclusions of this review are as follows:

(1) Despite the demonstration of successful size, orientation, and stacking control of catalytic SiNWs using IPSLS or VLS methods, a high-precision deterministic growth control of SiNWs in terms of diameter, uniformity, reproducibility, and surface passivation, is always a challenging issue that necessitates continuous innovations in growth or post-growth tailoring technologies, to approach the high standards achieved in mainstream top-down c-Si technology.

(2) Systematic work is required to establish a fabrication procedure dedicated to the catalytic growth integration of high-performance GAA FET devices, including SiNW channel suspension, dielectric passivation, work function matching, epitaxial growth, or S/D doping contacts.

(3) It is still debatable whether there is a well-defined growth orientation for all catalytic growth as well as how to achieve the desired c-SiNW orientations, while catering to the needs of n- and p-type channels, both of which are critical issues for both fundamental understanding and practical device applications.

(4) As a positive or negative aspect, the incorporation of catalytic atoms into as-grown SiNWs enables easy channel doping for rapid device prototyping but still needs to be more effectively controlled, as a key to building balanced high-performance CMOS logics.

(5) While the diameter of the stacked IPSLS SiNWs has been reduced to <10 nm, an intriguing question remains regarding the size limit for catalytic growth, which has a profound effect on producing well-positioned and aligned ultrathin 1D channels, particularly in the deep nanometer regime with a considerable quantum size confinement effect.

(6) How to extend the unique capability of catalytic growth to build functional 3D nanostructures such as a standing 3D helical structure that is difficult to fabricate for top-down lithography-etching but could find novel post-Moore applications in chiral optics, NEMS sensing, and optical memories.

With all these things said, we have seen an exciting start to the catalytic growth toward a reliable and industrially applicable new integration technology. This goal will undoubtedly fall short without well-coordinated and multidisciplinary joint efforts, in both theoretical and experimental aspects. It is also possible that a more deterministic and programmable catalytic growth will considerably promote or accelerate the implementation of advantageous 1D SiNW channels in a variety of application scenarios, which are not limited to microelectronics, but also fieldeffect sensing, human-machine interfaces, flexible displays, and physics-aware deep learning.

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