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Letter

Unprecedented Uniform 3D Growth Integration of 10-Layer Stacked Si Nanowires on Tightly Confined Sidewall Grooves

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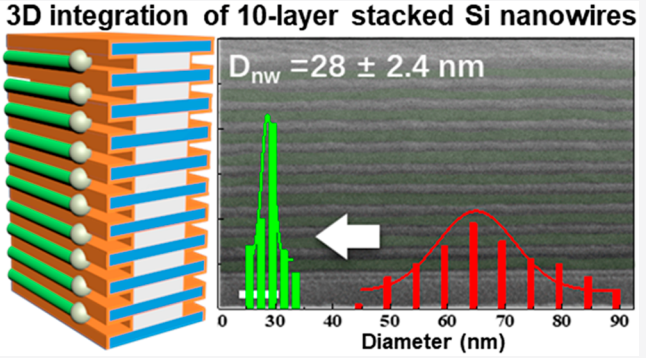
ABSTRACT: Bottom-up catalytic growth offers a high-yield, versatile, and powerful tool for the construction of versatile 3D nanocomplexes, while the major challenge is to achieve a precise location and uniformity control, as guaranteed by top-down lithography. Here, an unprecedented uniform and reliable growth integration of 10-layer stacked Si nanowires (SiNWs) has been accomplished, for the very first time, via a new groove-confined and tailored catalyst formation and guided growth upon the truncated sidewall of SiO_2/SiN_x multilayers. The SiNW array accomplishes a narrow diameter of D_{nw} = 28 ± 2.4 nm, NW-to-NW spacing of t_{sp} = 40 nm, and extremely stable growth over L_{nw} > 50 μm and bending locations, which can compete with or even outperform the *state-of-the-art* top-down lithography and etching approaches, in terms of stacking number, channel uniformity at different levels, fabrication cost, and efficiency. These results provide a solid basis to establish a new 3D integration approach to batch-manufacture various advanced electronic and sensor applications.



KEYWORDS: *3D growth integration, Si nanowire, stacked channels, in-plane solid−liquid−solid*

Bottom-up catalytic synthesis of one-dimensional nanowires (NWs), led by metal nano droplets, is best known as a high-yield and low-cost fabrication with diverse geometrical and compositional tunability.[1−5] However, the major challenge is how to integrate these tiny building blocks precisely for scalable electronic integration, as accomplished by the *top-down* lithography approach. On the other hand, fabricating 3D nanostructure complexes is rather difficult or inefficient for planar lithography, particularly for the fabrication of vertically stacked SiNW channels that will be adopted in the 5 nm-Technology Node[6] field effect transistors (FETs) to minimize the channel footprint and maximize the gate-channel capacitive coupling in a gate-all-around (GAA) configuration, as depicted schematically in Figure 1a. Usually, these 3D stacked SiNW channels are fabricated by top-down etching of heteroepitaxially grown Si/GeSi multilayers, followed by selective etching of the sacrificial Ge-rich spacers to leave suspended SiNWs.[7−9] In order to boost the drive current or integrate more logic units in the future, a larger stacking channel number N_{stk} is preferred, but this is constrained by the increased fabrication complexity and cost. So far, the stacked channel number in the disclosed GAA-FET devices is mostly N_{stk} = 3−6.[10−12]

Actually, *growing* SiNWs in a 3D architecture could be more efficient and convenient than *caving* them out of bulk materials. It has been demonstrated in our previous works that planar SiNWs can be grown by using indium (In) catalyst droplets, via an in-plane solid−liquid−solid (IPSLS) mechanism,[13−18] which can be guided by single step edges to grow into predesigned locations and routines on the surfaces coated with an amorphous Si (a-Si) precursor layer,[15,19−21] enabling thus a more convenient deployment of orderly SiNW channels for building FET devices, compared to the growth-transfer arrangement of vertically grown SiNWs via the vapor−liquid−solid (VLS) mechanism,[22−24] as depicted in Figure 1b. In addition, the IPSLS growth is also applicable to the tilted or vertical sidewalls, in defiance of the influence of gravity,[25,26] while the major drawbacks are the large SiNW diameter variation, typically ∼30%[27] due to the wide size dispersion of the leading In catalyst droplets, and the low integration density with NW-to-NW spacing >120 nm, which are far from what one would expect from a high-precision integration. Though prepatterning of the catalyst pads, by using electron beam lithography (EBL)[28−30] or polystyrene sphere lithography,[31,32] is known to greatly improve the diameter uniformity of VLS-grown SiNWs, these elaborate template technologies are inefficient or inadequate for patterning directly on the out-of-plane 3D surfaces.

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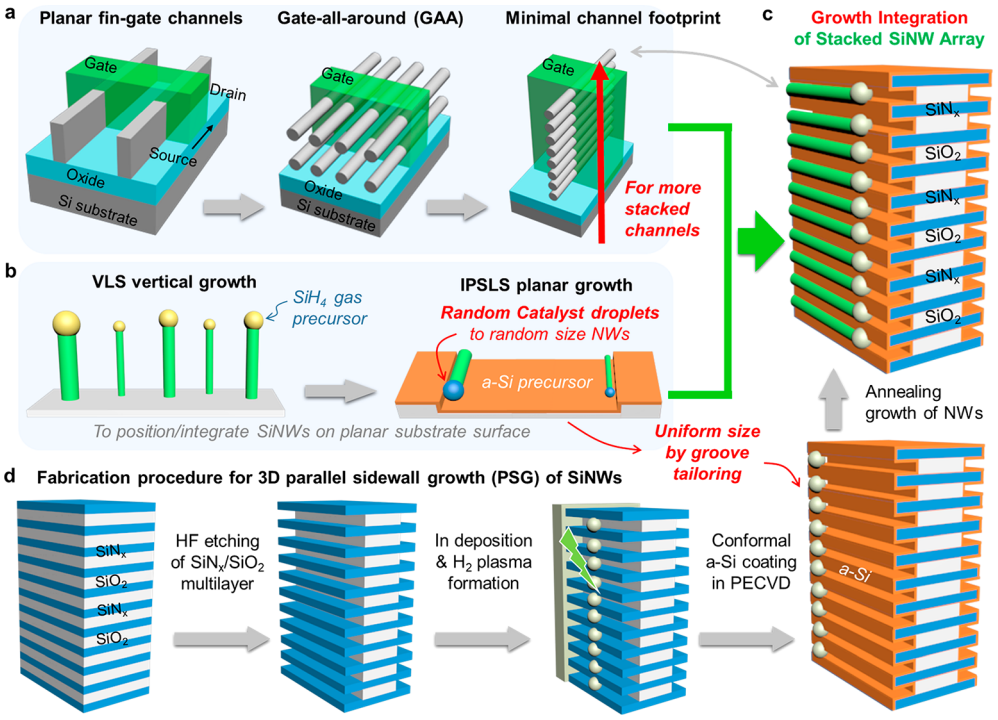

Figure 1. (a) Schematic evolution of the FET channels from fin-gate to GAA and to stacked channel configuration, where a high stacking number is preferred to minimize the channel footprint area and improve the drive current. (b) Comparison of the catalytic vertical growth of SiNWs via VLS mode to the guided growth of planar SiNWs via the IPSLS mechanism, where the SiNW diameters are determined by the size of leading catalyst droplets. (c) Illustration of a 10-layer stacked parallel growth of SiNWs, led by In catalyst droplets, on the truncated sidewall of SiN_x/SiO_2 multilayers, via a fabrication procedure depicted schematically in part d.

In this work, we report an unexpected uniform growth of an ultrathin SiNW array on the truncated vertical sidewalls of SiO_2/SiN_x multilayers. Surprisingly, the In catalyst formation confined within the narrow grooves, with widths smaller than the In atom surface diffusion length, can greatly suppress the random agglomeration and eliminate the undesired edge-riding droplets that are identified as the major causes for the large diameter fluctuations among neighboring SiNWs. With optimized parameter control, the SiNWs grown on the different groove levels, with stacking number up (but not limited) to 10 layers, achieve a uniform diameter of 28 ± 2.4 nm, spacing of t_{sp} = 40 nm, and very stable growth L_{nw} > 50 μm even over bending corners, representing a new landmark for high-precision 3D catalytic growth control that can compete with the state-of-the-art top-down approach. The underlying mechanisms are also discussed based on a groove-tailored diffusion model and neighbor-coupled merging and competition growth dynamics.

As schematically depicted in Figure 1d, the SiNWs were grown upon the truncated sidewalls of SiO_2/SiN_x multilayers with N_{stk} = 4−10 periods of oxide and nitride sublayers of t_{SiO} and t_{SiN} thick, respectively, which are deposited upon wafer or glass substrates by using a plasma enhanced chemical vapor deposition (PECVD) system and patterned by lithography and etching to expose the sidewalls. After that, the sample was immersed in a diluted 0.5% HF solution to *selectively* erode the oxide layer (at an 8−10 times faster etching rate than that of the nitride layer) to produce periodic concave grooves, with depth controlled by the HF etching duration. A typical scanning electron microscopy (SEM) image of the resulting sidewall grooves, prior to the growth of SiNWs, is presented in Figure 2a, where the bright stripes are the protruding SiN_x edges, while the darker regions are the concave SiO_2 grooves. Then, In catalyst stripes were deposited by electron beam evaporation (EBE), via lithography and lift-off procedure, crossing the sidewall lines, as depicted in Figure 1d. During the EBE deposition, the sample was placed tilted 60° on the substrate to expose the targeted sidewalls to the incident In atom flux. In the next step, the samples were loaded into the PECVD system for a H_2 plasma treatment at 250 °C to reduce the surface oxide of the In droplets, followed by an a-Si layer coating at 100 °C. Upon annealing at 350 °C, the In droplets were activated to absorb the nearby a-Si and to move along the guiding grooves and produce parallel SiNWs on the vertical sidewalls. At the end, the remnant a-Si layer can be selectively cleaned off, preserving only c-SiNWs, via a low-temperature H_2 plasma etching at 150 °C.

Parts b−f of Figure 2 show the typical SEM images of a parallel sidewall growth of 10-layer SiNWs, where the thin SiNWs are tinted to green for the ease of observation. Remarkably, the SiNWs grown with t_{SiO} = 40 nm and t_{SiN} = 25 nm are rather uniform, with a thin diameter of D_{nw} = 28 ± 2.4 nm according to the statistics in Figure 2g. In general, the SiNW diameter is determined by the leading In catalyst droplet, with $D_{nw} \sim fD_{In}$, as seen, for example, in Figure 2c, where the SiNWs fill in 70−80% of the concave tracks. Importantly, this parallel guided growth can be rather stable to produce ultralong and uniform SiNWs with length L_{nw} > 50 μm. Close examinations of the SiNWs grown over two of the bending corners, as shown in Figure 2d−f, reveal that all of the 10-layer SiNWs travel continuously with uniform diameters, as checked at two different places in Figure 2f and d, before and after growing over the two turning corners.

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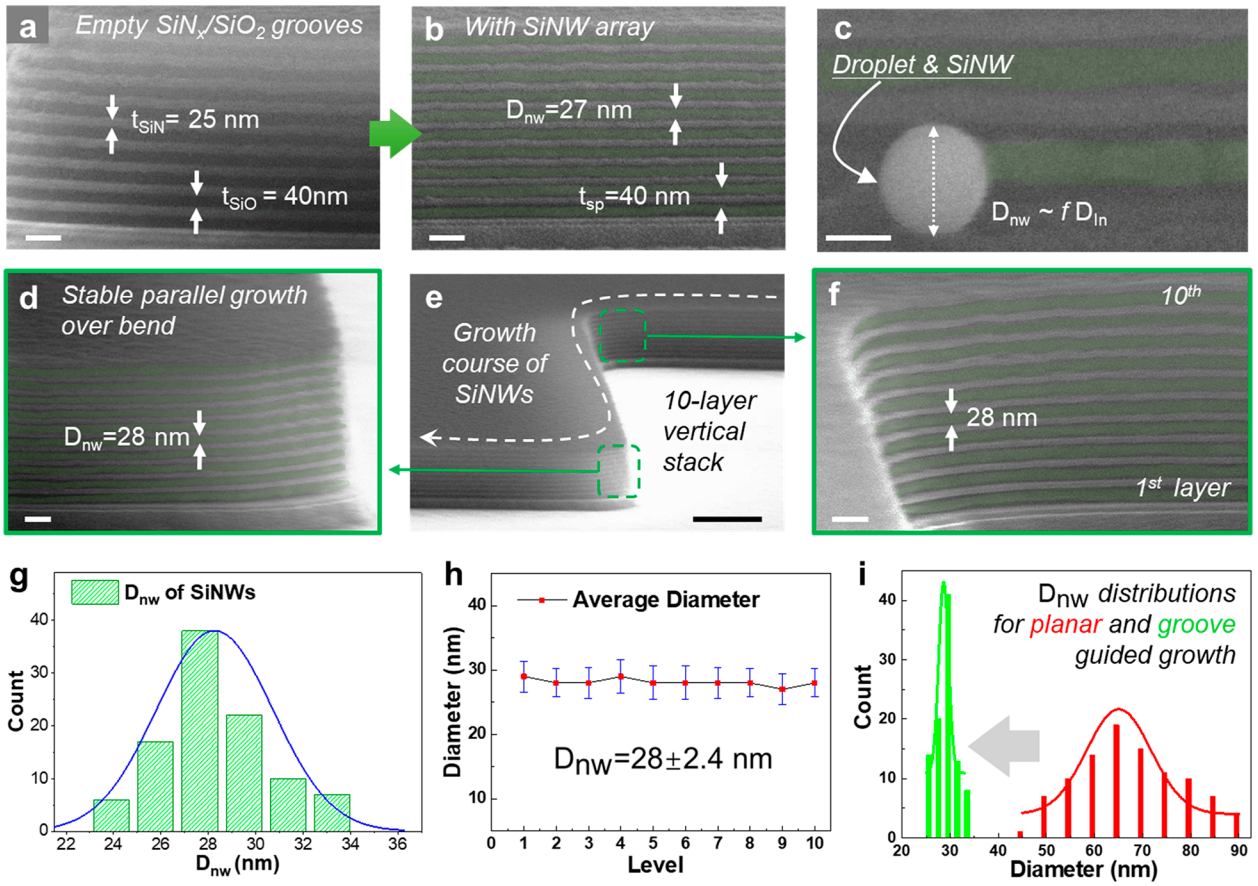

Figure 2. Morphology and statistics of 10-layer stacked SiNWs. (a) Typical SEM image of the empty sidewall grooves. (b) The side-view SEM image of 10-layer stacked SiNWs. (c) The SiNW led by In catalyst droplets, where D_{nw} is proportional to D_{In}. (d–f) The continuous growth of SiNWs over turning corners. (g–i) Statistics on diameters of SiNWs grown via PSG and planar growth. The scale bars in parts a, b, d, and f are for 100 nm, that in part c is for 50 nm, and that in part e is for 1 μm.

Taking the bottom layer as the first level, as marked in Figure 2f, the SiNW diameter variations at different levels are extracted and plotted in Figure 2h, indicating rather uniform diameter dispersion even among the SiNWs grown at different levels. In comparison, the SiNWs grown along the guiding step edges on the planar surface (Figure 3i) with similar parameters demonstrate a much larger diameter variation of $D_{nw}^{planar} \sim 66 \pm 11$ nm, which is almost 5 times wider than that observed for the groove-tailored growth of SiNWs (Figure 2i). This striking uniformity improvement, as well as the largely improved diameter and spacing control, implicates a unique *groove-tailored* growth mechanism that has not been explored or understood so far.

The key to achieving a uniform growth of SiNWs is to produce uniform In droplets that match the guiding grooves. Parts a and b of Figure 3 show the SEM images of the In droplets formed on the different sidewall grooves, prior to H_2 plasma treatment. In comparison, the In droplets formed on flat surfaces, with the same EBE evaporation of In catalyst, are much larger with a wider size dispersion, as seen in Figure 3c and Figure S1a and b for the cases upon planar SiO_2 and SiN_x surfaces, respectively. Close scrutiny on the sidewall grooves reveals that there are two distinct populations of the In droplets, that is, the smaller ones residing over the protruding SiN_x edges and the relatively larger ones sitting within the concave SiO_2 grooves. Statistics of the groove-sitting (light green) and the edge-residing (dark green) droplets on the **Type-I** grooves, with t_{SiO} = 40 nm and t_{SiN} = 25 nm (as seen in Figure 3a) are provided in Figure 3j, which are compared to the In droplet size dispersion found on the planar surface (the red columns, for SEM in Figure 3c). The mean diameters of the larger/smaller In droplets in the grooves/on the edges are around $D_{In}^{gr} \sim 38$ nm ($D_{In}^{edge} \sim 18$ nm), which are both much smaller than the typical sizes of the leading In droplets found at the end of the SiNWs on the sidewall, typically of $D_{In}^{planar} \sim 80$ nm (see, for instance, in Figure 2c). As the following H_2 plasma treatment used in this work was rather mild (with a rather low RF power and at low temperature), it will reduce only the In_2O_3 layer on the droplets, without causing a significant redistribution of the In droplets, as witnessed in Figure S2. Therefore, the smaller In droplets must have merged into large ones, after the a-Si coating and during the initial kicking off growth of SiNWs at the beginning of the annealing step.

In comparison, for the In droplets formed on the **Type-II** grooves, with the same SiO_2 layer but a wider SiN_x layer of 45 nm, the edge-riding droplets become larger but with a wider size dispersion, as seen in the statistics shown in Figure 3k, while the groove-sitting droplets seem to shrink in size (see the statistics in Figure S3). The consequence of the different groove designs on the growth of SiNWs is quite significant, as seen for comparison in the SEM images presented in Figure 3g and h, where the diameter uniformity degrades substantially for the SiNWs grown within the **Type-II** grooves with wider

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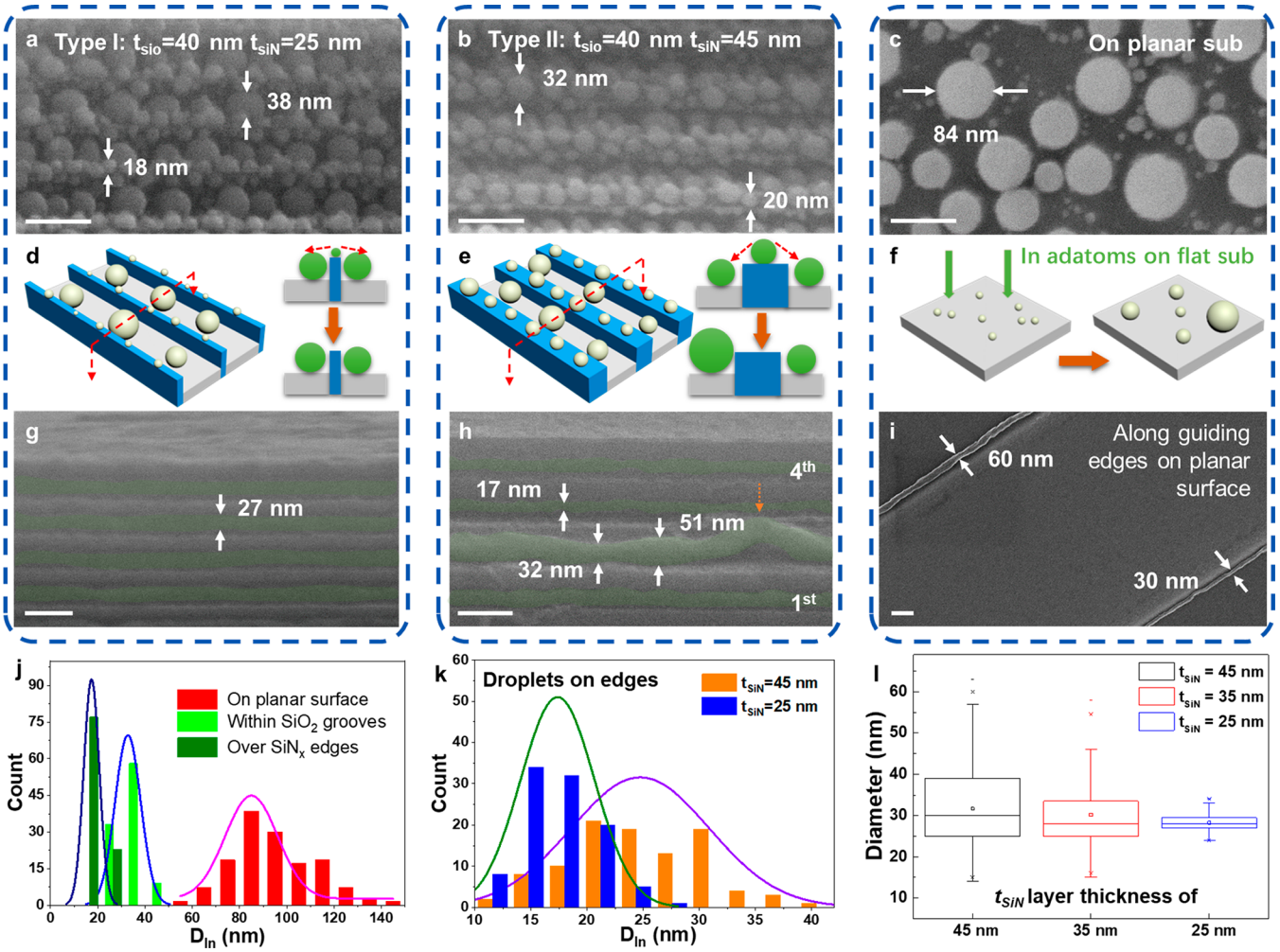

Figure 3. (a–c) Typical SEM images of In droplets on the sidewall or on the planar, while the corresponding models for droplets merging during the annealing process are illustrated in parts d–f. (g–i) SEM images of SiNWs grown with different nitride edges or on the planar. (j–l) Statistics on In droplet size and the diameter of SiNWs. The scale bars in parts a, b, c, g, and h are for 100 nm, and that in part i is for 200 nm.

nitride edge layers, with rather thick SiNWs of $D_{nw} \sim 51$ nm found side by side with the much thinner ones of $D_{nw} \sim 17$ nm in the neighborhood. The prominent impact of the nitride edge thickness can also be inferred from the statistics presented in Figure 3l, which highlight a clear trend that, with the increase of t_{SiN} = 25 to 35 nm (not shown here) and then to 45 nm, the diameter uniformity of the as-grown SiNWs degrades quickly.

Even with the same groove design, the In layer thickness also has a prominent influence on the geometry and uniformity of the SiNWs. For the case of a too thin In layer, with a nominal thickness of t_{In} = 20 nm, very thin SiNWs were produced in the grooves (see Figure 4a), which fill only a small portion <50% of the guiding tracks and demonstrate a larger diameter fluctuation, varying from 20 to 50 nm along the SiNWs. To the opposite situation of a too thick In layer with t_{In} = 40 nm, the larger In droplets seem to have more of a chance to touch their neighbors, across the nitride edges, to merge into even larger droplets, leading to much thicker SiNWs with D_{nw} > 60 nm separated by empty tracks in between, as seen in Figure 4e and depicted schematically in Figure 4f. Even for the somehow *matched* In layer thickness and groove sizes, as seen in Figure 4b, the separate SiNWs grown in neighbor grooves demonstrate an intriguing anticorrelated diameter variation, as inferred from the extracted diameter changes for two neighboring SiNWs shown in Figure 4d, which arises most likely from a dynamic competition for the available a-Si supply coated on the shared SiN_x edge lines.

To examine the crystallinity of the sidewall grown SiNWs, a cross-section slice of the 10-layer stacked array was cut by using focused ion beam milling and then characterized by high-resolution transmission electron microscopy (HR-TEM). As shown in Figure 5a, the SiNWs pseudocolored in green are found within the concave SiO_2 grooves, covered by a platinum (Pt) protection layer and separated by thin SiN_x edges. Close HR-TEM examinations (Figure 5b,c) reveal that the SiNWs are mostly ellipsoidal in cross section, with a shorter height of $H_{nw} \sim 14$ nm and a wider width of $D_{nw} \sim \frac{3}{2}H_{nw}$ (measured as diameter in the side-view SEM image), as well as a crystalline lattice with clear fringes spacing of d = 3.14 Å, corresponding to that of the Si(111) planes, and a growth direction being along Si⟨1$\underline{1}$0⟩, according to the diffraction patterns presented inFigure 5d.

In order to testify the electronic transport properties of the SiNW array, a simple but convenient top-gate FET configuration is fabricated, where, after depositing Ti/Au electrode contacts to the SiNWs on the sidewall groove by using tilted EBE evaporation, a 25 nm SiN_x dielectric layer was

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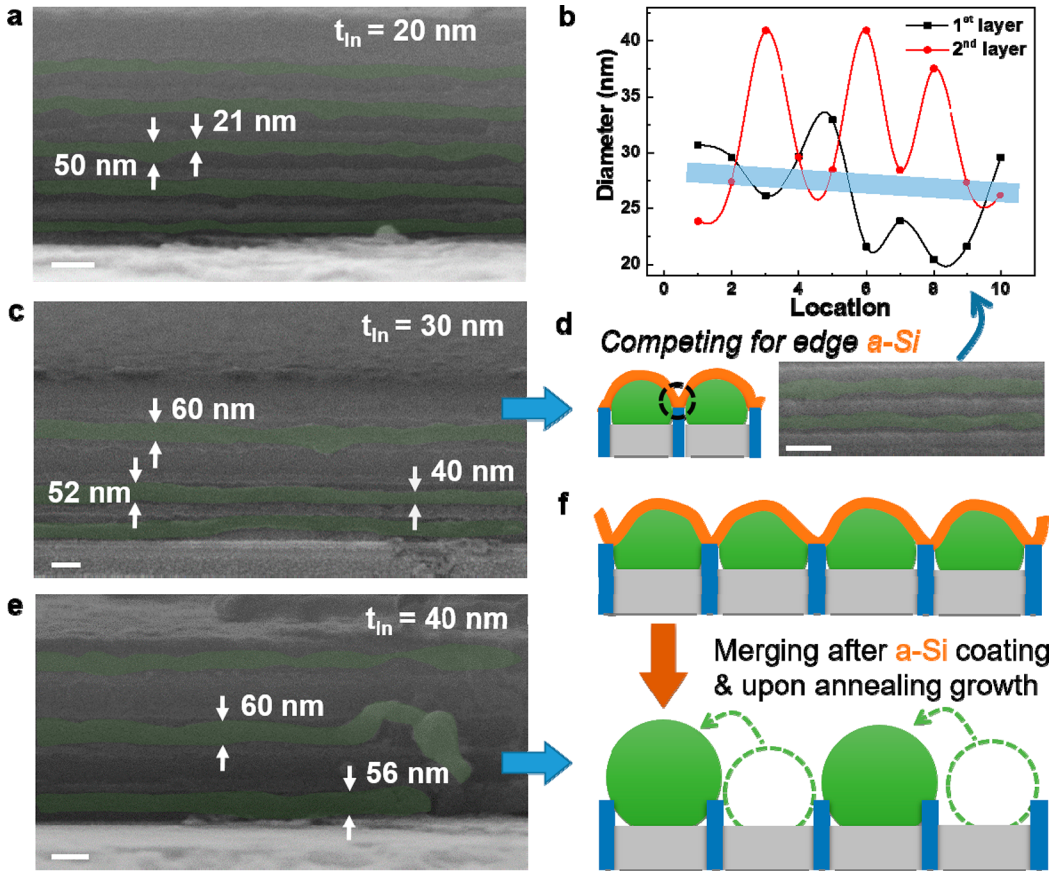

Figure 4. (a, c, e) Typical SEM image of SiNWs grown out of different In layer thicknesses. (b) Diameter variation statistics along two neighbor SiNWs, with the SEM image and schematic model depicted in part d. (f) The model for the In droplets merging during the annealing growth. The scale bars in parts a, c, d, and e are all for 100 nm.

deposited followed by the preparation of aluminum top-gate electrodes. The transfer properties are presented in Figure 5e, which indicates a typical p-type channel behavior (in a junctionless FET configuration) arising from the incorporation of In atoms into the SiNWs during the IPSLS growth that can serve as a p-type dopant in the SiNWs.[33] Despite an imperfect Schottky contact between the SiNW and electrodes, as inferred from the output curves in Figure 5f, a high on/off ratio $>10^7$ can be achieved with a reasonable subthreshold slope of 153 mV/dec. It should be noted that the actual electric performance of the SiNW channels should be evaluated in a complete GAA configuration, with conformal high-k dielectric layer and poly-Si gating medium, which will be explored in the future works.

As established in surface diffusion and nucleation theory,[34−36] the In atoms landing on the substrate surface during EBE evaporation will diffuse randomly until they run into each other to form larger immobile nuclei. Then, the islands continue to expand by collecting the nearby In atoms landing in the proximity zones, that is, the region that measures a diffusion length $\sim\lambda_{In}$ apart from the droplet. During the initial island-growth stage, prior to the formation of a continuous layer, the diffusion length can be roughly estimated by $\lambda_{In} \sim L_{sep}/2 = N_{In}^{-1/2}/2$, where L_{sep} and N_{In} are the average separation among the In droplets and their density, respectively. According to the droplet SEM shown in Figure S1, the diffusion lengths of In atoms on the planar SiO_2 and SiN_x surfaces can be estimated to be $\lambda_{In\_SiO} \sim 31$ nm and $\lambda_{In\_SiN} \sim 24$ nm, respectively, corresponding to an interdroplet separation much larger than the groove or edge widths, $\bar{L}_{sep} = 2\lambda_{In\_SiO} > t_{SiO}$ and $2\lambda_{In\_SiN} > t_{SiN}$.

In a simplified but heuristic picture, the expansion of the droplet can be related to the amount of In influx (F_{In}) received on the collection zones over a duration of t and written as

$$D_{In}^{\ 3} \sim S_{col}F_{In}t, \quad \text{with} \quad S_{col} \sim \bar{L}_{sep}^{\ 2} = 4\lambda_{In}^{\ 2} \tag{1}$$

In reality, there are always random fluctuations on the interdroplet separation, that is, $L_{sep} = 2\lambda_{In} + \Delta l$, which thus induces the diameter fluctuation of the droplets. For the catalyst droplets formed on a planar surface, the relative fluctuation amplitude is

$$A_{In}^{2D} \equiv \Delta D_{In}^{\ 3}/D_{In}^{\ 3} = \frac{(2\lambda_{In} + \Delta l)^2 - 4\lambda_{In}^{\ 2}}{4\lambda_{In}^{\ 2}} \sim \Delta l/\lambda_{In}, \quad \text{with} \quad \Delta l \ll \lambda_{In} \tag{2}$$

In comparison, for the droplet formed on sidewall grooves, the diffusion of In atoms over the protruding SiN_x edges (to go into the neighbor track) is greatly suppressed, and thus, the collection zone area is modified to $S_{In}^{gr} = t_{SiO}2\lambda_{In}$, with $2\lambda_{In} > t_{SiO}$. Now, the fluctuation amplitude becomes

$$A_{In}^{gr} = \frac{t_{SiO}(2\lambda_{In} + \Delta l) - t_{SiO}2\lambda_{In}}{t_{SiO}2\lambda_{In}} \sim \frac{\Delta l}{2\lambda_{In}} = A_{In}^{2D}/2 \tag{3}$$

In other words, the In droplet confined in the 1D grooves suffers less size fluctuation than those encountered on a planar

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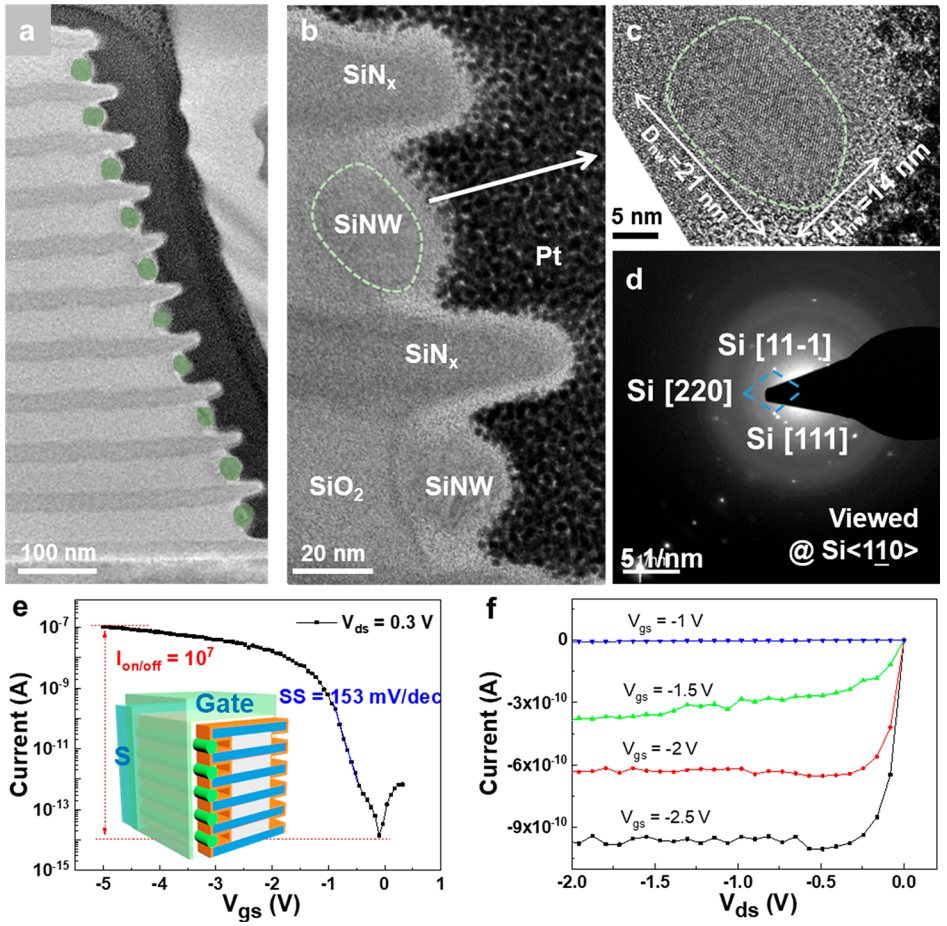

Figure 5. (a–c) High-resolution transmission electron microscopy characterizations of the cross section of the 10-layer SiNW stacks. (d) The electron diffraction pattern of the SiNW. (e, f) The typical transfer curve and the output curve of the prototype FET fabricated upon the sidewall-grown SiNWs.

Table 1. Comparison of the 3D Geometry Uniformity of Stacked SiNWs in the Literature

fabrication	size control by	stacked layers	av. D_{nw} (nm)	D_{nw} deviation	NW-to-NW spacing (nm)	temperature (°C)	ref
Si/SiGe etching	EBL	2	8	8.7%[a]	10	750	37
Si/SiGe etching	EBL	3	11	14.8%[a]	13	700	38
Si/SiGe etching	EBL	13	14 (top), 30 (bottom)	18.4%[a]	35	700	39
Bosch etching	EBL	5	37 (top), 50 (bottom)	17.6%[a]	70	900	40
VLS growth	sol–gel particles	1	6.4	18.7%	random	440	1
VLS growth	PS template	1	90	10.4%	~200	850	32
IPSLS growth	random droplets	4	114	23.7%	130	350	25
IPSLS growth	random droplets	4	40	20.5%	90	350	2
IPSLS growth	groove-tailored droplets	10	28	8.7%	40	350	this work

[a]Extracted from the disclosed SEM or TEM images in the papers.

surface, at least during the early discrete nucleation-expansion stage. On the other hand, the separating SiN_x edges can also prohibit the merging of In droplets in neighboring grooves (during their initial expansion), which is also very important to reduce the size fluctuation arising from random merging of In droplets (as happens more often on the 2D surface) and thus helps to achieve a narrower droplet size dispersion within the grooves.

Furthermore, as all of the In droplets will finally move within the concave SiO_2 tracks, instead of along the convex SiN_x edges, to lead a guided growth of SiNWs, the edge-residing droplets will have to merge with the nearby groove-sitting droplets during the initial kicking off growth, after a-Si coating and upon annealing. As the chance to tilt left or right is random, this merging process will induce size variation for the leading In droplets that adds to the diameter fluctuation of as-grown SiNWs. Therefore, with a wider SiN_x edge layer design (Figure 3b) and thus larger edge-riding In droplets, SiNWs with much larger diameter fluctuation are observed (Figure 3h), in strong contrast to the far more uniform SiNW growth with thinner SiN_x edge design (see Figure 2 and Figure 3g). Therefore, the SiN_x edge width should be minimized, while preserving a stable nanoedge structure to separate/confine the catalyst formation and growth within the grooves.

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Indeed, the groove-tailored ultrauniform growth of stacked SiNWs enables an unprecedented high-precision 3D fabrication and integration capability, which has never been accomplished before via *bottom-up* approaches, for example, compared to the VLS growth of SiNWs with or without template-assisted catalyst patterning (see the fifth and sixth entries in Table 1[1,32]), and our previous works[25,26] (see the seventh and eighth entries), that suffer a much larger diameter fluctuation, poorer geometry, and lower density controls. In several critical aspects, such as the stacking number, channel level uniformity, and fabrication efficiency/cost, it has even apparent advantages over the *start-of-the-art* stacked SiNW channel structures fabricated via *top-down* Si/SiGe multilayer buffered[37−39] and Bosch[40] etching technologies, as shown in Table 1, which require high-temperature epitaxial growth of Si/SiGe multilayers (>500 °C) or oxidation thinning (>900 °C) after Bosch etching, with large channel diameter variation, from the top to the bottom levels, that are typically ∼18% for stacking layers of greater than three layers,[39] except for that of the carefully controlled two-layer stacked channels of ∼8.7%.[37] In comparison, the groove-tailored 3D SiNWs are produced via a single-run parallel growth at only 350 °C, achieving a record (but not the limit) high stacking number of 10, which has never been accomplished via a high-yield bottom-up approach.

CONCLUSION

An unexpected uniform and high-density growth integration of an ultrathin 3D SiNW array has been accomplished, for the first time, where the sidewall grooves can suppress substantially the random diffusion and merging of catalyst droplets and regulate a rather stable sidewall guided growth of SiNWs with a uniform diameter of D_{nw} = 28 ± 2.4 nm and spacing of only t_{sp} = 40 nm. This high-precision 3D groove-tailored growth strategy represents indeed a new landmark of bottom-up catalytic growth to stand out as a new competitive/or even advantageous 3D fabrication and integration technology.

EXPERIMENTAL SECTION

Sidewall Groove Formation. First, the glass substrate or c-Si wafer was cleaned by acetone, ethanol, and deionized water in an ultrasonic cleaning machine, respectively. Then, the sample was sent into the PECVD system for the multilayer deposition at 300 °C. A SiN_x layer was deposited with a mixed gas of 100 sccm of SiH_4, 6 sccm of NH_3, and 100 sccm of N_2 at RF of 40 W and pressure of 80 Pa, while a SiO_2 layer was deposited with a mixed gas of 80 sccm of SiH_4, 120 sccm of N_2O, and 40 sccm of N_2 at RF of 10 W and pressure of 100 Pa. Two kinds of film were deposited alternately in the same system. Third, lithography was conducted with photoresist AZ 5214, followed by C_4F_8 plasma etching in the inductively coupled plasma (ICP) system to expose the sidewall. After that, the sample was immersed into 0.5% HF solution for 15 s to selectively etch the SiO_2 layers and form the grooves on the sidewall. The layers of grooves can be easily tuned by the deposition cycle, and the thickness of SiN_x/SiO_2 layers can be adjusted by the duration of deposition.

SiNW Fabrication. At the end of the sidewall, the region for the In catalyst was patterned by lithography, followed by EBE evaporation and lift-off procedure by acetone. In order to deposit In in the sidewall grooves, the sample was tilted by 60° during the evaporation. The discrete In droplets were formed both in the grooves and on the SiN_x edges for all layers. In the following step, the sample was loaded into the PECVD system for H_2 plasma treatment at 250 °C, a pressure of 140 Pa, and a radio frequency (RF) power of 10 W to remove the oxide layer of In droplets. After that, a-Si thin film as precursor was deposited at 100 °C by pure silane plasma at a RF power of 2 W and a pressure of 20 Pa. Finally, the growth was activated in a vacuum at 350 °C where the In catalyst droplets in the grooves and the ones on the SiN_x edges tend to merge and form bigger droplets and start to absorb the nearby precursor and move along the grooves to form c-Si nanowires. Due to the existence of a SiN_x layer, the movement was constrained in its own groove. And the remnant a-Si was etched by H_2 plasma at 150 °C, a RF power of 20 W, and a pressure of 140 Pa.

Top-Gate FET Fabrication and Electrical Measurement. Upon the five layers of stacked SiNWs on the sidewall, lithography was patterned to define a source-drain region. Before Ti/Au (8 nm/92 nm) electrode deposition using the EBE system, the oxide layer of SiNWs was removed by 4% HF solution. During the deposition, the sample was tilted by 60° for better coverage. After that, the SiN_x layer of 25 nm, serving as a dielectric layer, was deposited, followed by 120 nm Al evaporation as a top-gate electrode. The electrical measurement was conducted using a Keithley 2636B instrument at room temperature.

ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge at https://pubs.acs.org/doi/10.1021/acs.nanolett.0c02950.

Figure S1, SEM images and catalyst size distribution statistics of the In droplets deposited via EBE evaporation upon the (a) SiO_2 and (b) SiN_x substrates; Figure S2, SEM images of the In droplets evaporated on the hetero-SiO_2/SiN_x sidewall grooves before and after H_2 plasma treatment, respectively; Figure S3, statistics on the diameter distributions of the In droplets formed in the grooves with different SiN_x edge thicknesses (PDF)

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Notes

The authors declare no competing financial interest.

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