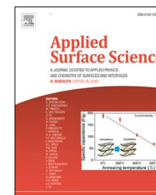
Applied Surface Science 718 (2026) 164889

Contents lists available at ScienceDirect

Applied Surface Science

journal homepage: www.elsevier.com/locate/apsusc



Full Length Article

In-plane growth control of uniform SiGe nanowires for thin film electronics

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ARTICLE INFO

Keywords:
Silicon-germanium nanowires
In-plane solid–liquid–solid
Composition control
Low-temperature growth
Field-effect transistor

ABSTRACT

The planar catalytic growth of highly ordered silicon nanowires (SiNWs) via an in-plane solid–liquid-–solid (IPSLS) mechanism represents a promising approach for the scalable fabrication of electronic and sensing devices over large areas. While alloying Si with Ge offers the potential for bandgap tuning and enhanced carrier mobility, the IPSLS-based synthesis of silicon–germanium nanowires (SiGeNWs) has remained relatively unexplored. In this work, we report the successful low-temperature (250 °C) growth of ultrathin $Si_{1-x}Ge_x$NWs using the IPSLS process, with varied composition from 0 to 75 at.%. Interestingly, the Ge composition in the alloy NWs is atomically uniform and can be precisely controlled by the Ge content in amorphous SiGe (a-SiGe) precursor layer. The resulting SiGeNWs exhibit uniform diameters (~35 nm) and can be organized into densely packed, well-aligned arrays, free of substrate-induced epitaxial strain as confirmed by Raman spectroscopy. All-low-temperature (<450 °C) field-effect transistors (FETs) fabricated using $Si_{0.7}Ge_{0.3}$NW channels demonstrate a improvement compared to baseline SiNW FETs, including an order-of-magnitude increase in on-current, increased hole mobility to 76 cm^2/V·s, an on/off current ratio ($I_{on}/I_{off} > 10^6$), and a subthreshold swing (SS = 135 mV/dec). These findings highlight the potential of IPSLS-grown SiGeNWs as ideal one-dimensional (1D) channels for future large-area thin-film and flexible electronics.

1. Introduction

Silicon-germanium nanowires (SiGeNWs), featuring tunable bandgaps, enhanced carrier mobility and full compatibility with mainstream crystalline silicon (c-Si) microelectronics, are promising candidates for future high-performance transistors [1–3], sensors [4], and optoelectronic devices [5–7]. Compared to top-down fabrication methods, such as electron beam lithography (EBL) or extreme ultraviolet (EUV) lithography, catalytic growth approaches like vapor–liquid–solid (VLS) [8,9] represent high-yield, low-temperature synthesis of SiGeNWs, with quasi-one-dimensional (1D) diameters <50 nm and without the need for high-quality wafer substrates [10–12]. Such features render the catalytic SiGeNWs particularly attractive for a wide range of large-area electronic applications, including thin-film transistors (TFTs) in flat-panel displays [13,14], flexible sensors [15,16], and logic circuits [17–19]. Furthermore, they also provide new avenues for advanced device architectures, such as monolithic three-dimensional integration and in-memory computing paradigms [20,21].

However, in the typical VLS catalytic approaches, the as-grown Si or SiGeNWs form randomly oriented vertical arrays or bundles standing on the substrate surface [22,23], which requires additional post-growth "pick-and-place" operations [24] to transfer them onto planar surfaces for subsequent device fabrication [25,26]. This has been a major hurdle for the scalable integration of catalytic NW-based electronics. To address this challenge, an in-plane solid–liquid-solid (IPSLS) growth mechanism [27] was established in our previous works, enabling the formation of well-aligned planar silicon nanowires (SiNWs) at designated locations, either on the substrate surface or along vertical sidewalls [28,29]. Although high-performance field-effect transistors (FETs) with well-positioned SiNW channels as narrow as 10 nm have been successfully demonstrated [30,31], the performance of SiNW-FET devices is still fundamentally limited by the relatively low hole carrier mobility in c-Si. Further device performance improvements require a new degree of control: the composition of the NWs.

It has been known that c-Ge has the highest hole carrier mobility of 1900 cm^2/V·s in all known semiconductors. Thus, incorporating Ge into SiNWs to form uniform crystalline SiGe alloys has the potential to enhance carrier mobility and provide a tunable bandgap suitable for near-infrared optoelectronic applications. However, the direct IPSLS growth of pure germanium nanowires (GeNWs) using amorphous germanium (a-Ge) as the precursor—replacing the amorphous silicon (a-Si) used in SiNW IPSLS growth—has been found to be unstable (as

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https://doi.org/10.1016/j.apsusc.2025.164889
Received 22 July 2025; Received in revised form 27 September 2025; Accepted 11 October 2025
Available online 13 October 2025
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discussed later). Therefore, a more practical strategy is to gradually increase the Ge content in the amorphous SiGe (a-SiGe) precursor layer, to examine whether this enables more stable IPSLS growth of SiGeNWs, and to what extent.

In this work, we present a systematic study of the IPSLS growth of uniform SiGeNWs with gradually increasing Ge content, which has never been investigated before. We found that a stable guided growth of well-defined SiGeNWs can be achieved even at Ge contents as high as 75 %. Interestingly, the SiGeNWs are monocrystalline with uniform Si and Ge distribution, with the same Si/Ge ratio preset in the a-SiGe precursor films, controlled precisely by the SiH_4/GeH_4 ratio in the deposition gases. Notably, compared to the mainstream epitaxial growth of SiGe layer on c-Si wafer, which inevitably causes significant strain accumulation [32,33], the IPSLS-grown SiGeNWs are found to be free of substrate-induced epitaxial strain, as verified by Raman characteristics. Considering the p-type catalytic In atom doping in the SiGeNWs, All-low-temperature (<450 °C) FET devices were successfully fabricated based on $Si_{0.7}Ge_{0.3}$NW channels, which achieve a subthreshold swing (SS) of 135 mV/dec, an on/off current ratio (I_{on}/I_{off}) of $>10^6$, and a hole mobility of 76 $cm^2/V{\cdot}s$.

2. Experiments and methods

The IPSLS growth involves the following steps: First, the patterning of multi-steps guiding edges, as schematically depicted in Fig. 1b, with the height and width of each mini-steps controlled to be H ~ 100 nm and W ~ 100 nm, respectively, as witnessed in Fig. 1c. Details of the multi-step fabrication process are provided in Fig. S1; Second, In catalyst strips, with a norminal thickness of 8 nm and a width of 2 μm, were deposited at one ends of the multi-step guiding edges using photolithography, thermal evaporation, and standard lift-off processes; Third, the sample was placed in a PECVD system, and the In strips were treated at 250 °C with H_2 plasma to remove the oxide layer on the surface of the In strips and form discrete nanodrops, with a hydrogen flow rate of 50 sccm, a pressure of 130 Pa, and a RF power of 35 W. Then, an a-$Si_{1-x}Ge_x$ precursor film was obtained at 100 °C by adjusting the gas flow ratio of SiH_4 and GeH_4. Taking $Si_{0.7}Ge_{0.3}$NW as an example, an a-$Si_{0.7}Ge_{0.3}$ film (15 nm) was deposited on the sample surface under the conditions of a SiH_4 flow rate of 2 sccm, a gas mixture of 5 % GeH_4 in 95 % H_2 at 4 sccm, a chamber pressure of 40 Pa, and an RF power of 10 W. Finally, the substrate temperature was increased to 250 °C and held in vacuum for 60 min. During this annealing process, molten In droplets move along the guiding edges and absorb the a-$Si_{0.7}Ge_{0.3}$ layer, producing crystalline $Si_{0.7}Ge_{0.3}$NW behind it.

Notably, the growth temperature of SiGeNWs is 100 °C lower than that of pure SiNWs, primarily due to the markedly higher solubility of Ge in In [34]. At 350 °C, the equilibrium solubility of Ge (~2.4 at.%) is nearly three orders of magnitude greater than that of Si (~3.2×10^{-3} at. %), and this difference further increases at higher temperatures [35,36]. Lowering the growth temperature helps narrow this solubility gap, which is crucial for achieving stable and compositionally uniform SiGeNW growth. However, when the Ge content exceeds 75 %, instability and even collapse of the catalytic In droplet are observed, resulting in irregular NW morphology and composition (Fig. S2a). Fig. S2b reveals a collapsed In droplet region, where the liquid metal spreads laterally and loses its spherical morphology. A short and distorted $Si_{0.15}Ge_{0.85}$NW segment can be observed adjacent to the collapsed droplet. This collapse is driven by the significantly increased solubility and fast diffusion of Ge in In at high Ge fractions, which accelerates the incorporation of Ge atoms and results in rapid nanowire growth. The unstable catalyst droplet quickly mixes with the amorphous precursor layer, producing only short (<1 μm) and morphologically irregular NWs. Fig. 1d shows the $Si_{0.7}Ge_{0.3}$NWs, highlighted in blue pseudo-color, neatly arranged along the steps with uniform spacing and a mean diameter of $D_{nw} = 34.4 \pm 4.7$ nm, as indicated in Fig. 1e. The spacing between the NWs matches the pre-designed step width ($W_{nw} \approx W = 100$ nm). The self-assembled growth of SiGeNWs can be guided into dense arrays without relying on high-precision lithography.

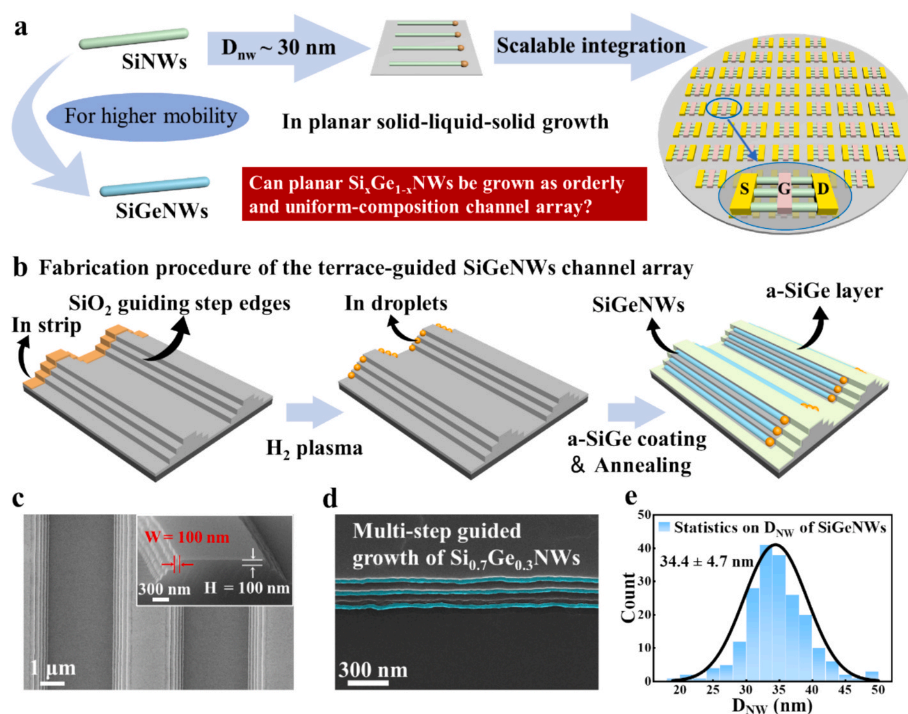

Fig. 1. (a) The IPSLS mechanism provides an effective strategy for integrating NW devices into planar structures. (b) Schematic illustration of the synthetic process for high-density terrace-guided SiGeNWs in a PECVD system. (c) The top-view and side-view SEM images of the as-produced oblique sidewall terraces. (d) SEM images of the SiGeNWs grown along the dense sidewall terraces. (e) A statistical analysis of the diameter of SiGeNWs grown on the oblique sidewall terraces.

3. Results

3.1. Structural and compositional characterizations

The structural quality, compositional homogeneity, and residue strain of the as-grown $Si_{1-x}Ge_x$NWs were evaluated by using high-resolution transmission electron microscopy (HR-TEM), scanning transmission electron microscopy coupled with energy-dispersive X-ray spectroscopy (STEM-EDS), and Raman spectroscopy. The elemental mappings from EDS (Fig. 2b,d,f) reveal rather uniform distributions of the Si and Ge atoms in all NWs, confirming the formation of a substitutional solid solution without any detectable phase segregation. Notably, the In concentration rises with increasing Ge content. Specifically, In concentrations increase from 0.07 at.%, 0.18 at.%, to 0.47 at.% for the $Si_{0.9}Ge_{0.1}$NWs, $Si_{0.7}Ge_{0.3}$NWs, and $Si_{0.5}Ge_{0.5}$NWs, respectively, as shown in Fig. 2g. These In concentrations substantially exceed the solid solubility limit of In in $Si_{0.5}Ge_{0.5}$ alloys (0.02–0.06 at.%) [37], indicating a strong In-doping enabled by the IPSLS growth mechanism. On for the highest Ge composition of 50 %, slight precipitations of In atoms are observed in the marked regions by white circles in Fig. 2f. A previously reported dimer-atom insertion kinetic model was proposed to explain the incorporation of In into NWs, revealing that In incorporation can exceed its equilibrium solubility by one to two orders of magnitude [38]. The observed In segregation in $Si_{0.5}Ge_{0.5}$NWs is primarily driven by the supersaturated state established during the rapid growth process. According to the HR-TEM and STEM-EDS analysis of $Si_{0.9}Ge_{0.1}$NWs, $Si_{0.7}Ge_{0.3}$NWs, and $Si_{0.5}Ge_{0.5}$NWs in Fig. 2a–f, these alloyed SiGeNWs are all monocrystalline with well-defined lattice fringes and corresponding interplanar spacings of ~1.96 Å, ~3.19 Å, and ~3.23 Å, for those of (220), (111), and (111) planes, respectively. To ensure the accuracy of the TEM calibration, we further characterized SiNWs as a reference standard (Fig. S3), whose measured (111) lattice spacing is close to the standard value of Si (111) (~3.14 Å). In addition, another $Si_{0.5}Ge_{0.5}$NW sample was characterized at three different positions (Fig. S4), giving (111) lattice spacings of 3.21–3.26 Å.

Raman spectroscopy provides insights into the vibrational modes and strain within the SiGeNWs. As shown in Fig. 3a, the Raman spectra of $Si_{1-x}Ge_x$NWs with Ge contents ranging from 0 to 75 at.% exhibit three prominent optical phonon modes: the Ge–Ge LO–TO phonon modes (265–295 cm^{-1}), the Si-Ge vibrational band (400–410 cm^{-1}), and the Si-Si phonon modes (464–512 cm^{-1})[39]. Their intensities and frequencies vary systematically with composition. At $x = 0.5$, the Si–Ge mode dominates, while both Si–Si and Ge–Ge modes are also clearly visible, indicating the coexistence of all three bond types in a random alloy structure. Furthermore, the Raman peak positions exhibit composition-dependent shifts (Fig. 3b–d). Specifically, the Si–Si mode frequency decreases, while the Ge–Ge mode frequency increases with higher Ge content. The Si–Ge mode frequency exhibits a bell-shaped dependence, peaking near 50 % Ge content, which aligns with the maximized formation of Si–Ge heteronuclear bonds due to the balanced Si and Ge atomic ratio.

To further evaluate the strain state of the nanowires, the measured Raman peak positions of the Si–Si, Si–Ge, and Ge–Ge modes were compared with the theoretical curves for unstrained SiGe alloys (Refs. [40,41]), as shown in Fig. 3b–d. The Si–Si mode in the Si-rich regime ($x \leq 0.5$) and the Ge–Ge mode in the Ge-rich regime ($x \geq 0.4$) show excellent agreement with the theoretical unstrained values, with deviations typically within ~2–3 cm^{-1}. Larger deviations (~10–20 cm^{-1}) are observed for the Ge–Ge mode at low Ge contents ($x \approx 0.1$–0.3) and for the Si–Si mode at high Ge contents ($x \approx 0.6$–0.75). These points, affected by weak peak intensity and background interference, are highlighted by black ellipses in panels (b) and (c). Rath et al. [41] demonstrated that weak Ge–Ge peaks in the low Ge regime are strongly influenced by the quasi-amorphous background, which results in uncertainties in peak extraction. Alonso and Winer [42] reported localized Si–Si vibrational modes in the 420–470 cm^{-1} range (marked by a red arrow in Fig. 3a), which can overlap with and interfere in the extraction of the main Si–Si peak at high Ge contents. In our experiments, the laser spot (~a few microns) is much larger than the NW diameter (~tens of nanometers), so the collected Raman signal inevitably includes contributions from both the crystalline SiGeNW and the surrounding a-SiGe film. The broad background from the a-SiGe film especially affects weak Raman modes, thereby amplifying uncertainties in peak fitting. Importantly, Lu et al. [39] showed that SiGeNWs with diameters larger than ~10 nm does not exhibit significant phonon confinement effects, confirming that the observed deviations are caused by weak-peak and

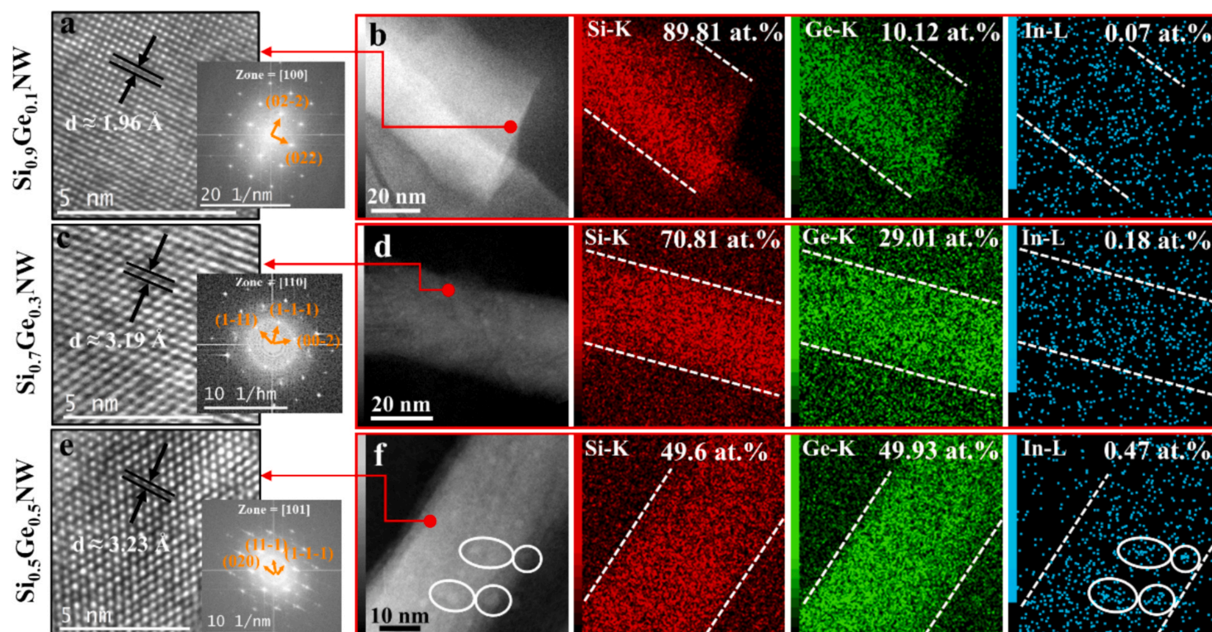

Fig. 2. (b), (d) and (f) show the STEM image and EDS elemental mappings of $Si_{0.9}Ge_{0.1}$NW, $Si_{0.7}Ge_{0.3}$NW and $Si_{0.5}Ge_{0.5}$NW, respectively, where the Si, Ge and In elemental mappings are shown in red, green and blue, respectively. (a), (c) and (e) show the HR-TEM images taken at the red-circled areas in (b), (d) and (f), respectively, with the corresponding Fourier transform as an inset.

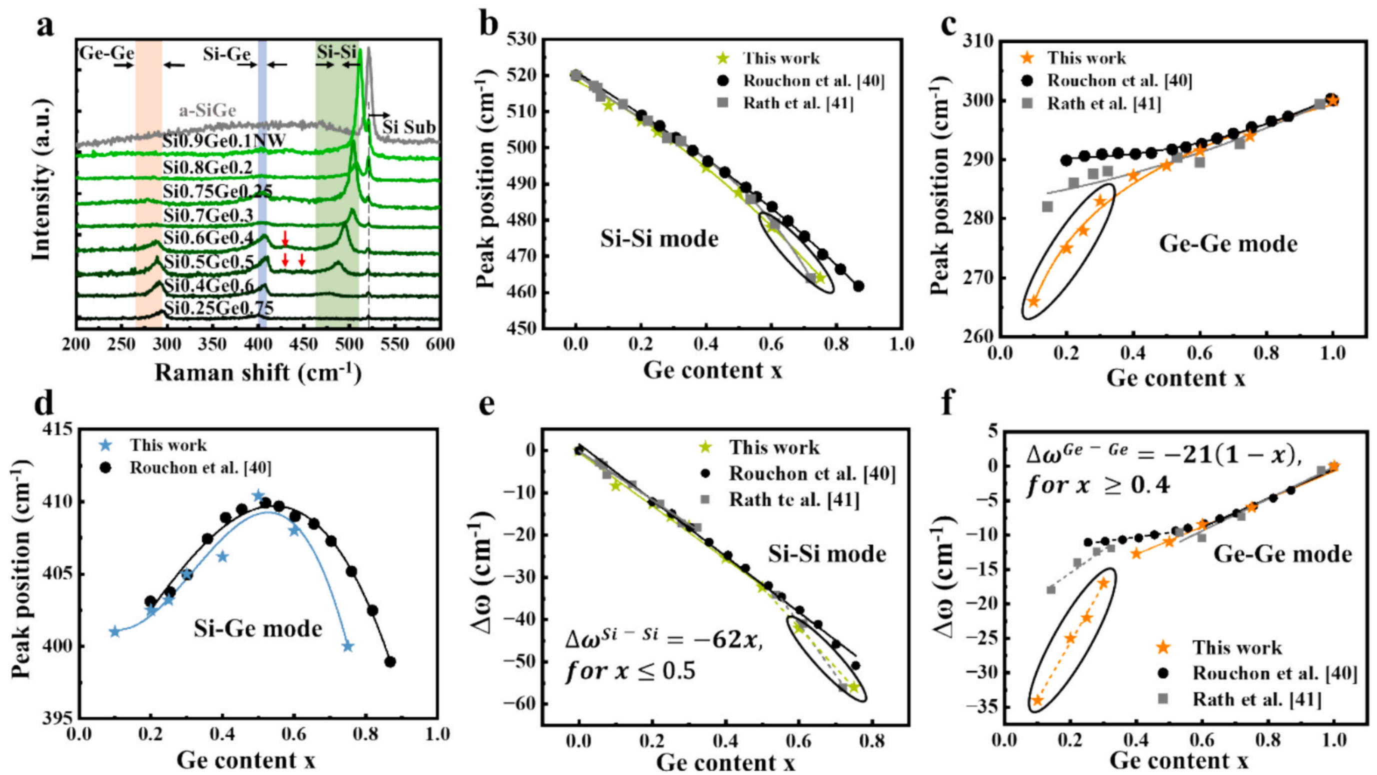

Fig. 3. (a) Raman spectra of IPSLS-grown $Si_{1-x}Ge_x$NWs with different Ge contents. (b–d) Raman peak positions of the Si–Si, Si–Ge, and Ge–Ge modes as a function of Ge content, compared with the theoretical unstrained alloy curves from the literature [40,41]. (e and f) Frequency shifts $\Delta\omega_{exp}$ of the Si–Si and Ge–Ge modes relative to the theoretical values. The Si–Si mode in the Si-rich regime ($x \le 0.5$) and the Ge–Ge mode in the Ge-rich regime ($x \ge 0.4$) follow the unstrained curves closely, while larger deviations are observed for the Ge–Ge mode at low Ge contents ($x \approx 0.1$–0.3) and the Si–Si mode at high Ge contents ($x \approx 0.6$–0.75). These points, affected by weak peak intensity and background interference, are highlighted by black ellipses.

background interference rather than residual strain. To ensure robust analysis, we fitted Δω using the Si–Si mode in the Si-rich regime and the Ge–Ge mode in the Ge-rich regime. The frequency shift of the Si–Si mode follows a quasi-linear relationship in the Si-rich regime ($x \le 0.5$), expressed as $\Delta\omega^{Si-Si} = -62x$, $\varepsilon_r = 0$ (Fig. 3e). Similarly, for the Ge–Ge mode in the Ge-rich regime ($x \ge 0.4$), the shift can be described by $\Delta\omega^{Ge-Ge} = -21(1-x)$ for $x \ge 0.4$ (Fig. 3f). These linear frequency trends originate from systematic changes in bond lengths [40], confirming that the SiGeNWs grown by the IPSLS mechanism are free of substrate-induced epitaxial strain.

The chemical composition of a-$Si_{1-x}Ge_x$ precursor films was also analyzed using X-ray photoelectron spectroscopy (XPS). The binding energy (E_b) was calibrated with reference to the C 1s spectra at 284 eV obtained from the surface of a-SiGe films. As shown in Fig. S5a, the XPS spectra of the a-$Si_{1-x}Ge_x$ films exhibit Ge 3d peaks (29 eV) and Si 2p peaks (99 eV). Si–O peaks at approximately 532 eV (not shown) and 103 eV in the Si 2p region are attributed to the presence of atmospheric oxygen. Analysis confirmed that the composition of the NWs matches that of the initial a-SiGe precursor film. The composition of the a-$Si_{1-x}Ge_x$ precursor thin films is directly correlated with the SiH_4/GeH_4 gas flow ratio. Varying this ratio allows precise control over the Si and Ge content in the deposited films, as demonstrated in Fig. S5b.

3.2. Electrical Properties of SiGeNW FETs

In addition, we measured the resistivity of $Si_{1-x}Ge_x$NWs with a

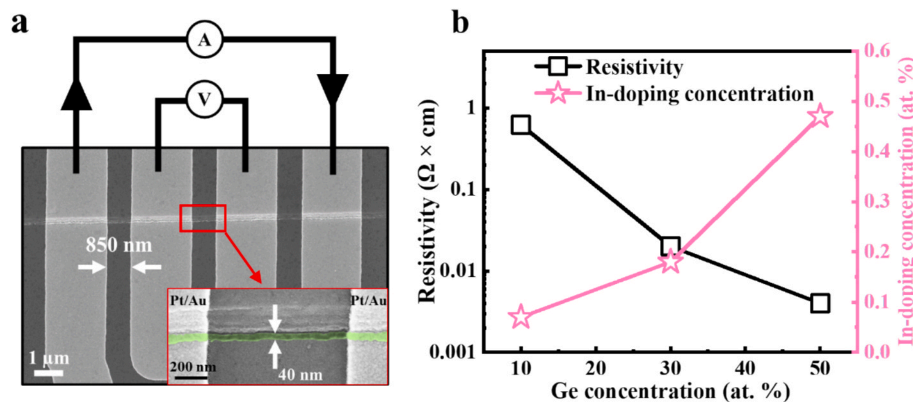

Fig. 4. (a) Schematic diagram and SEM image of the four-point probes measurement, with the inset being an enlarged SEM image of SiGeNW marked in the red box. (b) Dependence ofresistivity and In-doping concentration on the Ge fraction.

diameter of 40 nm using a four-point probe configuration, as shown in Fig. 4a. Equidistant electrodes (850 nm apart) were patterned on a single $Si_{1-x}Ge_xNW$ using electron beam lithography (EBL). For the as-grown $Si_{0.9}Ge_{0.1}NW$, $Si_{0.7}Ge_{0.3}NW$, and $Si_{0.5}Ge_{0.5}NW$, the measured electrical resistivity (ρ) was approximately 0.62 Ω·cm, 0.02 Ω·cm, and 0.004 Ω·cm, respectively, as depicted in Fig. S6. The correlation between resistivity and In-doping concentrations, relative to the Ge fraction, is shown in Fig. 4b. The electrically active fraction of implanted In atoms increases with the Ge fraction in the $Si_{1-x}Ge_xNW$, owing to the rise in In solid solubility. This relationship is demonstrated by the observed decrease in resistivity as the In-doping concentration increases.

To validate the electrical performance of our high-density SiGeNW arrays, we fabricated FET devices using SiNW, $Si_{0.9}Ge_{0.1}NW$, $Si_{0.7}Ge_{0.3}NW$, and $Si_{0.5}Ge_{0.5}NW$ as active channel materials with a channel length (L_{ch}) of 3 μm, as illustrated in Fig. 5a. The details of the fabrication process and operating principle of the $Si_{1-x}Ge_xNW$ FET are provided in Fig. S7. As shown in Fig. 5b, compared to SiNW FETs, the on-current of the FET increases with increasing Ge content. For example, the on-current of $Si_{0.7}Ge_{0.3}NW$ FET increases by one order of magnitude, and the on-current of $Si_{0.5}Ge_{0.5}NW$ FET increases by two orders of magnitude. However, as the Ge content increases, the gate control over the channel weakens, particularly in the case of the $Si_{0.5}Ge_{0.5}NW$ FET, where the gate control becomes negligible. This is due to the higher In doping in the NWs, which increases the carrier concentration, and narrows the depletion region, thereby preventing the gate electric field from effectively penetrating the channel. The weakening of gate control reduces the modulation of the channel conductance, increasing the SS and I_{off} in the FET devices. Additionally, the transfer characteristics of $Si_{1-x}Ge_xNW$ channels were simulated using the Silvaco TCAD 3D device simulator (Synopsys, Inc.). As shown in Fig. S8b, the simulated data exhibit a consistent trend with the experimental results. Additional details on the simulated energy bands are provided in Fig. S8c.

Thin channels and sufficiently large contact areas are essential for improving the electrical performance of SiGeNW FETs. Therefore, based on the previously developed step-necking process [43], we achieved $Si_{0.7}Ge_{0.3}NW$ structures with thin-diameter channels (D_{neck}) in the middle section to ensure full depletion, while maintaining thick profiles (D_{nw}) at both ends to provide sufficiently large contact areas for improved S/D. As shown in Fig. 5c, the In droplet moves along the top surface, facilitating the growth of $Si_{0.7}Ge_{0.3}NWs$. At the protrusion, the $Si_{0.7}Ge_{0.3}NW$ is stretched into a thinner segment ($D_{neck} < D_{nw}$). Once the In droplet transitions to the lower plane, the growth equilibrium is restored, resulting in thicker ends and forming a continuous thick/thin/thick $Si_{0.7}Ge_{0.3}NW$ structure. Detailed experimental procedures can be found in our previous study [43]. Unlike previous studies that employed SF_6 etching to create jumping steps perpendicular to the guiding terraces, this work uses C_4F_8 etching to achieve steeper jumping steps. These steps are more conducive to forming shorter and thinner necking regions ($D_{neck} < 20$ nm, $L_{neck} < 20$ nm). Additional details regarding the step-necking process are provided in Fig. S9.

To demonstrate the advantages of step-necking $Si_{0.7}Ge_{0.3}NW$ channels, FETs were fabricated by depositing Pt/Au contacts on the channel, followed by coating with a 25 nm Al_2O_3 dielectric layer and a 60 nm Al film as the gate electrode. The spacing between the two Pt/Au films was controlled to ~3 μm. The schematic structure of the device is shown in Fig. 5c. According to the I_{ds}–V_{ds} curve in Fig. S10, the contacts between the $Si_{0.7}Ge_{0.3}NW$ channel and S/D metal exhibit Schottky contact characteristic, indicating the nature of a SBT FET device. As illustrated in Fig. 5d, the uniformly $Si_{0.7}Ge_{0.3}NW$-FETs exhibits a relatively high I_{off} of 1×10^{-11} A at $V_{ds} = -0.1$ V with an I_{on}/I_{off} of $\sim 10^3$ and a large SS of 686 mV/dec, indicating incomplete depletion of the channel. In contrast, the step-necking $Si_{0.7}Ge_{0.3}NW$-FET, featuring a thinner and shorter channel, benefits from improved electrostatic control, achieving a significantly reduced SS of 135 mV/dec, a lower I_{off} of 1×10^{-13} A and a slightly higher I_{on} at $V_{ds} = -0.1$ V, corresponding to an I_{on}/I_{off} exceeding 10^5. Notably, at $V_{ds} = -0.5$ V, the I_{on}/I_{off} surpasses 10^6. The results demonstrate that the unique geometric structure of the step-necked $Si_{0.7}Ge_{0.3}NW$ channels enhances FET performance by improving electrostatic control, reducing SS, and achieving higher I_{on}/I_{off}. The method of extracting the mobility of $Si_{0.7}Ge_{0.3}NWs$ is provided in Fig. S11. Compared with the mobility of SiNWs (65 cm^2/V·s) [44], the mobility of $Si_{0.7}Ge_{0.3}NWs$ increased slightly to 76 cm^2/V·s.

To place our device results in context, we have included a benchmarking table (Table S1) that compares our IPSLS-grown SiGeNW FETs with Si, Ge, and SiGe NW FETs fabricated by both top-down and bottom-up approaches. This comparison highlights several advantages of the IPSLS method, including the low process temperature (≤450 °C) and the elimination of NW transfer steps required in bottom-up VLS growth. The

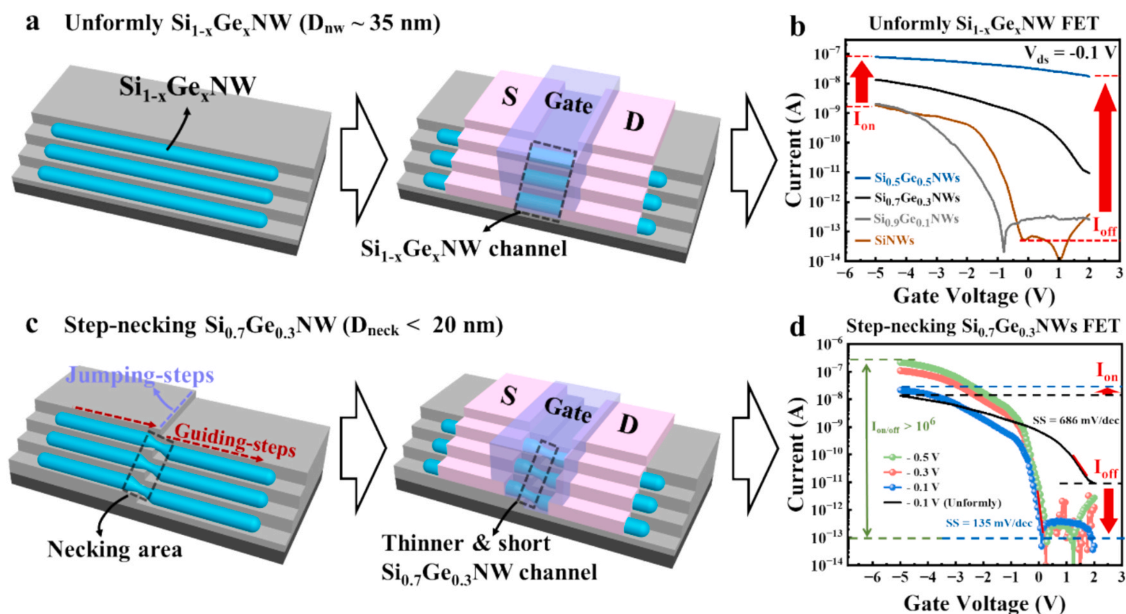

Fig. 5. (a) Schematic illustration of the $Si_{1-x}Ge_xNW$ FET based on uniformly thick channels. (b) The transfer characteristics of FETs based on uniformly thick SiNW, $Si_{0.9}Ge_{0.1}NW$, $Si_{0.7}Ge_{0.3}NW$, and $Si_{0.5}Ge_{0.5}NW$ channels at $V_{ds} = -0.1$ V. (c) Short-channel transistor built upon step-necking $Si_{0.7}Ge_{0.3}NWs$, where the thinner middle sections serve as the channel and the thicker ends serve as the S/D contacts. (d) Transfer curve of the step-necking $Si_{0.7}Ge_{0.3}NW$-FET.

step-constricted $Si_{0.7}Ge_{0.3}$NW FETs achieved SS = 135 mV/dec and $I_{on}/I_{off} > 10^6$, demonstrating competitive performance relative to other reported NW FETs. Nevertheless, the benchmarking also reveals that the performance of our current devices remains lower than the reported values for top-down NW FETs, underscoring the need for further optimization of nanowire composition, interface quality, and device architecture.

4. Discussion

This work provides a promising route toward the scalable, integrated catalytic growth of SiGeNW arrays as channel materials for p-type metal–oxide–semiconductor (PMOS) devices. Notably, the low-temperature, position-controlled growth of well-ordered 1D SiGeNW arrays directly on insulating dielectric layers reduces the reliance on pre-existing c-Si substrates and advanced lithography techniques, making this approach potentially attractive for future monolithic 3D integrated electronics and in-memory computing applications [45–47]. However, compared to SiGeNWs channels fabricated by top-down etching from epitaxial SiGe thin films using advanced lithography [48], the current SiGeNWs still require further optimization in terms of size uniformity and integration density. To address this, our previously demonstrated growth strategy based on ultra-narrow sidewall trench confinement for high-density integration of sub-10 nm SiNWs (with an interwire pitch of 10 nm) [30] could be extended and adapted to SiGeNW systems. Moreover, device performance remains to be improved, which could potentially be achieved through gate-all-around (GAA) architectures for enhanced electrostatic control. In this regard, our earlier development of an in situ SiNW release technique [31] provides a promising route for enabling suspended SiGeNW structures.

It is also worth noting that the presence of In precipitates in SiGeNWs may introduce recombination-active centers, posing a potential threat to the reliability of electronic and optoelectronic devices. This highlights the need to explore alternative catalyst materials. For instance, employing tin (Sn) catalysts for the growth of high-Ge-content SiGeSnNWs or even GeSnNWs may enable the realization of direct-bandgap semiconductors [49,50]. Moreover, achieving complementary metal–oxide–semiconductor (CMOS) technology requires n-type channels. In this regard, our previous work demonstrated that both Bi-catalyzed growth [51] and precursor doping strategies [52] enables the formation of n-type NWs, offering a promising pathway toward n-type SiGeNWs. Additionally, SiGeNWs with higher Ge fractions are expected to provide enhanced carrier mobility, and we envision that the controlled growth of pure GeNWs will become a central focus of our future research.

5. Conclusions

In summary, utilizing the in-plane solid–liquid–solid (IPSLS) mechanism at a low temperature of 250 °C, we demonstrated the growth of ordered SiGe nanowire (SiGeNW) arrays that are free of substrate-induced epitaxial strain. The resulting nanowires exhibit tunable Ge compositions (0–75 at.%), uniform diameters of ~35 nm, and a regular spacing of 100 nm. Electrical measurements reveal a systematic reduction in SiGeNW resistivity with increasing indium doping concentration, underscoring the effectiveness of compositional control and self-doping strategies for enhancing FET performance. Fabricated FETs with step-constricted $Si_{0.7}Ge_{0.3}$NW channels achieved a subthreshold swing of 135 mV/dec and an on/off current ratio exceeding 10^6, confirming the feasibility of integrating strain-free SiGeNWs as p-type channels in future PMOS technology.

Credit author statement

J.A. carried out the experiments, analyzed the data, and wrote the manuscript. L.W. participated in the Raman characterization. Z.H. contributed to the device simulations. X.S., J.W., and L.Y. oversaw all phases of the research and revised the manuscript. All authors participated in the writing and revision of the manuscript. All the authors have approved the final manuscript.

CRediT authorship contribution statement

Junyang An: Writing – original draft, Methodology, Investigation, Formal analysis. **Lei Wu:** Formal analysis, Data curation. **Zhiyan Hu:** Software, Methodology. **Xiaopan Song:** Formal analysis. **Junzhuan Wang:** Writing – review & editing, Supervision, Project administration, Formal analysis, Data curation. **Linwei Yu:** Writing – review & editing, Project administration, Conceptualization.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Acknowledgments

This study was supported by the National Natural Science Foundation of China for Distinguished Young Scholars No. 62325403, National Key Research Program of China under Grant No. 92164201, National Basic Research Program of China 2024YFA1208900, Jiangsu Funding Program for Excellent Postdoctoral Talent under No. 2024ZB427, and the China Postdoctoral Science Foundation under Grant Number 2025T180143.

Appendix A. Supplementary data

The fabrication process of multi-steps (Fig. S1); SEM image of SiGeNW with Ge content exceeding 75 % (Fig. S2); TEM calibration using SiNW (Fig. S3); TEM characterization of another $Si_{0.5}Ge_{0.5}$NW sample (Fig. S4); XPS spectra of a-$Si_{1-x}Ge_x$ precursor films with different compositions (Fig. S5); Four-point probe measurement of SiGeNWs (Fig. S6); The operating principle of SiGeNW FET (Fig. S7); Simulated Structure of SiGeNW FET (Fig. S8); The dynamics of step-necking SiGeNWs (Fig. S9); I_{ds}-V_{ds} curve of $Si_{0.7}Ge_{0.3}$NW NK-FETs (Fig. S10); The calculation of $Si_{0.7}Ge_{0.3}$NWs mobility (Fig. S11). Supplementary data to this article can be found online at https://doi.org/10.1016/j.apsusc.2025.164889.

Data availability

The data in this work is available from the authors upon reasonable request.

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