High-Performance S/D-First IGZO TFTs Integrated With p-Type Si Nanowire FETs for Complementary Logic

Le Weng#, Wentao Qian#, Shuo Zhang, Zhinong Yu*, Junzhuan Wang*, Linwei Yu*

***Abstract*—High-performance complementary logic requires process-compatible n-type and p-type devices with low degradation. Here, we report the heterogeneous integration of source/drain-first (S/D-first) IGZO TFTs with in-plane solid–liquid–solid (IPSLS)-grown p-type Si nanowire (SiNW) FETs for complementary logic. The S/D-first process effectively suppresses lithography-induced channel damage, thereby enabling that the field-effect mobility of IGZO TFT increases to 31.4 $cm^2 V^{-1} s^{-1}$, while the subthreshold swing decreases 166 mV dec^{-1}. Meanwhile, the p-SiNW FETs exhibit a field-effect mobility of 54 $cm^2 V^{-1} s^{-1}$ and a subthreshold swing of ~117 mV dec^{-1}. Based on these complementary devices, low-power inverters as well as NOR, NAND, and AND logic gates are demonstrated, confirming the feasibility of combing the n-IGZO TFTs and p-SiNW FETs for heterogeneous complementary logic integration.**

***Index Terms*— Complementary logic, sputtered IGZO, in-plane solid–liquid–solid (IPSLS), p-type SiNW FETs, heterogeneous integration**

I. Introduction

Both p-type and n-type devices are essential for realizing low-temperature complementary logic circuits[1]. In recent years, p-type FETs based on IPSLS-grown Si nanowires (SiNWs) are attractive pull-up devices owing to their well-defined one-dimensional channels, low leakage current, and superior electrostatic control with top-gate architectures[2-4]. To pair with these p-type devices, IGZO TFTs serve as ideal n-type pull-down candidates because of their high electron mobility, low off-state current, and low-temperature processability[5-7]. However, realizing scalable SiNW/IGZO complementary logic requires n-IGZO TFTs that can be lithographically defined while maintaining high channel quality. Existing lithography-based IGZO TFT processes, such as protective-layer or self-aligned schemes[8, 9], often rely on additional etching, plasma treatment, or thermal repair steps, which increase process complexity and may introduce channel or interface damage. Moreover, in conventional IGZO-first processes, the IGZO channel is deposited before source/drain (S/D) formation, exposing the active layer directly to photoresist coating, development, lift-off solvents, and metal deposition. Such process exposure can induce organic residues, surface disorder, oxygen-vacancy-related defects, and nonideal contact regions, resulting in degraded mobility, enlarged subthreshold swing (SS), and reduced current drivability[10]. Therefore, a damage-minimized and lithography-compatible IGZO process is imperative for realizing well-matched n-type pull-down devices for SiNW/IGZO complementary logic.

In this work, we develop an S/D-first process for integrating n-type IGZO TFTs with IPSLS-grown p-SiNW FETs. By defining the S/D electrodes before IGZO deposition, this process suppresses lithography-induced channel degradation, improves contact/access transport, and reduces charge trapping at the gate-dielectric/IGZO interface. The optimized n-IGZO TFTs exhibit enhanced mobility, steeper subthreshold swing, and an on/off current ratio exceeding 10^7, providing adequate drive capability and effective current matching with the p-SiNW FETs. Based on these complementary devices, planar complementary inverters, alongside NOR, NAND, and AND logic gates are successfully demonstrated.

II. Experiment

IGZO TFTs with width/length of 50/10 μm were fabricated using IGZO-first and S/D-first process sequences, differing only in the formation order of the 30-nm Ni S/D electrodes and 20-nm IGZO channel. The IGZO film was sputtered in an Ar/O_2 atmosphere with a flow ratio of 10:1 at 5 Pa and 100 W, followed by annealing at 300 °C in N_2 for 30 min. A 6/9-nm-thick Al_2O_3/HfO_2 bilayer was deposited by ALD as the gate dielectric, followed by a 60-nm Ni top gate.

For p-SiNW FETs, AZ5214 photoresist was patterned on 500-nm SiO_2, followed by cyclic ICP etching using C_4F_8/O_2 plasma to form terraced guiding steps. Subsequently, a 5-nm indium (In) layer was thermally evaporated on the side of steps and then treated by H_2 plasma at 200 °C in the PECVD system to form discrete In droplets. After 10-nm a-Si deposition, the temperature was raised to 300 °C to melt In droplets again, making them absorb a-Si at the front end while precipitate crystalline SiNWs at the rear end along the guiding steps. Then, 30-nm Ni S/D electrodes, a 6/9-nm Al_2O_3/HfO_2 gate dielectric,

This work was supported in part by the National Natural Science Foundation of China for Distinguished Young Scholars under Grant No. 62325403 (L.Y.), National Basic Research Program of China under Grant No. 2024YFA1208900 (J.W.). *(Corresponding authors: Linwei Yu, Junzhan Wang and Zhinong Yu)*

L. Weng, W. Qian, J. Wang and L. Yu are with School of Electronic Science and Engineering//National Laboratory of Solid-State Microstructures, Nanjing University, Nanjing 210093, China(e-mail: yulinwei@nju.edu.cn, wangjz@nju.edu.cn).

S. Zhang and Z. Yu are with School of Optics and Photonics, Beijing Engineering Research Center of Mixed Reality and Advanced Display, Beijing Institute of Technology, Beijing 100081, China(e-mail: znyu@bit.edu.cn).

L. Weng and W. Qian contributed equally to this work

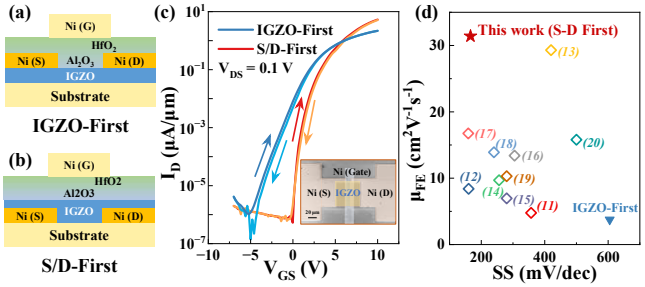

Fig.1 Schematic cross-section of the (a) IGZO-first and (b) S/D-first TFTs. (c) Measured transfer characteristics and hysteresis curves of two TFTs. The inset shows an optical image of the S/D-first TFT. (d) Benchmark plot of u_{FE} versus SS for Al_2O_3 and/or HfO_2 -based devices.

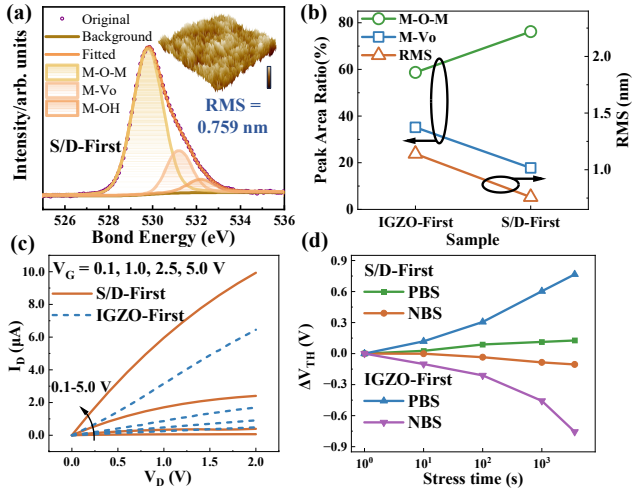

Fig.2 (a) Measured O 1s XPS spectrum and peak fitting of the S/D-first sample. The inset shows AFM morphology of the S/D-first sample (5×5 μm). (b) Comparison of the O 1s chemical-state composition and surface roughness of the IGZO-First and S/D-First samples. (c) Measured output characteristics of the IGZO-First and S/D-First TFT. (d) The corresponding V_{TH} extracted from the measured transfer curves under different stress times.

and a 60-nm Ni top gate were sequentially formed.

For the inverters and logic gates, p-SiNWs were first fabricated with patterned S/D electrodes, followed by IGZO deposition, common ALD gate dielectric formation, and Ni top-gate patterning.

III. Results and Discussion

Fig. 1 compares the structures and electrical characteristics of IGZO TFTs fabricated via IGZO-first and S/D-first process sequences. Compared with the IGZO-first process shown in Fig. 1(a), the S/D-first process shown in Fig. 1(b) defines the Ni source/drain electrodes before IGZO deposition, thereby preventing the active IGZO channel from direct exposure to subsequent S/D lithography and patterning. The transfer characteristics in Fig. 1(c) show that the S/D-first TFT exhibits steeper turn-on behavior and higher current drivability. After optimization, the field-effect mobility (μ_{FE}) of the S/D-first IGZO TFT increases from 7.79 to 31.4 $cm^2 V^{-1} s^{-1}$, while the SS decreases from 605 to 166 mV dec^{-1}, with an on/off current ratio exceeding 10^7. It also shows a smaller hysteresis of 11 mV than the IGZO-first TFT (52 mV). The benchmark plot in Fig. 1(d) further shows that the S/D-first device achieves a highly

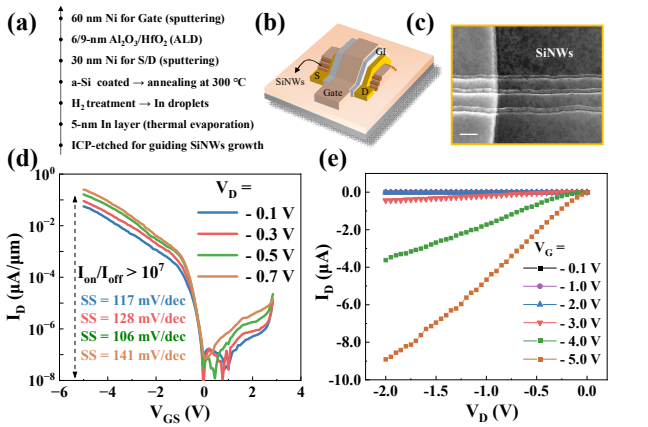

Fig.3 (a) Fabrication process flow of the p-SiNW FETs. (b) Schematic structure of the top-gate p-SiNW FET. (c) Measured SEM image of the guided SiNWs (Scalebar: 200nm). (d) Measured transfer characteristics of the p-SiNW FET measured at different V_D. (e) Measured output characteristics of the p-SiNW FET.

competitive SS and μ_{FE} relative to reported IGZO TFTs with Al_2O_3 and/or HfO_2 -based gate dielectrics[11-20] .

To clarify the origin of the improved performance in the S/D-first TFTs, XPS, AFM, output, and bias-stress analyses were performed, as shown in Fig. 2. The O 1s spectra in Fig. 2(a) were deconvoluted into metal-oxygen bonds (M-O-M), oxygen vacancy related components (M-Vo) and hydroxyl-related (M-OH) components. For the IGZO-first sample, the M-O-M fraction is 58.70%, while the M-Vo component reaches 35.17%, indicating substantial process-induced degradation of the IGZO surface. In contrast, the S/D-first sample shows an increased M-O-M fraction of 76.19% and a reduced M-Vo fraction of 17.78%. Together with its smoother AFM surface, these results indicate a denser metal-oxygen network with fewer oxygen vacancy related defects. Beyond improving channel quality, the S/D-first architecture enhances gate control over the contact regions. As shown in Fig. 2(c), its current advantage becomes pronounced at high V_{GS}, where the larger low-V_D output conductance and nearly linear behavior indicate improved carrier injection and reduced effective on-state contact resistance. After 3600 s of PBS and NBS at $V_{GS} = \pm 2$ V (E_{ave} = 1.33 MV/cm), the S/D-first TFT exhibits threshold-voltage shifts (ΔV_{TH}) of 127 and -105 mV, respectively, versus 766 and -756 mV for the IGZO-first TFT, as shown in Fig. 2(d). Given their different initial V_{TH} values (1.05 and -1.25 V for S/D-first and IGZO-first TFT, respectively), the smaller normalized shift $\Delta V_{TH}/|V_{OV}|$ of the S/D-First TFT, where $V_{OV} = V_{GS} - V_{TH}$, further confirms improved channel and interface quality and electrical stability.

Despite these advantages, the S/D-first process may cause nonuniform IGZO coverage near electrode edges and restrict the choice of contact metals and thermal budget. These issues can be mitigated through thickness optimization and stable contact materials.

Fig.3(a) summarizes the SiNW FET device fabrication process, in which three-tier guiding steps are formed by cyclic ICP etching to guide the subsequent SiNW growth. Fig. 3(b) illustrates the top-gate SiNW FET structure, while Fig. 3(c) presents an SEM image of orderly SiNWs with diameters of approximately 25 nm, which are contacted by the S/D metal

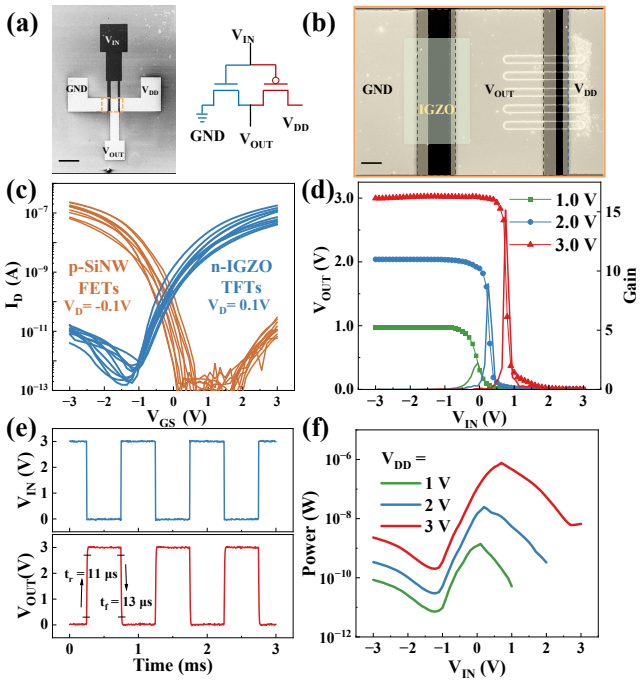

Fig.4 (a) SEM image and circuit schematic of the inverter composed of a p-SiNW FET and an n-IGZO TFT (Scalebar: 100 μm). (b) Enlarged image showing the integrated channels region (Scalebar: 10 μm). (c) Measured transfer characteristics of ten n- and p-FETs ($|V_D|$ = 0.1 V). (d) Measured voltage transfer characteristics and gain of the inverter. (e) Measured dynamic waveforms of the inverter at 1 kHz square-wave input. (f) Measured static power consumption of the inverter.

electrodes with a channel width of 3 μm. The representative p-SiNW FET in Figs. 3(d)-(e) exhibits typical p-type behavior, an I_{ON}/I_{OFF} exceeding 10^7 and a minimum SS of 106 mV dec^{-1}, indicating effective electrostatic gate control over the SiNW channels. The output characteristics show clear gate-dependent current modulation, which can be ascribed to the low-resistance contact between the Ni S/D electrodes and the SiNWs.

Based on optimized n-IGZO TFTs and IPSLS-grown p-SiNW FETs, planar complementary inverters were fabricated. Figs. 4(a) and 4(b) show the inverter layout, equivalent circuit, and enlarged integrated region, where the IGZO and SiNW channels are connected at the output node. Fig. 4(c) shows the transfer characteristics of ten p/n FET pairs, confirming reproducible current matching required for balanced and low-power inverter operation. The voltage transfer characteristics in Fig. 4(d) exhibit clear switching with increasing gain as V_{DD} increases, reaching a peak value of 15 at V_{DD} = 3 V. The dynamic response of the inverter was further evaluated using a 1 kHz square-wave input varying between 0 and 3 V. As shown in Fig. 4(e), the inverter exhibits full-swing output with rise and fall times of 11 and 13 μs, respectively. Fig. 4(f) shows pW-level minimum static power across different V_{DD} values, enabled by the low off-state currents of both transistors. The gate-leakage-induced current upturns in Fig. 4(c) only slightly increase the residual power near $V_{IN} = \pm V_{DD}$, but does not compromise its low-power operation. Further reductions can be achieved by optimizing V_{TH} alignment, SS, gate-dielectric quality, and gate-overlap area.

Further, complementary NOR, NAND, and AND gates were demonstrated, as shown in Fig. 5. Their optical images and

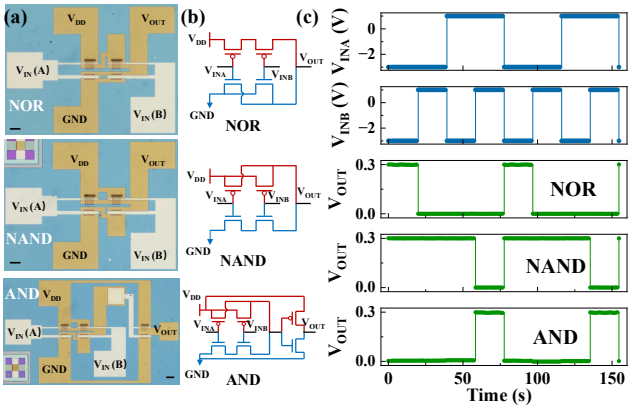

Fig.5 (a) Optical images of the fabricated NOR, NAND, and AND gates (Scalebar: 50 μm). (b) Corresponding circuit schematics of the p-SiNW/n-IGZO complementary logic gates. (c) Measured transient input and output characteristics of complementary logic gates.

TABLE I
BENCHMARK COMPARISON OF CFET BASED ON IGZO TFTS

Material (p/n)	SS (p/n) (V/dec)	V_{DD} (V)	Gain	Static power	Ref
SnO+ IGZO	28.7/ 1.84	40	24	12.5 μW	[21]
LTPS+ IGZO	0.65/ 0.25	8	114	10 μW	[22]
Te+ IGZO	0.4/ 0.6	3	75	30 nW	[23]
SiNWs+ IGZO	**0.12/ 0.17**	**3**	**15**	**0.2 nW**	**This work**

corresponding p-SiNW/n-IGZO circuit schematics are presented in Figs. 5(a) and 5(b). Dynamic measurements were performed at V_{DD} = 0.3 V by applying sequential voltage signals to V_{INA} and V_{INB}, where input voltages of 1 and -3 V represent logic '1' and '0', respectively. The measured output signals switch consistently with the designed logic states, as shown in Fig. 5(c), confirming the correct transient operation of the SiNW/IGZO complementary logic gates. The power consumption of the logic gates was also evaluated, and the maximum static power consumption of the NOR, NAND, and AND gates remained below 25 pW under all input conditions.

Table I benchmarks the present p-SiNW/n-IGZO logic against reported IGZO-based complementary circuits. The low and closely matched SS values of 0.12 and 0.17 V/dec^{-1}, together with the high mobilities and well-matched p/n drive currents, enable an ultralow static power consumption of 0.2 nW at V_{DD} = 3 V. Moreover, lithographically defined SiNWs guiding steps, scalable IGZO sputtering, and conformal ALD gate dielectrics provide a practical pathway toward large-area manufacturing of the complementary logic platform.

IV. CONCLUSION

In summary, high-performance S/D-first IGZO TFTs were developed and integrated with IPSLS-grown p-SiNW FETs for complementary logic. The S/D-first process suppresses lithography-induced channel degradation, improves channel and interface quality, and lowers contact resistance, resulting in a higher mobility and smaller SS. By combining with p-SiNW FETs, low-power complementary inverters alongside NOR, NAND, and AND gates were successfully demonstrated. This work provides a scalable and process-compatible route for heterogeneous p-SiNW/n-IGZO complementary integration.

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