37.2 A 47.0Tb/s/mm 112Gb/s/pin PAM4 Single-Ended Transceiver Featuring 4-Aggressor Crosstalk Cancellation and Supply-Noise Tolerance for Short-Reach Memory Interfaces

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Abstract

This paper presents a five-lane 112Gb/s/pin PAM4 single-ended transceiver in 28nm CMOS for high-density short-reach memory interfaces. Low-power triple-equalization, 4-aggressor shape-fitting crosstalk cancellation and supply-noise-tolerant clock distribution networks are involved to improve the signal integrity. The design demonstrates robust performance against severe crosstalk and supply noise, achieving an energy efficiency of 0.52pJ/b and an edge density of 47.0Tb/s/mm.

The rapid advancement of high-performance computing and AI promotes the evolutions of short-reach memory interfaces (e.g. HBM), die-to-die and chiplet links (e.g. UCIe); these interfaces utilize single-ended (SE) data transmissions for high-bandwidth I/O density. However, SE signaling is vulnerable to interference and noise: e.g. crosstalk (XT) and supply noise (SN). As the per-pin data rate exceeds 20Gb/s, using higher-level pulse-amplitude modulation (PAM) becomes essential: PAM4 is used for 22Gb/s GDDR6X [1] and PAM3 used for 42Gb/s GDDR7 [2]. However, the reduced signal-to-noise ratio (SNR) introduces greater signal-integrity challenges. The transmitter (TX) in [3] uses a feed-forward equalizer (FFE) and crosstalk cancellation (XTC) to cancel far-end crosstalk (FEXT) for 3D-staggered interposer channels, but it is limited to 4Gb/s NRZ. A 24Gb/s/pin PAM4 transceiver (TRX) [4] uses a PAM-based XTC scheme, but does not address SN. The clock-referenced PAM3 TRX proposed in [5] tolerates both SN and XT, but only two aggressors are considered, which does not address the high-density scenarios in multi-layer interposers where more than two adjacent aggressors can impair the victim signal [6].

To address these problems, this paper presents a 112Gb/s/pin PAM4 single-ended TRX, featuring four-aggressor XTC and SN tolerance. Figure 37.2.1 shows the top-level architecture of the implemented TRX and the on-chip 2mm channels. The TRX includes 5 SE data lanes and 1 differential clock lane. Each data lane sends 112Gb/s data using the proposed energy-efficient triple-equalization (TEQ) driver and termination scheme. The four-aggressor shape-fitting XTC is integrated into the driver. The receiver (RX) uses single-ended-to-differential (S2D) and two-stage buffers to drive the slicers. The clock lane shares the same 4:1 multiplexer, driver and termination as those of the data lanes to transmit the differential quarter-rate forwarded clock. Injection-locked oscillators (ILOs) are used as an I/Q-phase generator (IQG) in the clock lane's RX; per-pin de-skew circuits in the data-lane RXs are also based on ILOs. The 14GHz four-phase clocking architecture comprises of a transmission-line (TL) based global clock-distribution network (CDN) and per-lane local CDNs, both of which are SN insensitive; thus, minimizing power-supply-induced jitter (PSIJ). Moreover, the on-chip 2mm silicon-interposer-mimicked channels are designed as a two-layer structure with a horizontal pitch of 2.35µm and a vertical pitch of 1.75µm: exhibiting high channel density and severe four-adjacent-aggressor XT. The insertion loss (IL) of the channel is 3.9dB at Nyquist (28GHz); the worst case IL-to-FEXT ratio for the same-layer aggressors is 22.4dB, and for the different-layer aggressors is 25.5dB.

Figure 37.2.2 shows the low-power TEQ driver and termination scheme. The relatively low IL of short-reach channels requires less equalization (EQ) and impedance matching for improved power efficiency. First, a small-size high-output-impedance driver is implemented to significantly decrease the power consumption of the driver and the preceding pre-driver, and to minimize the output-node capacitance. Second, the resistor-feedback amplifier (RFA)-based termination in the RX side offers not only a moderate level of impedance matching to reduce reflections, but also a signal amplification to enhance received signal swing. Compared to double- and single-sided resistor termination schemes, the RFA termination has an advantage in both power efficiency and signal integrity. Third, although the on-chip channel loss is only 3.9dB, the aggregate loss, including driver, channel, pad + ESD capacitance (~130fF at each side) and termination, is up to 12.8dB at 28GHz, which requires some EQ. However, rather than a power-hungry TX FFE or an RX continuous-time linear equalizer (CTLE), we use three types of lightweight equalizers targeting different frequency points, resulting in a smooth response within the Nyquist frequency. The passive RC equalizer and active inductor attenuate DC content and also provide gain at 5 and 15GHz. Further, a gain above 20GHz is achieved via the passive inductor in the RFA, which is implemented by middle-layer thin metal to reduce its footprint. Consequently, a 9.1dB signal-loss improvement is realized by TEQ within a 0.5mW power drawn from the active inductor. The overall power consumption of the TEQ driver and termination is <3.8mW.

Figure 37.2.3 displays the proposed four-aggressor shape-fitting XTC combined within the driver. The XT-compensated signal is coupled, via a capacitor, to superimpose it onto the transmitted signal. However, unlike off-chip channel cases [7], the FEXT noise produced by on-chip short-reach channels manifests as changes in polarity, delay and pulse shape. An XTC signal with an unmatched delay or ill-fitting shape cannot fully compensate for the XT noise. Conversely, the maximum level of XTC can be achieved by a delay-matched and shape-fitted XTC signal. In the proposed XTC, delay matching is realized by the digitally controlled capacitor, while shape fitting is achieved by tuning the rise and fall rates of the XTC signal. The measured eye shmoos based on recovered data at RX in the right of Figure 37.2.3 show that the proposed XTC expands the three PAM4 eyes at BER ≤ 10^{-9} from completely closed to having openings of 160 × 40, 200 × 60, and 200mUI × 60mV.

Figure 37.2.4 demonstrates the proposed SN-tolerant global and local CDNs. The global CDN is composed of coplanar transmission lines (TLs) and impedance-matched current-mode-logic (CML) drivers. Compared to a conventional inverter-chain CDN the CML driver has a significantly enhanced robustness against SN. The input capacitance of each lane can be absorbed as part of the capacitive components of the TL. With the effect of wire inductance, the distributed clocks maintain sharp edges without increasing power consumption [8]. On the other hand, the local CDN is implemented with inverter chains due to area constraints. However, the clock buffer in the local CDN is SN insensitive due to two mechanisms: (1) the back-to-back (B2B) inverters connected between the differential outputs exhibit an inverse polarity in SN sensitivity to that of the forward (F) inverters. Hence, the overall SN sensitivity decreases as the B2B:F inverter size ratio increases, leading to a reduced PSIJ. (2) The supply noise compensator (SNC) further reduces the residual PSIJ by modulating the inverter delay in the opposite direction to V_{DD} delay modulation [9]. Post-layout simulation shows that the PSIJ reduces from 3.1 to 0.5ps for the case of a 100mV_{pp} 200MHz SN when the B2B:F inverter size ratio is 1:2 and SNC is enabled. Clock-pattern eye diagrams are also measured under a clean V_{DD_CLK} and a noisy V_{DD_CLK}: a 5% degradation of eye width is observed when injecting 100mV_{pp} 200MHz SN onto V_{DD_CLK}.

Measured RX eye shmoos under various configurations of EQ, XTC and SNC are presented in Fig. 37.2.5. To evaluate both XTC and SN tolerance of the proposed TRX, apart from the aggregate 12.8dB signal loss considering both circuit and channel, all the four XT aggressors are activated and a 100mV_{pp} 200MHz SN is also injected onto V_{DD_CLK}. In the first configuration, equalizers (except passive inductor), shape-fitting XTC and SNC are all deactivated, resulting in no observable eye opening at BER ≤ 10^{-9}. In the second scheme, TEQ is fully enabled while XTC and SNC remain off, and the eye openings improve but remain invisible at BER ≤ 10^{-9}. In the third scheme, SNC is activated but XTC is not, there are still no effective eyes at BER ≤ 10^{-9}. Conversely, in the fourth configuration where XTC is activated but SNC is not, the measured eye openings are 120 × 30, 120 × 40, and 120mUI × 50mV. In the final scheme, both XTC and SNC are enabled and the measured eyes are open with 120 × 40, 160 × 60, and 160mUI × 60mV.

The prototype chip, including the proposed TRX and on-chip test channels, is fabricated in 28nm CMOS. The BER and eye-openings are measured via the on-chip PRBS7 pattern generator and checker, and an eye-opening monitor. A differential 14GHz clock is generated by an arbitrary waveform generator and fed into the TX. To emulate a noisy power supply environment, supply noise is injected onto V_{DD_CLK} via capacitive coupling on the PCB. Figure 37.2.6 demonstrates a performance comparison table with prior works for short-reach interfaces, the die micrograph and an area summary of active circuits including clock and data paths. Compared to prior works, the implemented TRX shows effective 4-aggressor XTC and SN tolerance for 112Gb/s/pin PAM4 signals, with a 0.52pJ/b energy efficiency, and an die-shore density of up to 47.0Tb/s/mm (including clock lanes).

Figure 37.2.7 summarizes the measured performance of shape-fitting XTC at different aggressor settings and SNC performance at various frequencies of 100mV_{pp} SN. It shows that the proposed XTC provides up to a 0.16UI extension for the four-aggressor worst case tested. Results show that the SNC is effective below 800MHz, but less effective at higher frequencies due to SNC bandwidth limitations. The test-chip power breakdown is also shown in Fig. 37.2.7.

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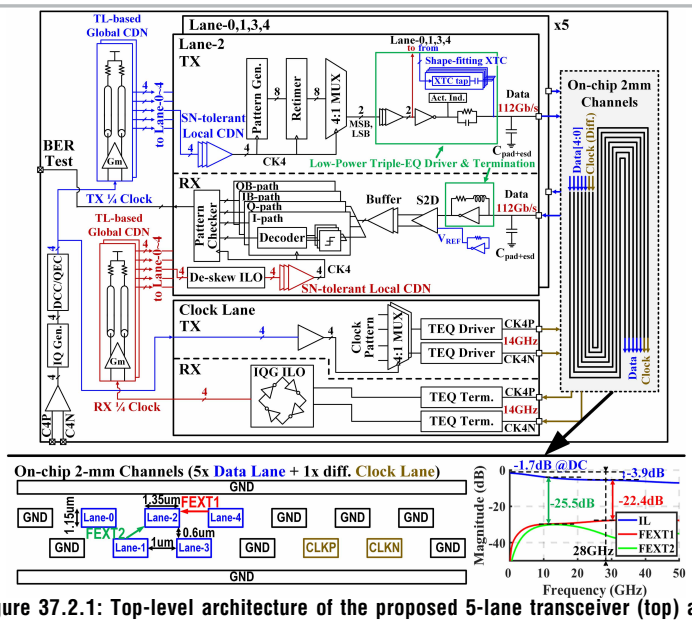


Figure 37.2.1: Top-level architecture of the proposed 5-lane transceiver (top) and characteristics of the on-chip channels (bottom).

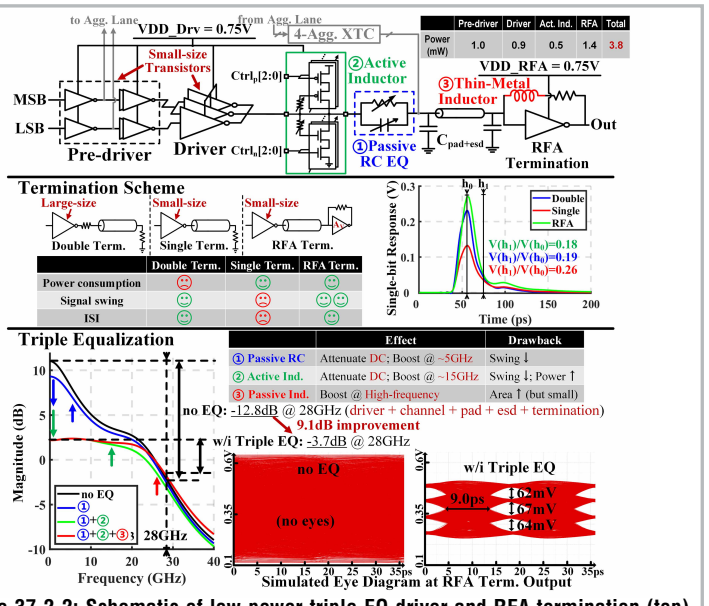


Figure 37.2.2: Schematic of low-power triple-EQ driver and RFA termination (top), comparisons of termination schemes (middle) and details of the triple-EQ (bottom).

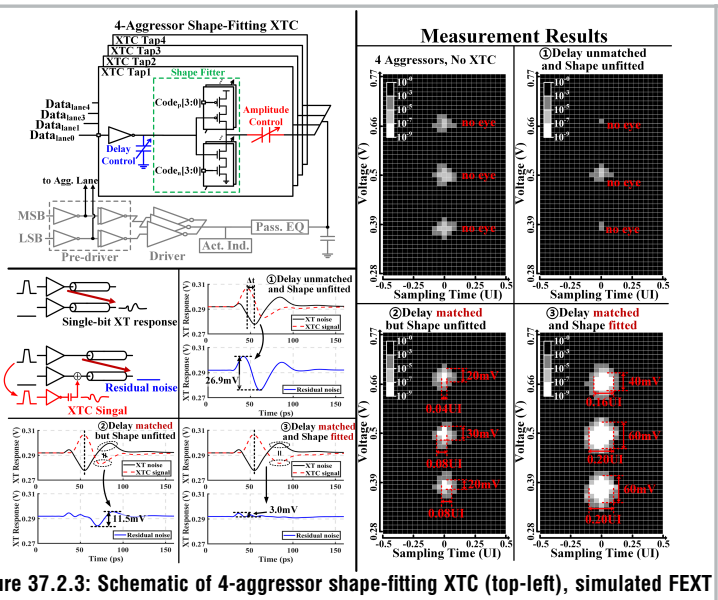


Figure 37.2.3: Schematic of 4-aggressor shape-fitting XTC (top-left), simulated FEXT responses (bottom-left) and measured eyes (right) for various schemes of delay and shape.

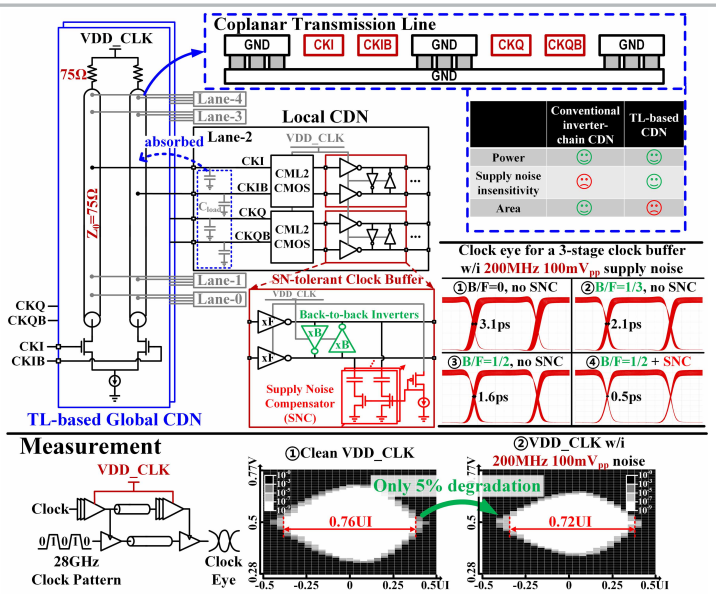


Figure 37.2.4: TL-based global and local CDN with SN-tolerant buffers (top), and measured clock eyes under 200MHz 100mV$_{pp}$ SN (bottom).

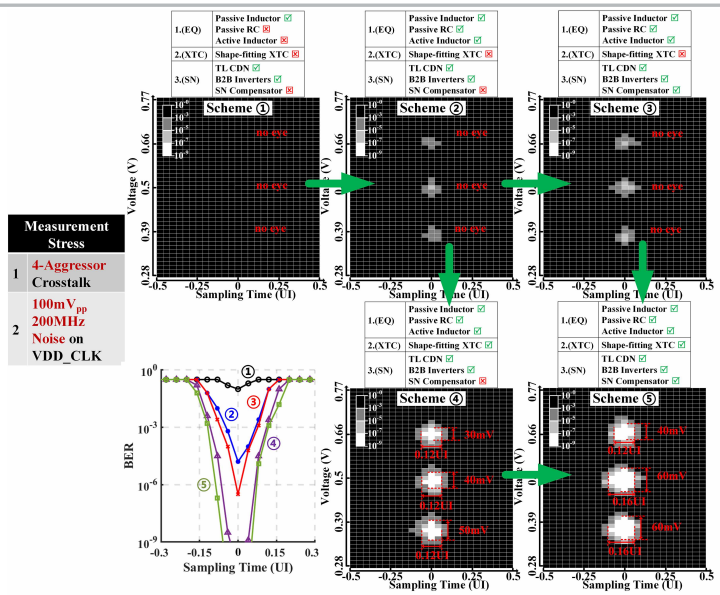
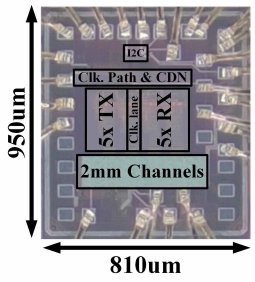


Figure 37.2.5: Measured eye diagrams and BER curves for various configurations of EQ, XTC and SNC, under 4-aggressor XT and 200MHz 100mV$_{pp}$ SN.



Block	Area (mm²)
5x TX	0.049
5x RX	0.061
Clock Path & CDN	0.015
Clock Lane	0.012
Active Area	0.137

	ISSCC'20 [3]	ISSCC'22 [10]	JSSC'23 [6]	JSSC'24 [4]	ISSCC'25 [5]	This Work
Technology	65nm	28nm	5nm	28nm	28nm	28nm
Data Rate (Gb/s/lane)	4	10	50.4	24	42	112
Signaling	Single-ended NRZ	Single-ended Di-code	Single-ended SBD	Single-ended PAM4	Single-ended PAM3	Single-ended PAM4
Channel Reach (mm)	6	6	1.2	4	2	2
XTC Type	FFE-XTC	No	Channel Layout	PAM-based XTC	FS-XTC	Shape-Fitting XTC
# of XTC Aggressor	4	/	/	2	2	4
Supply Noise Tolerance	No	No	No	No	Yes	Yes
Energy Efficiency (pJ/b)	1.5	0.39	0.30	0.46	0.28	0.52
Area (mm²/lane)	0.0023	0.0006	0.011	0.0010	0.0012	0.027
Edge Density (Tb/s/mm)	8	2	2.14	12	9.16*	47.0*

* Including clock lanes.

Figure 37.2.6: Die micrograph, area allocation, and comparisons with prior works for short-reach interfaces.

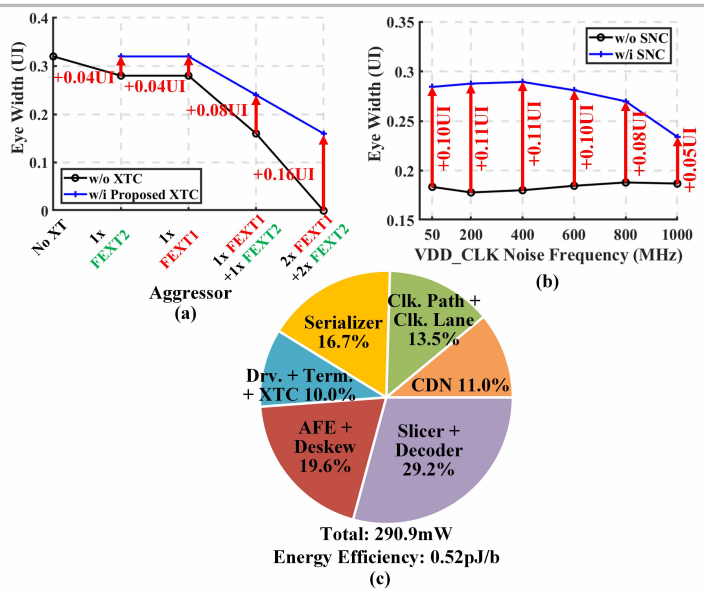


Figure 37.2.7: Measured eye widths at (a) various settings of XT aggressors, (b) various frequencies of 100mV$_{pp}$ SN, and (c) pie-chart showing the TRX power breakdown.

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